TMDSEVM6474L Schematic

SCHEMATIC PAGE DESCRIPTION :

01 : COVER SHEET
02 : SYSTEM BLOCK DIAGRAM
03 : DSP - BTMOD,GPIO,McBSP,TST HDR
04 : JTAG INTERFACE (ON BOARD / EXTERNAL EMULATION HEADER)
05 : DDR2 INTERFACE
06 : SRIO,SGMII, 88E6122
07 : 88E6122 POWER, I2C UART BRIDGE
08 : DSP - RESET, SMRT REFLEX POWER, E2PROM
09 : AMC CONNECTOR, AIF,MMC,IPMI
10 : DSP - CLOCK MANAGEMENT
11 : DSP - POWER SUPPLY
12 : FPGA - NAND FLASH INTERFACE
13 : BOARD POWER SUPPLY & RESET CIRCUITRY
14 : REVISION HISTORY & DUMMY PARTS

I2C ADDRESS TABLE :

REF DES	DESCRIPTION	7 BIT ADDRESS
U23	EEPROM	0x50, 0x51
U29	DUAL UART BRIDGE	0x4D
U12	FPGA	TBD
U34	CDCL6010	0x68

PCB Mechanical Details :

1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. PCB MATERIAL: FR4
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

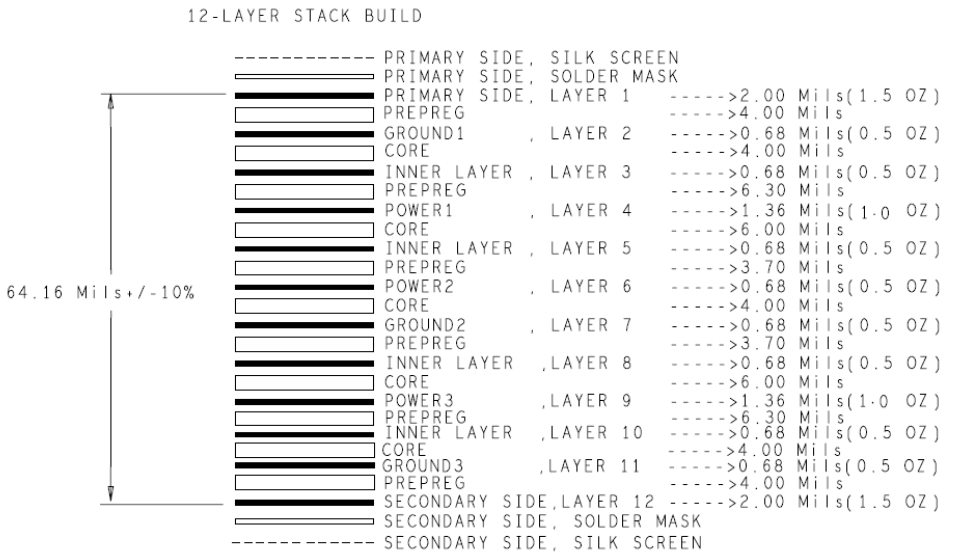
NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.

MAJOR REVISION HISTORY :

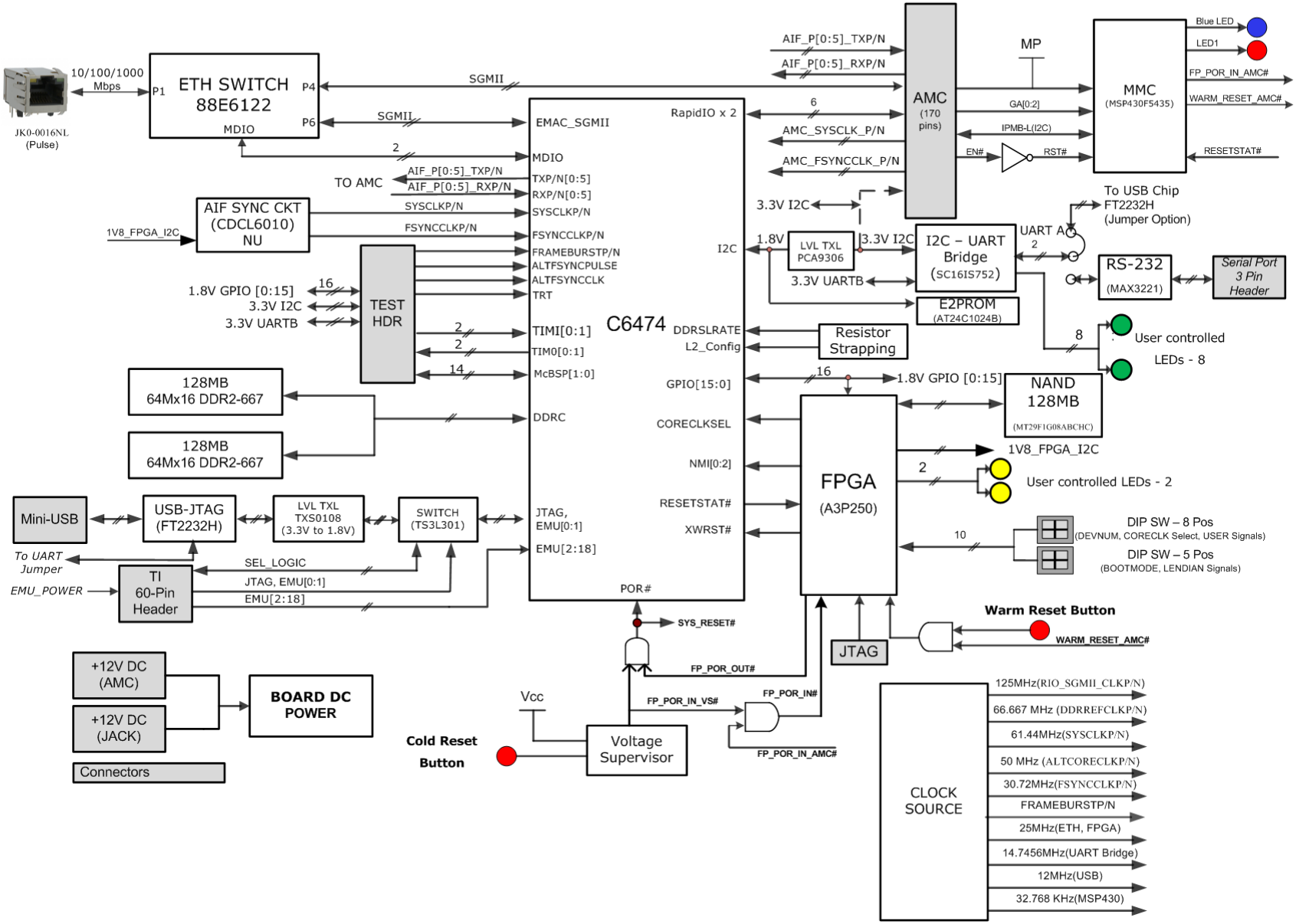
PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	1.0	Proto Build	06-AUG-2010
2.0	2.0	Production Build	11-OCT-2010

PCB LAYER STACK-UP DETAILS :

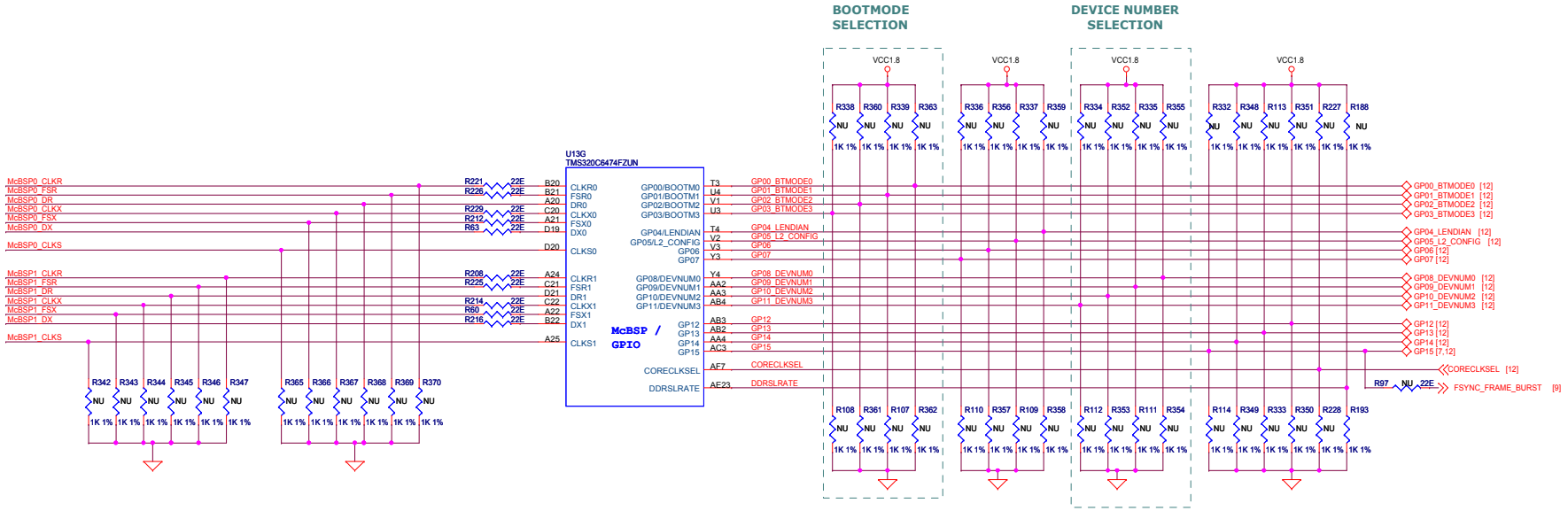


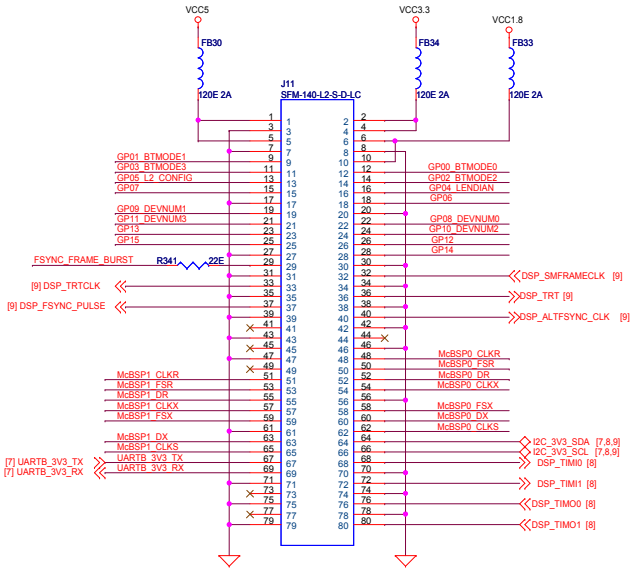
Project: TMDSEVM6474L	Designed for TI by eInfochips	
Title: Cover Sheet		
Size: C	Document Number: 16-00080-02	Rev: 2.0
Date: Monday, October 11, 2010	Sheet 1 of 14	

BLOCK DIAGRAM



Project: TMDSEVM6474L		Designed for TI by eInfochips
Title: System Block Diagram		
Size: C	Document Number: 16-00080-02	Rev: 2.0
Date: Monday, October 11, 2010	Sheet 2 of 14	

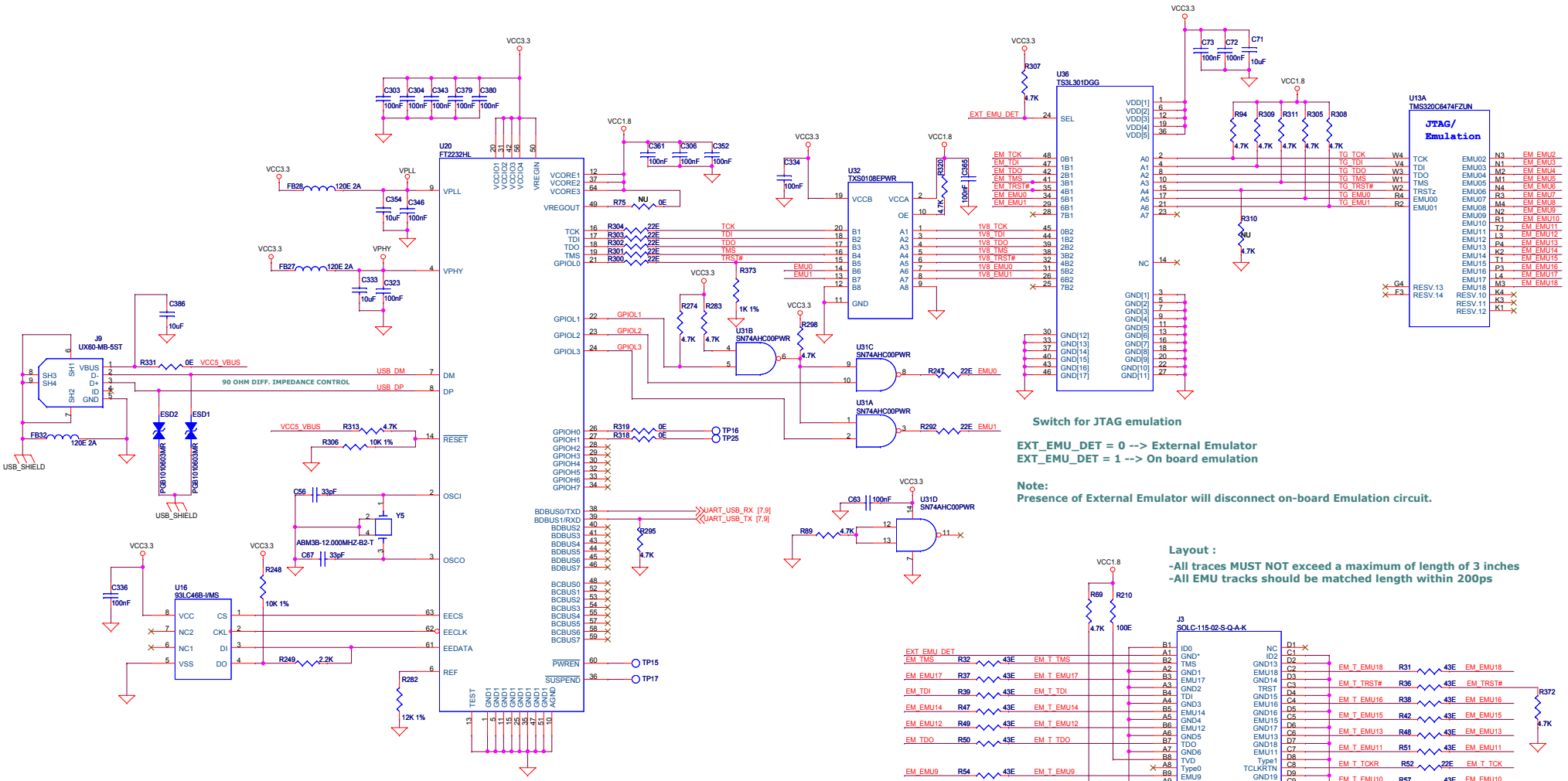




BOOTMODE[3:0]	DESCRIPTION
0000 (0)	No Boot
0001 (1)	I2C Master Boot A (Slave Address : 0x50H)
0010 (2)	I2C Master boot B (Slave address : 0x51H)
0011 (3)	I2C Slave Boot
0100 (4)	EMAC Master Boot
0101 (5)	EMAC Slave Boot
0110 (6)	EMAC Forced - Mode Boot
0111 (7)	Reserved
1000 (8)	Serial Rapid IO Boot (Config 0)
1001 (9)	Serial Rapid IO Boot (Config 1)
1010 (10)	Serial Rapid IO Boot (Config 2)
1011 (11)	Serial Rapid IO Boot (Config 3)
10xx (12-15)	Reserved

Note :
(1) GPIO, McBSP[0:1], Timer[0:1] and FSYNC signals connected to connector J11, are 1.8V level I/Os.
(2) UARTB and I2C signals connected to connector J11, are 3.3V level I/Os.

Project: TMDSEVM6474L	Designed for TI by eInfochips	
Title: BTMOD,GPIO,McBSP,TST HDR		
Size: C	Document Number: 16-00080-02	Rev: 2.0
Date: Monday, October 11, 2010	Sheet 3 of 14	



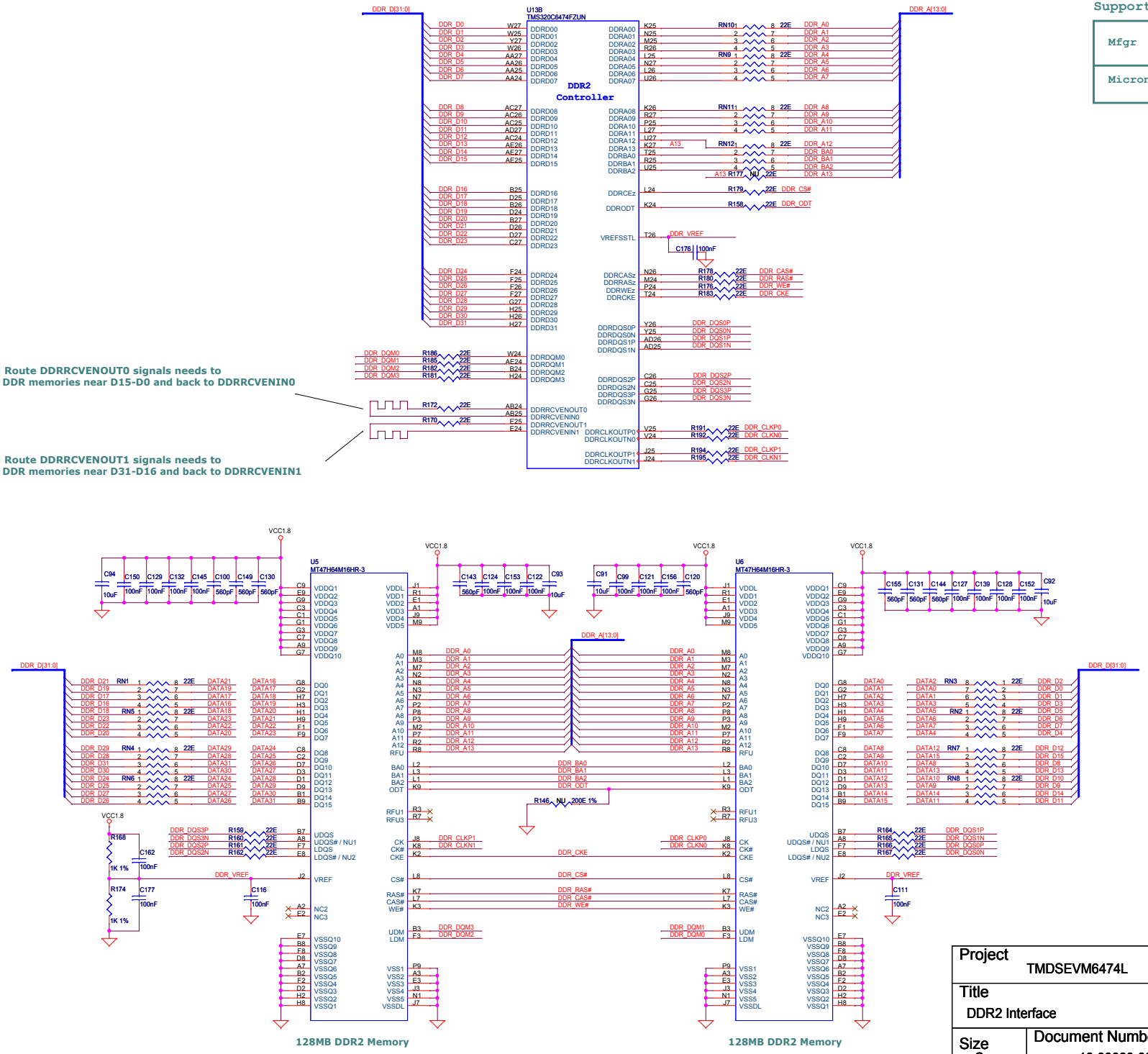
Project: TMDSEVM6474L	Designed for TI by eInfochips	
Title: JTAG Interface		
Size: C	Document Number: 16-00080-02	Rev: 2.0
Date: Monday, October 11, 2010	Sheet 4 of 14	

Supported Memories (84 FBGA) :

Mfgr	256MB (128MB x 2)	512MB (256MB x 2)
Micron	MT47H64M16HR-3	MT47H128M16HG-3

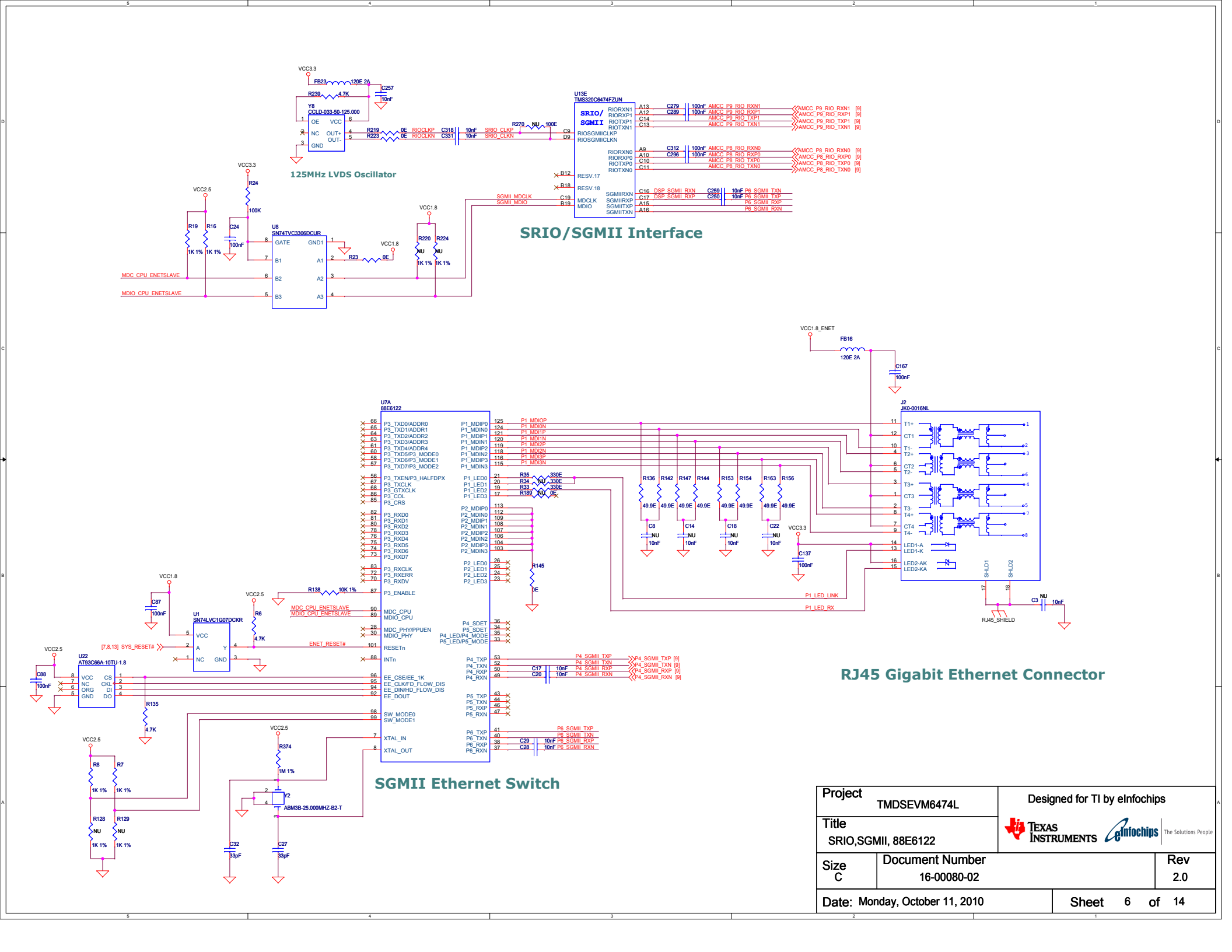
NOTE: Route DDRRCVENOUT0 signals needs to run to DDR memories near D15-D0 and back to DDRRCVENIN0

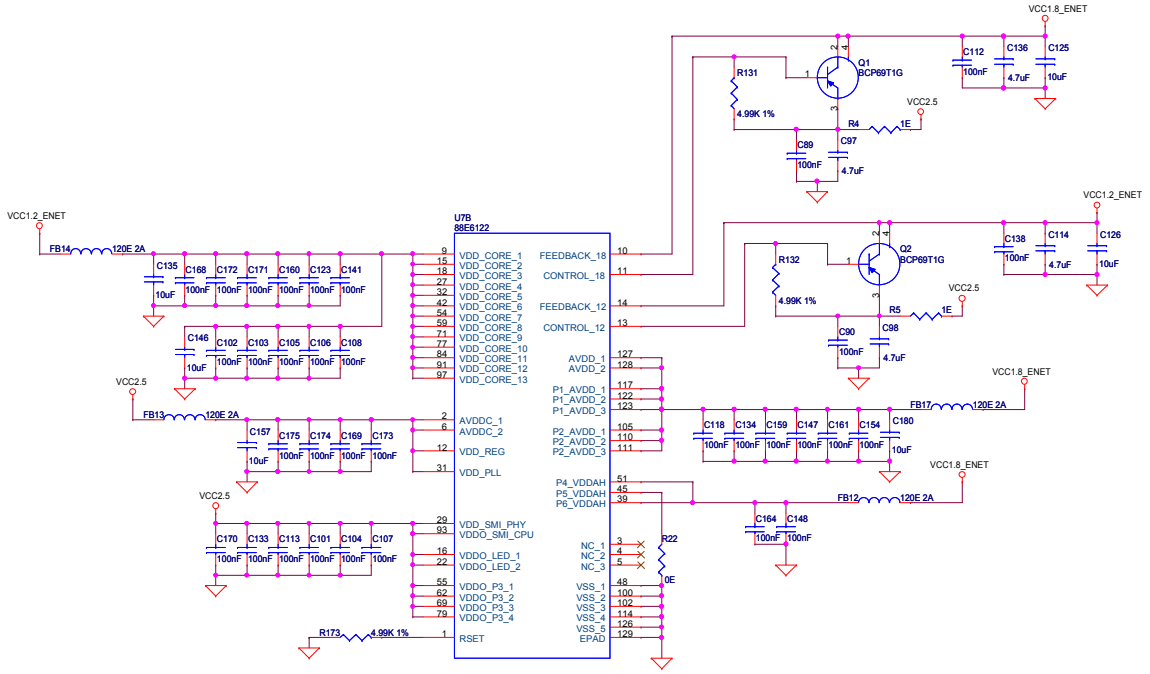
NOTE: Route DDRRCVENOUT1 signals needs to run to DDR memories near D31-D16 and back to DDRRCVENIN1



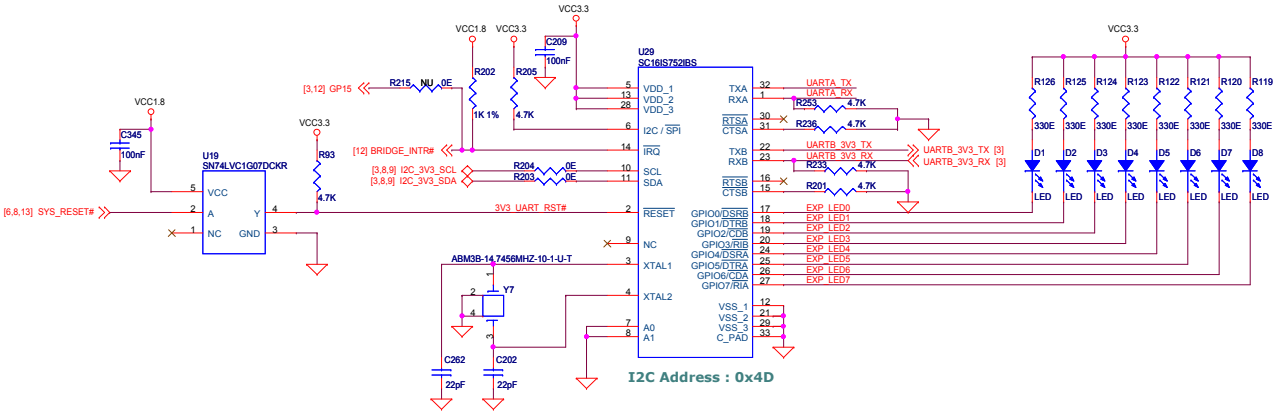
256MB DDR2 Memory Interface

Project: TMDSEVM6474L	Designed for TI by eInfochips	
Title: DDR2 Interface		
Size: C	Document Number: 16-00080-02	Rev: 2.0
Date: Monday, October 11, 2010	Sheet 5 of 14	

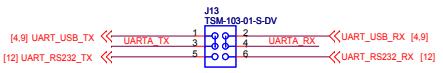

125MHz LVDS Oscillator
SRIO/SGMII Interface
RJ45 Gigabit Ethernet Connector
SGMII Ethernet Switch
Project
TMDSEVM6474L
Designed for TI by eInfochips
Title
SRIO,SGMII, 88E6122
Size
C
Document Number
16-00080-02
Rev
2.0
Date: Monday, October 11, 2010
Sheet 6 of 14



Ethernet Switch Power Supply



I2C - UART Bridge

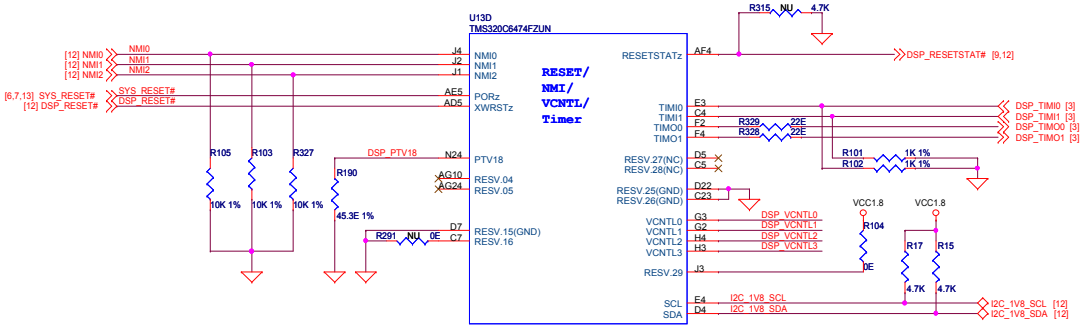


J13.3 to J13.1 & J13.4 to J13.2: UART over USB Connector J9 (Default)

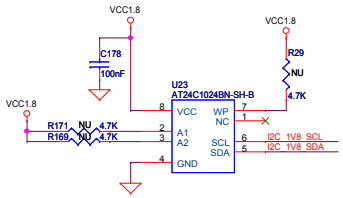
J13.3 to J13.5 & J13.4 to J13.6: UART over 3-Pin Header J10

UART Route Select Jumpers

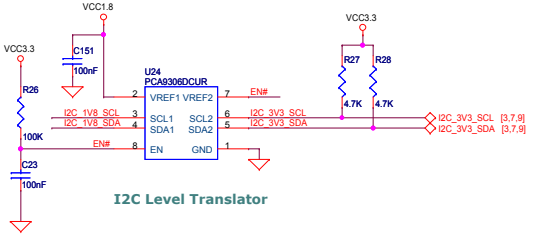
Project: TMDSEVM6474L	Designed for TI by eInfochips	
Title: 88E6122 Supply,I2C UART		
Size: C	Document Number: 16-00080-02	Rev: 2.0
Date: Monday, October 11, 2010	Sheet 7 of 14	



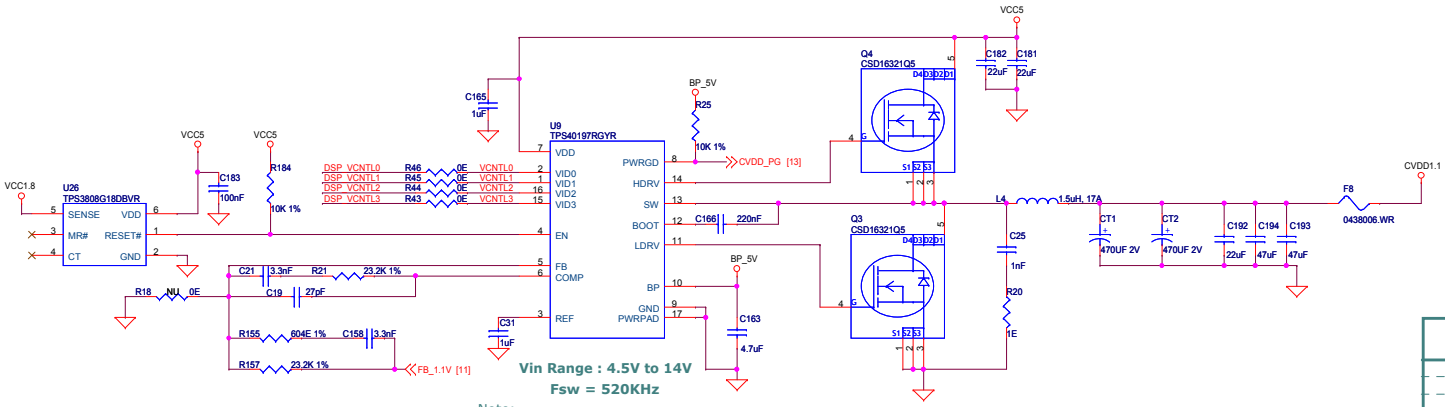
C6474 : Reset, NMI, I2C, Smart Reflex



Configuration EEPROM
I2C Address : 0x50



I2C Level Translator



CVDD @ 6A

Vin Range : 4.5V to 14V
Fsw = 520KHz

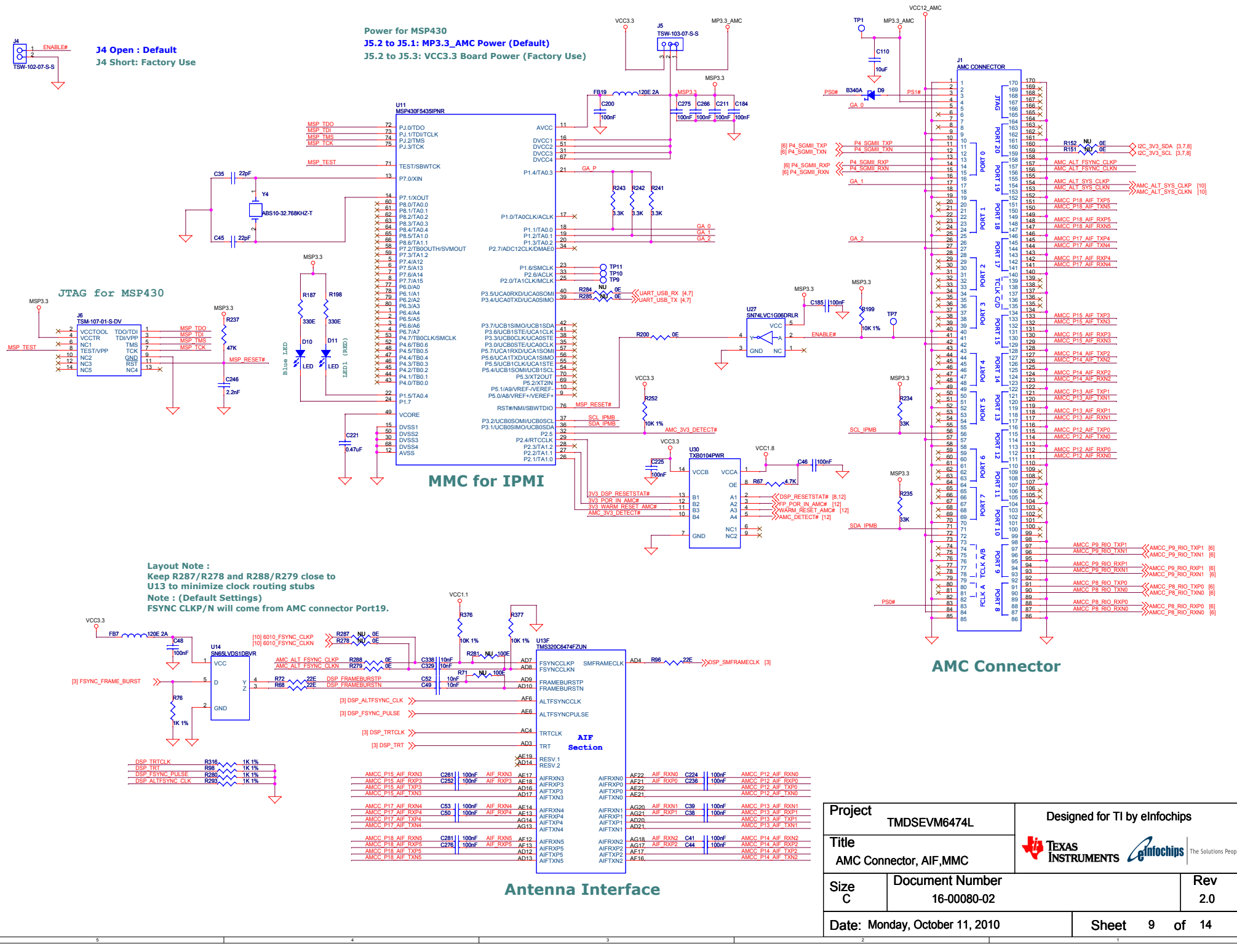
Note:
U9 will be enabled 20mS after VCC1.8 is up.

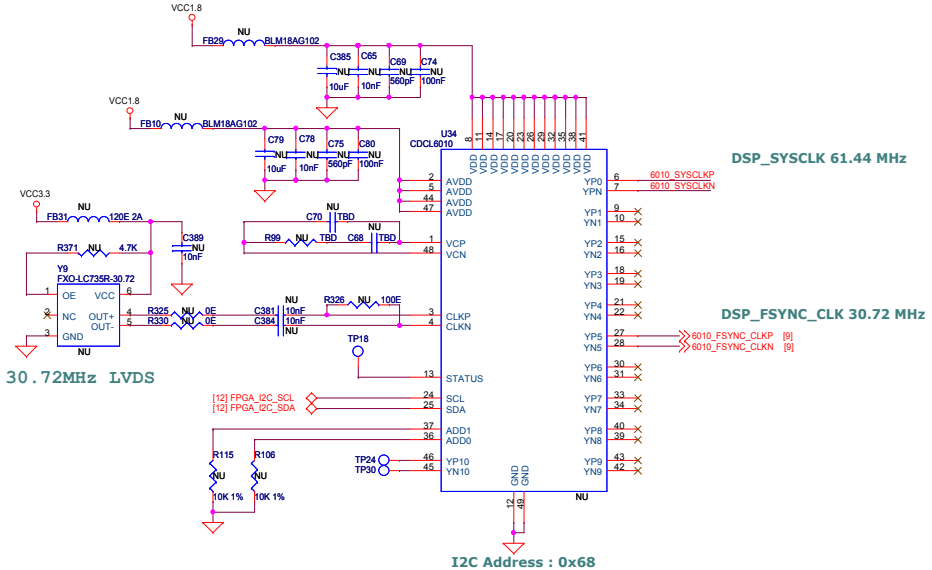
Smart Reflex Power Supply

VNCTL Pin Mapping

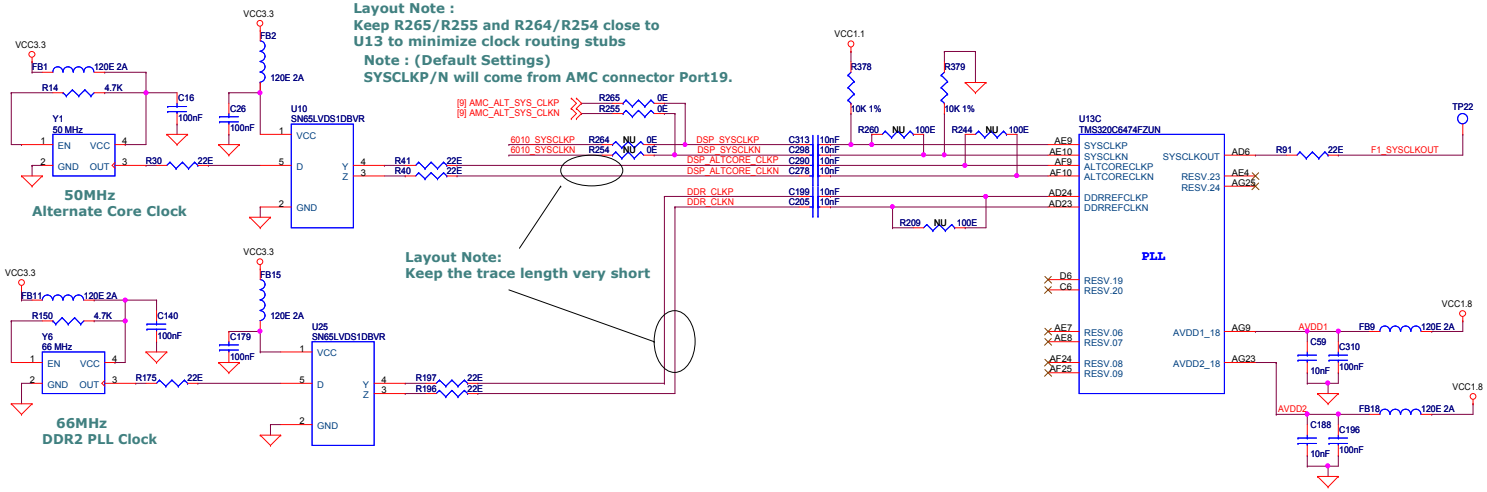
VCNTL[3:0]	CVDD VALUE (Volt)
0000 (0)	0.901
0001 (1)	0.920
0010 (2)	0.940
0011 (3)	0.960
0100 (4)	0.980
0101 (5)	1.000
0110 (6)	1.020
0111 (7)	1.040
1000 (8)	1.060
1001 (9)	1.080
1010 (10)	1.100
1011 (11)	1.120
1100 (12)	1.140
1101 (13)	1.160
1110 (14)	1.180
1111 (15)	1.200

Project: TMDSEVM6474L	Designed for TI by eInfochips	
Title: RST#, E2PROM,SMRT REFLEX		
Size: C	Document Number: 16-00080-02	Rev: 2.0
Date: Monday, October 11, 2010	Sheet 8 of 14	

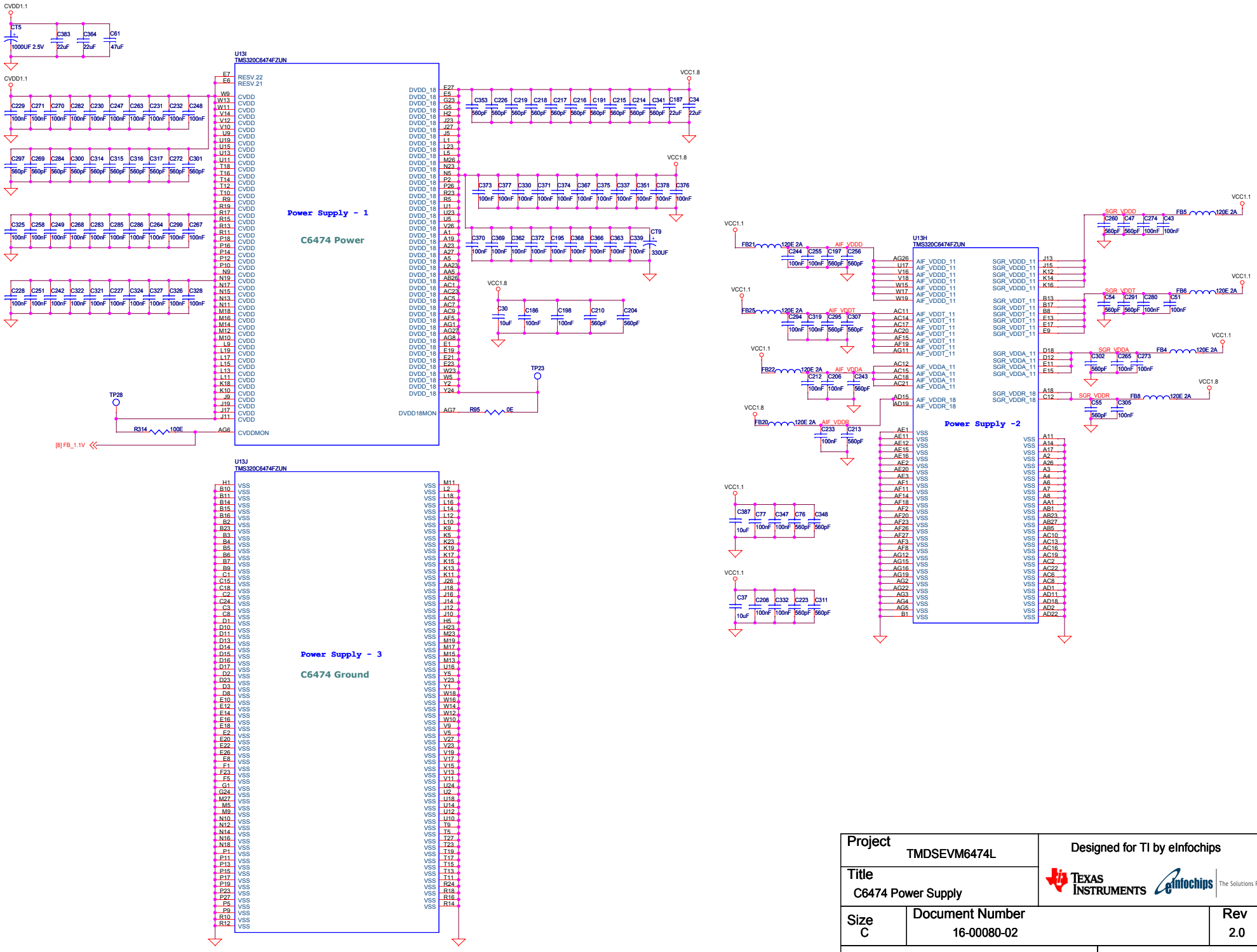

J4 Open : Default
J4 Short: Factory Use
Power for MSP430
J5.2 to J5.1: MP3.3_AMC Power (Default)
J5.2 to J5.3: VCC3.3 Board Power (Factory Use)
JTAG for MSP430
MMC for IPMI
AMC Connector
Layout Note :
Keep R287/R278 and R288/R279 close to
U13 to minimize clock routing stubs
Note : (Default Settings)
FSYNC CLKP/N will come from AMC connector Port19.
Antenna Interface
AIF Section
Project
TMDSEVM6474L
Designed for TI by eInfochips
Title
AMC Connector, AIF,MMC
Size
C
Document Number
16-00080-02
Rev
2.0
Date: Monday, October 11, 2010
Sheet 9 of 14

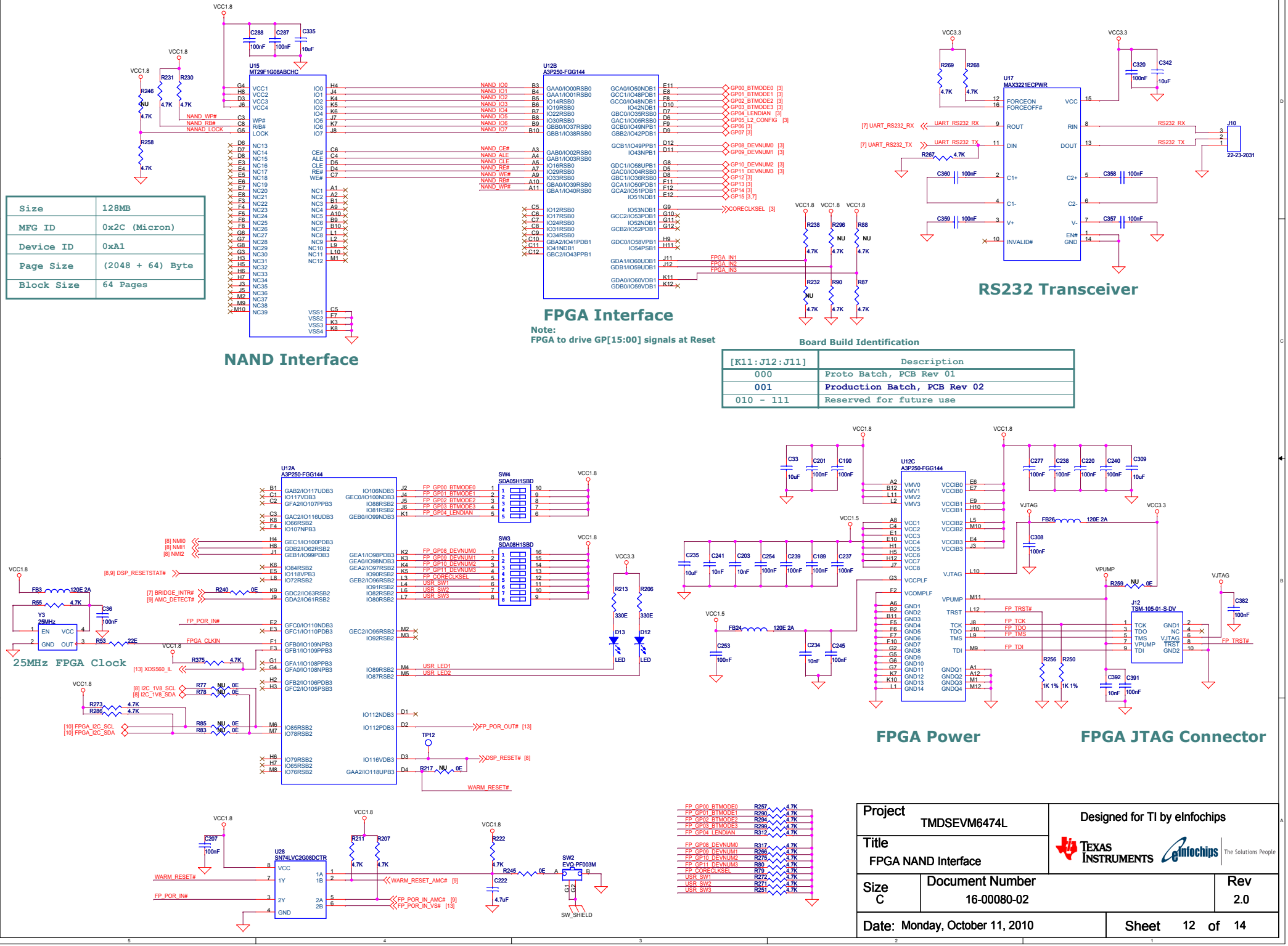


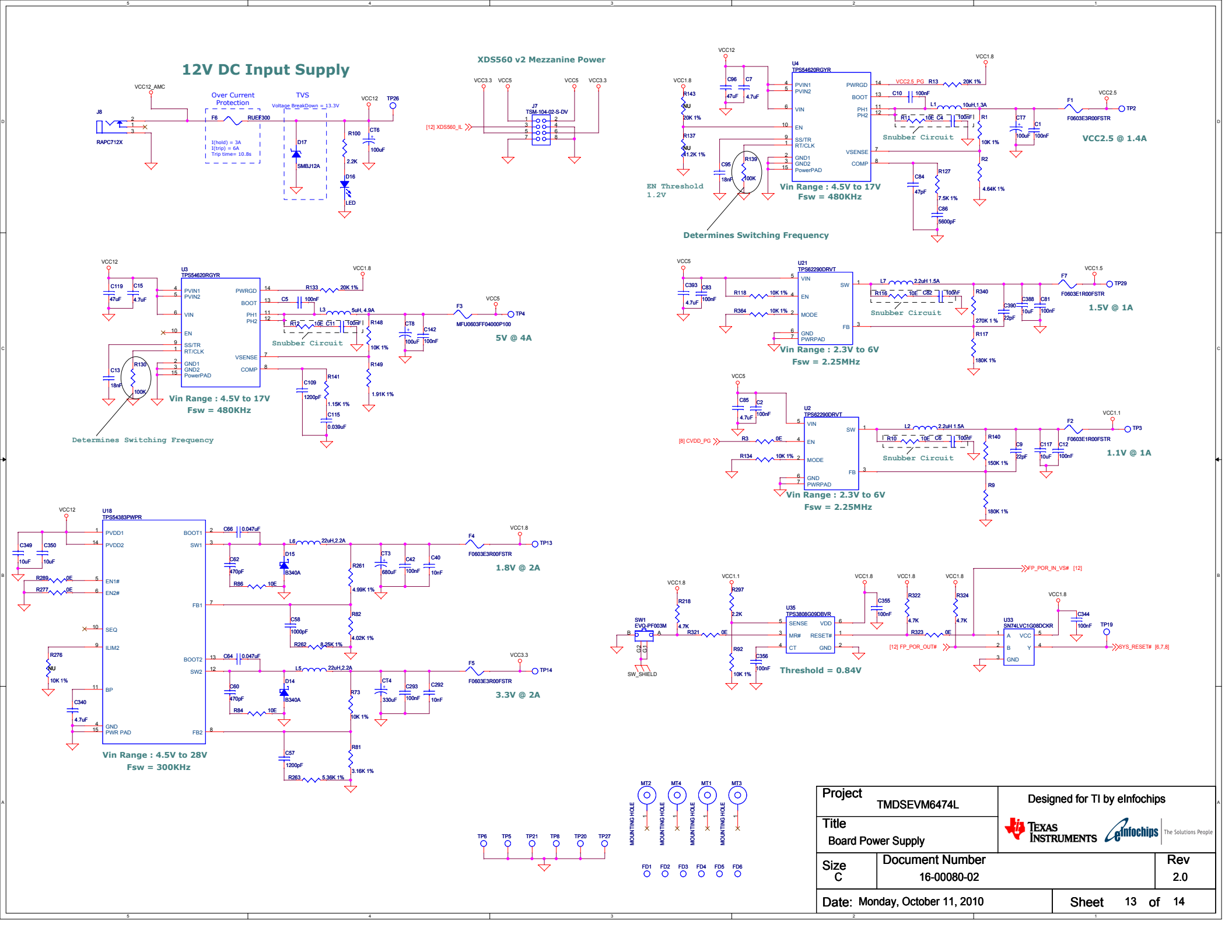
Clock Multiplier, Divider, Jitter Cleaner, Buffer



Project: TMDSEVM6474L		Designed for TI by eInfochips
Title: Clock Management		
Size: C	Document Number: 16-00080-02	Rev: 2.0
Date: Monday, October 11, 2010	Sheet 10 of 14	


U13I
TMS320C6474FZUN
Power Supply - 1
C6474 Power
U13J
TMS320C6474FZUN
Power Supply - 3
C6474 Ground
U13H
TMS320C6474FZUN
Power Supply -2
CVDD1.1
VCC1.8
VCC1.1
TP28
TP23
R314
100E
R95
0E
[8] FB_1.1V
CVDDMON
DVDD18MON
Project
TMDSEVM6474L
Designed for TI by eInfochips
Title
C6474 Power Supply
Size
C
Document Number
16-00080-02
Rev
2.0
Date: Monday, October 11, 2010
Sheet 11 of 14

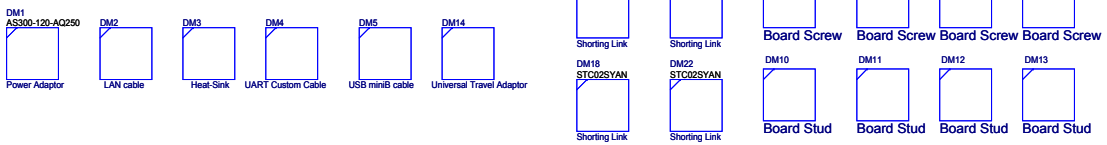

NAND Interface
FPGA Interface
Note:
FPGA to drive GP[15:00] signals at Reset
RS232 Transceiver
Board Build Identification
25MHz FPGA Clock
FPGA Power
FPGA JTAG Connector
Size
128MB
MFG ID
0x2C (Micron)
Device ID
0xA1
Page Size
(2048 + 64) Byte
Block Size
64 Pages
[K11:J12:J11]
Description
000
Proto Batch, PCB Rev 01
001
Production Batch, PCB Rev 02
010 - 111
Reserved for future use
Project
TMDSEVM6474L
Designed for TI by eInfochips
Title
FPGA NAND Interface
Size
C
Document Number
16-00080-02
Rev
2.0
Date: Monday, October 11, 2010
Sheet 12 of 14


12V DC Input Supply
VCC12_AMC
J8
RAPC712X
Over Current Protection
F6
RUEF300
I(hold) = 3A
I(trip) = 6A
Trip time= 10.8s
TVS
Voltage BreakDown = 13.3V
D17
SMBJ12A
R100
2.2K
CT6
100uF
VCC12
TP26
D16
LED
XDS560 v2 Mezzanine Power
VCC3.3
VCC5
J7
TSM-104-02-S-DV
[12] XDS560_IL
U4
TPS54620RGYR
PVIN1
PVIN2
VIN
EN
SS/TR
RT/CLK
GND1
GND2
PowerPAD
PWRGD
BOOT
PH1
PH2
VSENSE
COMP
VCC1.8
R143
DNU
20K 1%
R137
41.2K 1%
C96
47uF
C7
4.7uF
C95
18nF
R139
100K
EN Threshold
1.2V
Determines Switching Frequency
VCC2.5_PG
R13
20K 1%
C10
100nF
L1
10uH,1.3A
R11
10E
C4
100nF
Snubber Circuit
R1
10K 1%
R2
4.64K 1%
C77
100uF
C1
100nF
F1
F0603E3R00FSTR
VCC2.5
TP2
VCC2.5 @ 1.4A
Vin Range : 4.5V to 17V
Fsw = 480KHz
R127
7.5K 1%
C84
47pF
C86
5600pF
U3
TPS54620RGYR
C119
47uF
C15
4.7uF
C13
18nF
R130
100K
R133
20K 1%
C5
100nF
L3
5uH, 4.9A
R12
10E
C11
100nF
R148
10K 1%
R149
1.91K 1%
C109
1200pF
R141
1.15K 1%
C115
0.039uF
CT8
100uF
C142
100nF
F3
MFU0603FF04000P100
VCC5
TP4
5V @ 4A
Snubber Circuit
Vin Range : 4.5V to 17V
Fsw = 480KHz
Determines Switching Frequency
U21
TPS62290DRVT
C393
4.7uF
C83
100nF
R118
10K 1%
R364
10K 1%
L7
2.2uH 1.5A
R116
10E
C82
100nF
R340
270K 1 %
R117
180K 1%
C390
22pF
C388
10uF
C81
100nF
F7
F0603E1R00FSTR
VCC1.5
TP29
1.5V @ 1A
Snubber Circuit
Vin Range : 2.3V to 6V
Fsw = 2.25MHz
U2
TPS62290DRVT
C85
4.7uF
C2
100nF
[8] CVDD_PG
R3
0E
R134
10K 1%
L2
2.2uH 1.5A
R10
10E
C8
100nF
R140
150K 1%
R9
180K 1%
C9
22pF
C117
10uF
C12
100nF
F2
F0603E1R00FSTR
VCC1.1
TP3
1.1V @ 1A
Snubber Circuit
Vin Range : 2.3V to 6V
Fsw = 2.25MHz
U18
TPS54383PWPR
PVDD1
PVDD2
EN1#
EN2#
SEQ
ILIM2
BP
GND
PWR PAD
BOOT1
SW1
FB1
BOOT2
SW2
FB2
C349
10uF
C350
10uF
R289
0E
R277
0E
R276
DNU
10K 1%
C340
4.7uF
C66
0.047uF
C62
470pF
R86
10E
L6
22uH,2.2A
D15
B340A
R261
4.99K 1%
CT3
680uF
C42
100nF
C40
10nF
F4
F0603E3R00FSTR
TP13
1.8V @ 2A
C58
1000pF
R82
4.02K 1%
R262
8.25K 1%
C64
0.047uF
C60
470pF
R84
10E
L5
22uH,2.2A
D14
B340A
R73
10K 1%
CT4
330uF
C293
100nF
C292
10nF
F5
F0603E3R00FSTR
VCC3.3
TP14
3.3V @ 2A
C57
1200pF
R263
5.36K 1%
R81
3.16K 1%
Vin Range : 4.5V to 28V
Fsw = 300KHz
SW1
EVQ-PF003M
SW_SHIELD
R218
4.7K
R321
0E
R297
2.2K
R92
10K 1%
C356
100nF
U35
TPS3808G09DBVR
SENSE
MR#
CT
VDD
RESET#
GND
C355
100nF
R322
4.7K
R323
0E
R324
4.7K
FP_POR_IN_VS# [12]
[12] FP_POR_OUT#
U33
SN74LVC1G08DCKR
A
B
GND
VCC
Y
C344
100nF
TP19
SYS_RESET# [6,7,8]
Threshold = 0.84V
TP6
TP5
TP21
TP8
TP20
TP27
MT2
MT4
MT1
MT3
MOUNTING HOLE
FD1
FD2
FD3
FD4
FD5
FD6
Project
TMDSEVM6474L
Designed for TI by eInfochips
Title
Board Power Supply
TEXAS INSTRUMENTS
eInfochips
The Solutions People
Size
C
Document Number
16-00080-02
Rev
2.0
Date: Monday, October 11, 2010
Sheet 13 of 14

TMDSEVM6474L - REVISION HISTORY

PCB REV.	SCH. REV.	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	0.1	First Draft Created.	23-JUN-2010	eInfochips
	0.2	Updated for Internal / TI review comment	25-JUN-2010	eInfochips
	0.3	- EEPROM added in Ethernet Switch section. - TPS54010 replaced by TPS40197 for smart reflex power supply - Updated for internal / TI review comments.	06-JUL-2010	eInfochips
	0.4	- Voltage supervisor circuit added on VCC1.8 to ensure CVDD11 to be available after VCC1.8. - R485 and R454 are changed to 22E. - U4.C7 grounded by 0E resistor to minimize risk. - Q7 and Q8 parts changed to TI's "CSD16321Q5" as per FAE suggestion	10-JUL-2010	eInfochips
	0.5	- Change Bulk capacitors of Smart Reflex power supply from 470uF to 1000uF - Replace 3 bulk capacitors of 330uF and 220uF with single 1000uF capacitor - Take feedback from CVDD Monitor pin of U4 for Smart Reflex sense input. - Change resistor devider value for U3,U14,U5 and U41. - Add PU and PD option to LOCK pin of NAND flash.(Default : PD) - 0E/0603 added on FB line of U8(Smart Reflex)	15-JUL-2010	eInfochips
	0.6	- 0E/0603 added on FB line of U8(Smart Reflex) - Changed few components values in smart reflex as per the latest reference design provided by local TI FAE.	20-JUL-2010	eInfochips
	0.7	- Removed R519 (1E) Resistor due to space constraint. - Added PD to CS line of SPI EEPROM connected to 88E6122 - Keep provision for 3-bits board identification instead of 2-bits - SGMII connection between 88E6122 and AMC edge connector are corrected after internal review. - Swap AMC_ALT_SYS_CLKP/N and AMC_ALT_FSYNC_CLKP/N at AMC edge connector as per the AMC Rev 2.0 short Form specification - Updated Stack-up on Cover Page	04-Aug-2010	eInfochips
	Issue 1.0	- Released for PCB Fabrication -- Proto Boards	06-Aug-2010	eInfochips
2.0	Issue 2.0	Production Batch Release - U32 part number changed to TXS0108EPWR - Board Identification # changed to 001 from 000 - R310 (4.7K) made NU, 4.7K PD added on EM_TRST#, 1K PD added on TRST# net - 1M bias resistor added on Y2.1 pin - AMC_DETECT# signal provided to FPGA by through a level translator chip U30 - Pull up added on XDS560_IL net - 10K PU and PD added on SYSCLK P/N and FSYNCCLK P/N pins of C6474 - CT6 part # changed	11-OCT-2010	eInfochips

Dummy Components



Project: TMDSEVM6474L		Designed for TI by eInfochips
Title: Revision History		
Size: C	Document Number: 16-00080-02	Rev: 2.0
Date: Monday, October 11, 2010	Sheet 14 of 14	