einfochips An Arrow Company | The Solutions People

Physical Design of a 7nm based Superfast Programmable Ethernet Switch

World's first programmable chip Size >500mm2 and frequency >1GHz

Targeted for Hyperscale data centers

Processing above 10 TBPS

RTL to GDSII at 7nm Technology node

Case Study

Executive Summary

Today, internet networks have grown exponentially, at a rate that was unimaginable a few years ago. With increasing requirements of cloud computing, sophisticated network connections, proliferation of artificial intelligence and machine learning technology, and overall global adoption of distributed applications, the demand for improved reliability, visibility, security, AI and ML workloads, and storage across networking architectures has also increased. To address this demand, our client, a US-based startup, has built a fully programmable networking ASIC using Protocol Independent Switch Architecture (PISA).

The client was planning to design a second generation chip, with full programmability above 10 Tbps packet processing speed. Based on 7nm technology node, the chip aimed to deliver double the performance compared to its first generation chip, making it an ideal choice for cloud, hyperscale data centers and service provider networks. To accomplish this ambitious goal, the client was looking for an engineering partner with expertise in physical layout of chips at 7nm technology.

Client Profile

The client is a US-based start-up that focuses on the design and manufacture of silicon, systems, and software for programmable network switches. Targeting the data center market with a product that will revolutionize data center infrastructure, the client is pushing the boundaries of ASIC.

Business Challenge

The clients' second-generation chip targeted 2X performance improvement over first-generation and was expected to be groundbreaking product as one of the first fully programmable networking ASICs. The primary challenges was that the tool flow and methodology was not mature and well defined for the newer technology node (7nm).

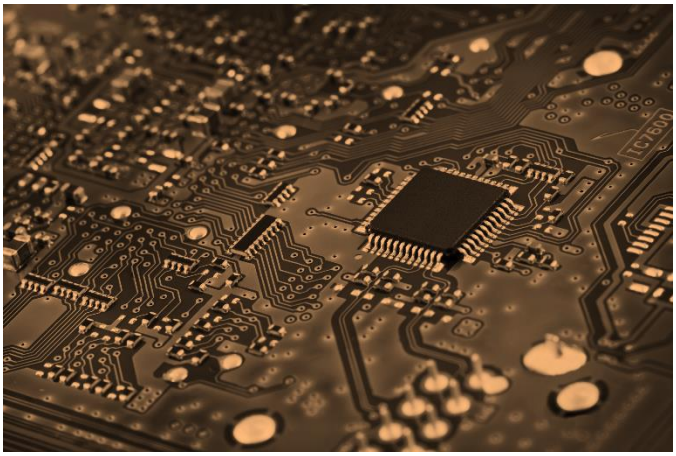
Solution

Leveraging strong experience in physical design methodologies, eInfochips helped the client to close all the blocks and clusters assigned within stipulated time frame for tape out of the ASIC.

Key highlights:

- Netlist to GDSII implementation for 30+ blocks
- One of the blocks had 14 million instances (50+ million gate count)
- Block Closure: Block level Floorplan, Power plan, Placement & Routing , Clock tree synthesis , STA and Physical Verification
- Helped the methodology team to stabilize and improve QoR through ICC based flow
- Implemented Semi custom CTS for blocks
- Full chip PnR, DRV-LVS closure, RDL Routing, Bump and power insertion at top level

EDA tools: Genus, Innovus, Tempus, Voltus, Quantus, Calibre



Benefits

- With a strong focus on die size optimization and performance, eInfochips improved chip frequency above 1GHz with 70% of chip area utilization
- Together, we have completed the tape-out of the next-gen data center ASIC with higher throughput, performance and programmability

About eInfochips

eInfochips, an Arrow company, is a leading global provider of product engineering and semiconductor design services. With over 500+ products developed and 40M+ deployments in 140 countries, eInfochips continues to fuel technological innovations in multiple verticals. The company's service offerings include digital transformation and connected IoT solutions across various cloud platforms, including AWS and Azure.

USA HQ 2025 Gateway Place, Suite #270, San Jose, CA 95110.

INDIA HQ 11 A/B Chandra Colony, CG Road, Ellisbridge, Ahmedabad 380 006.

www.einfochips.com | marketing@einfochips.com