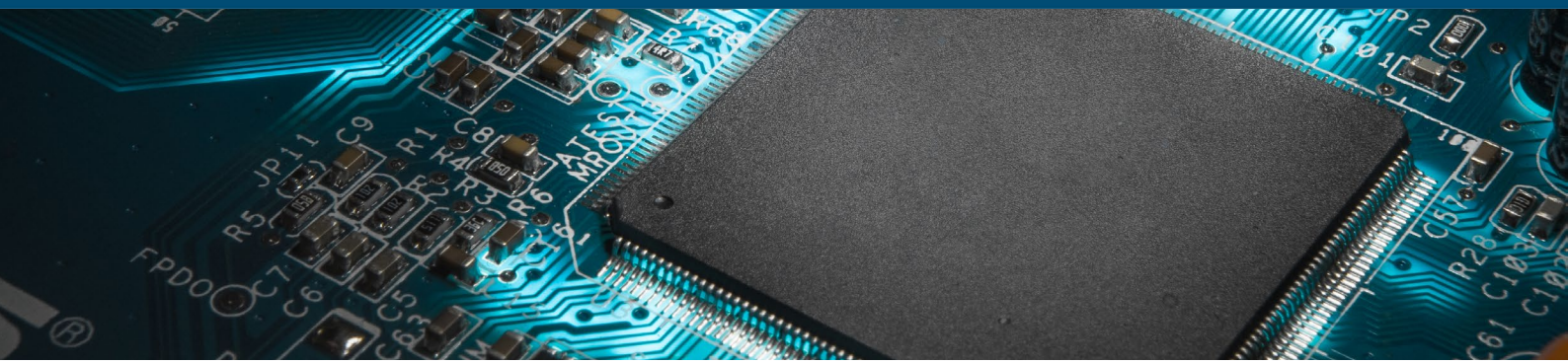
OTL
Verification IP



Overview:

eInfochips's OTL Verification IP Product is the comprehensive OTL interface protocol validation solution. ITU-T recommendation G.709 annexure C defines OTL interface mechanism by which OTU4 and OTU3 signals can be carried for short-reach client side applications. OTU4 signals can be carried over 10 parallel lanes, which are formed by bit multiplexing of 20 logical lanes. OTU3 signals can be carried over 4 parallel lanes.

The recommendation specifies the way in which OTU4 or OTU3 frames are first divided into 1020 groups of 16 bytes and sent on parallel lanes. Before doing that, the transmitter follows various rules related with lane rotation.

The recommendation also specified the role of receiver, which is responsible for framing, multi- lane alignment and deskews of incoming data before forming OTU4 and OTU3 frames.

OTL Verification IP developed at eInfochips can be used to verify a transmitter or receiver functionality for both OTU4 and OTU3 interfaces. It is developed in System Verilog HVL and using UVM as verification methodology. The use of methodology allows the single VIP instance be configured as either transmitter or receiver thereby easing the work of VIP integration in testbench. This VIP can be configured as per the user requirements and various hooks provided with it allows user to control behaviour of various VIP components completely while testing its own application.

Architecture:

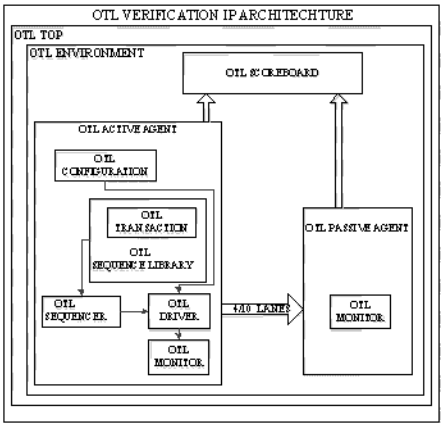


Figure 1: OTL VIP Architecture

Figure 1 shows overall architecture of OTL Verification IP. OTL VIP is developed using System Verilog, the unified language for Design & Verification and UVM reusable verification methodology.

OTL VIP can be used as active, passive or passive only monitor to verify Networking based design having OTL interface in different scenarios.

OTL VIP comprises of following major elements.

- Driver
- Monitor
- Generator : Sequences & Sequencer
- Protocol Checkers
- APIs
- Coverage Capability
- Assertions
- Configuration
- Report Generator

Application:

OTL Verification IP provides flexible and efficient mechanism to verify OTL interface protocol for any design using various supported modes. There are three modes, in which this VIP can be utilized to verify OTL protocol functionality in different way.

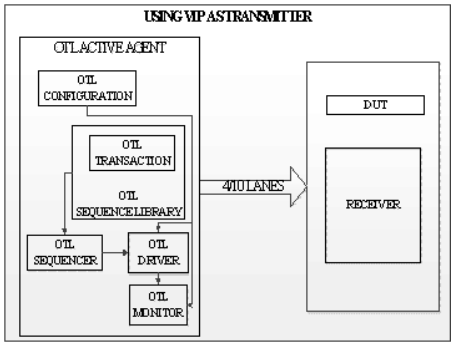


Figure 2: OTL VIP to OTL DUT

Figure 2 shows OTL VIP as an active transmitter to pump OTN traffic to OTN DUT. In this mode, it can verify OTL functionality of the DUT as well as it can generate all types of OTL error and stress scenarios to test DUT's capability to handle complex OTL protocol scenarios.

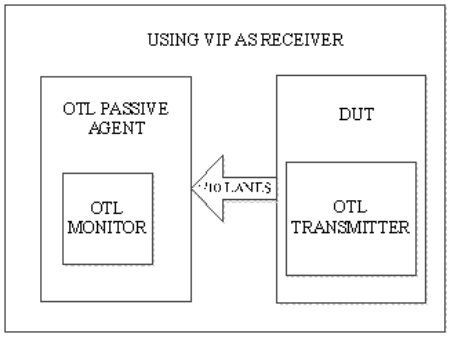
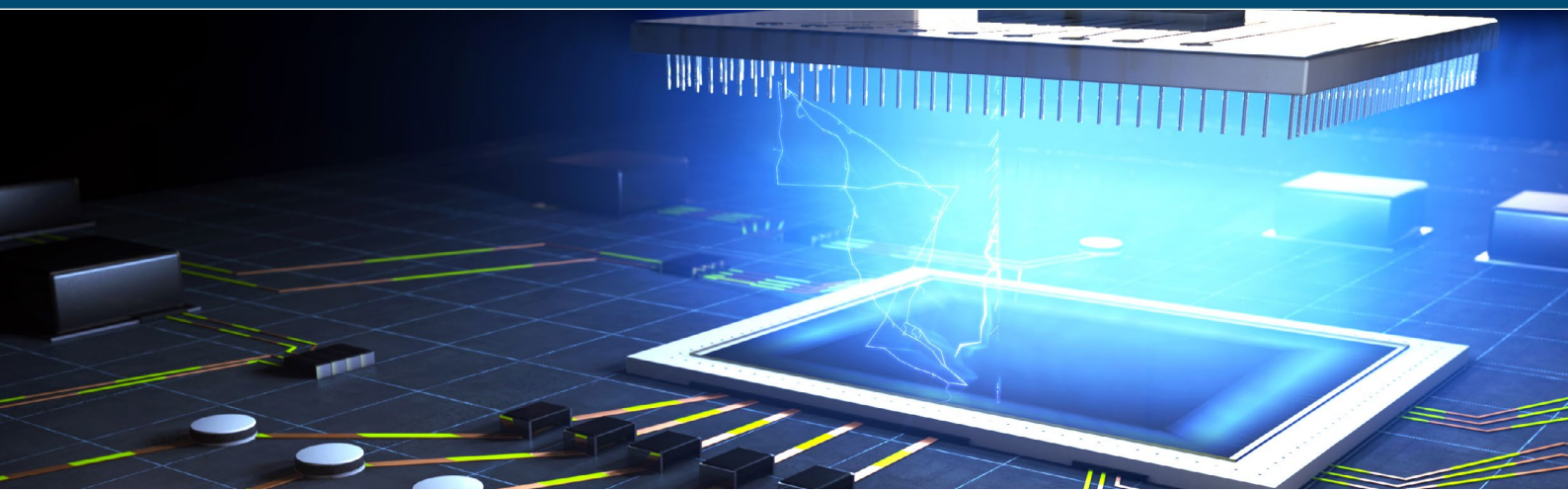


Figure 3: OTL DUT to OTL VIP

Figure 3 shows another mode of OTL VIP. Here OTL VIP is receiving OTN traffic from OTL transmitter DUT. In this mode, OTL VIP is used in passive mode and has capability to verify OTL transmitter DUT's capability



thoroughly. In this configuration, if DUT generates any OTL protocol errors or it behaves unexpectedly, then it can be easily caught by OTL VIP activing as a receiver.

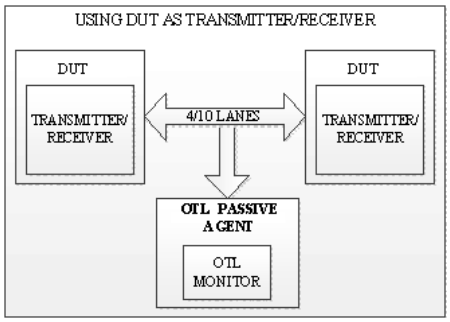


Figure 4: OTL VIP as a passive monitor

Finally, Figure 4 shows OTL VIP acting as a passive monitor when two OTL DUTs are interacting with each other.

Major Product Features:

Transmitter features:

- OTUk Frame division in 16 bytes chunk (k = 3,4).
- Round robin distribution of OTUk frame (k = 3,4).
- Lane rotation using MFAS in case of 40G.
- LLM generation in case of 100G.
- Bit multiplexing of logical lanes in case of 100G
- User Configurable Support For Scrambling
- Generation of Fixed, Incremental or random data.
- Support to generate PRBS data.
- Flexibility to map any logical lanes to any physical lane.
- Error injection in Frame Alignment Sequence (FAS) and Multi Frame Alignment Sequence (MFAS).
- Support for Frame Slip generation.
- Error injection in Logical Lane Marker(LLM) in case of 100G
- 10^(-3) Bit Error rate generation
- User Configurable Support For defect and alarm thresholds

Receivers features:

- OTUk Framing on each lanes(k = 3,4)
- Lane identifier recovery
- Multilane alignment
- OTU3 mode de-skew capacity
- OTU4 mode de-skew capacity
- Receiver Bit Error Rate tolerance before error correction
- Framing Alignment State machine error recovery
- Multilane alignment state machine error recovery
- LOFLANE defect generation per lane
- OOFLANE defect generation per lane
- Deskew Fail defect generation
- OLA defect generation per lane
- LOR defect generation per lane
- User configurable support for Descrambling
- User Configurable Support For defect and alarm thresholds

Extended Capabilities:

- Fully compliant to UVM Methodology – UVM1.1.
- Supported Simulator VCS E-2011-03.
- Supports Directed, Constrain Random and Fully Random stimulus generation.
- Supports generic TLM interface for layered sequences support.
- Supports variety of Error Injection via sequences/call-backs and supports other protocol specific errors.
- Supports full OTL3.4 and OTL4.10 protocols.
- Built-in protocol checkers for OTL interface.
- Supports Functional Coverage collection.
- Supports flexibility to use VIP in IP as well as SoC verification.
- Support for directed, constrained and random testing.
- Support for Data Integrity Check.
- Support for automated defect and alarms checks.

Deliverables:

- OTL VIP System-Verilog Source Code.
- User Guide and Release Notes.
- Test cases mentioned in the Test Plan along with the list of Sanity Test cases
- Test Plan + Coverage Plan
- Various prototype examples on topological usage of active, passive or passive monitor.
- Sample Verification Environment.or passive monitor.
- Sample Verification Environment.