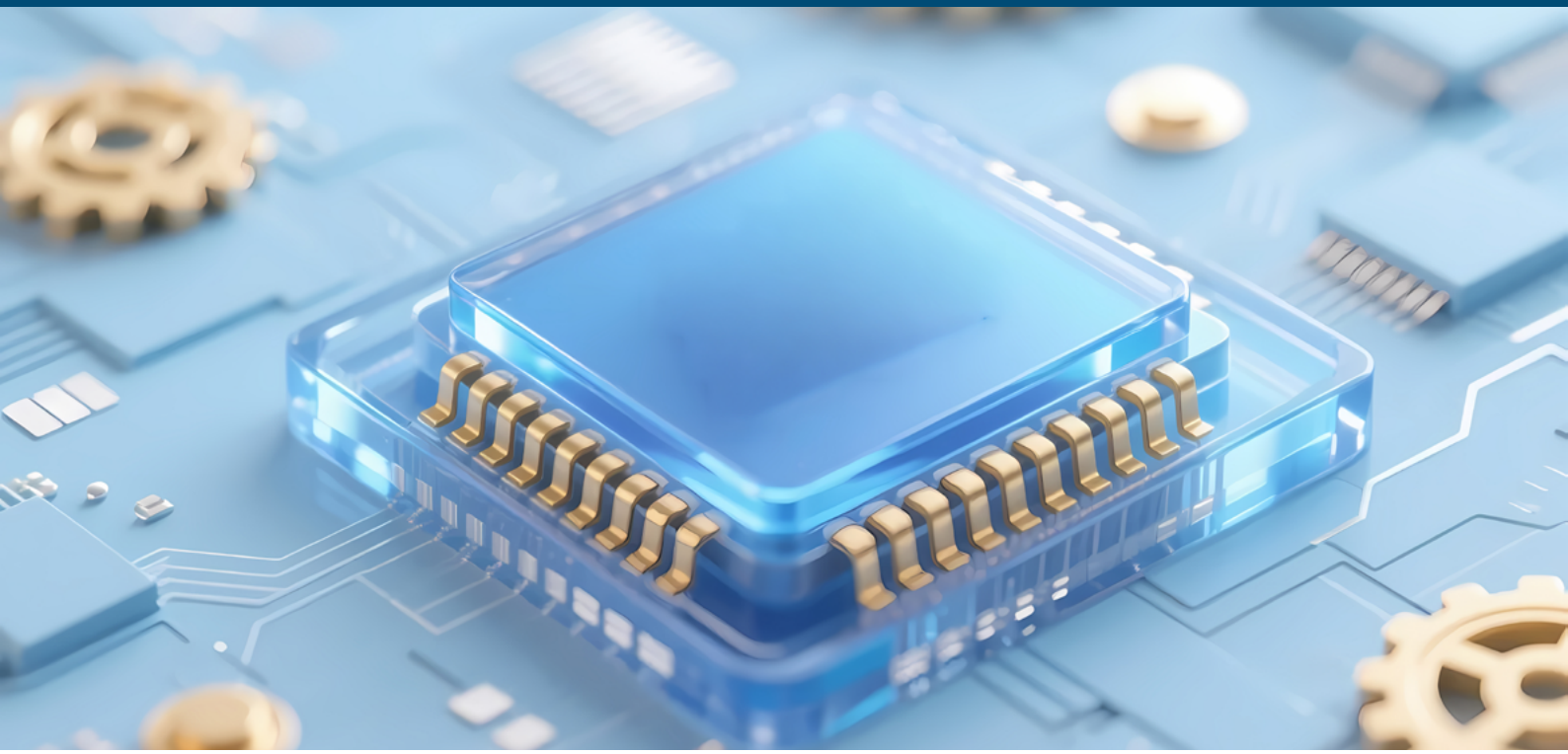
HIGH SIDE CHARGE PUMP MINUS 5V LDO



About eInfochips

eInfochips is a product engineering and semiconductor design services company offering ASIC/SoC design, Analog & Mixed- Signal IP development, FPGA design, and embedded engineering services across multiple industry segments.

eInfochips provides silicon-proven Analog IPs and custom design solutions for power management, data conversion, connectivity, and mixed-signal applications. The company enables customers to accelerate chip development and deliver high-performance, power-efficient semiconductor products.

eInfochips Advantages

- **30** Years of experience in system design
- **17** Design centres worldwide
- **400+** Tapeouts
- **100M+** Product deployments across globe
- **180nm to 18A** expertise

eInfochips A3ACPNLDON5V High Side Charge Pump Minus 5V LDO

The A3ACPNLDON5V High-Side Charge Pump – 5 V LDO (HSCP-LDO5N) is a linear regulator that derives its input from the Boost Converter output and provides a regulated output approximately 5 V below the boosted supply. With a Boost input range of 19 V to 47 V, the regulator provides an output range of 13 V to 41 V.

The regulator supplies the bias rails for the high-side sense amplifiers and the low-side output sense amplifier. An NMOS pass device is used to provide improved power-supply noise rejection and a clean supply rail for accurate sensing.

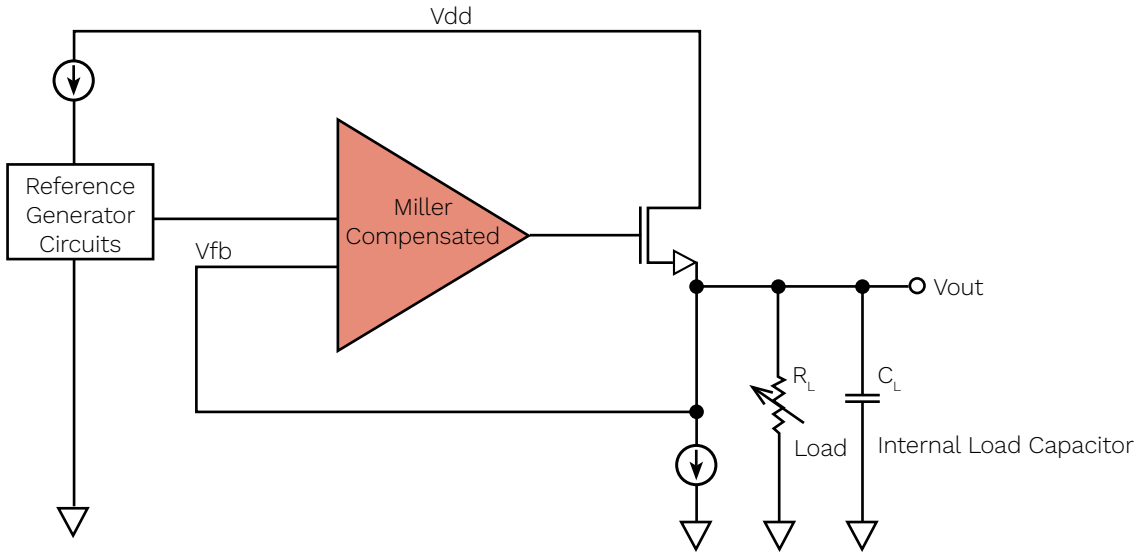
The regulator supports a 5 mA nominal DC load and maintains stable operation across the specified load and operating conditions. Pre-layout and post-layout DC, AC/stability, and transient simulations were performed across TT, FF, and SS process corners, at –40°C, 27°C, and 150°C, and for Boost input voltages of 19 V and 47 V.

Bias supply for high-side current-sense amplifiers (3 channels)

Bias supply for the low-side output sense amplifier

Precision current-sense signal chains in motor-drive and power-stage ICs

Noise-sensitive analog bias rails referenced to a boosted supply



Features

- Generates a regulated supply of VBOOST – 5 V from the Boost-converter output rail (19 V– 47 V input → 13 V– 41 V output)
- NMOS pass-transistor topology for high power-supply rejection and low output noise
- Delivers 5 mA constant DC load current
- **Supply voltage range:** 15 V to 16 V (regulator core); Boost input range 19 V–47 V
- Output voltage shows no measurable shift from no-load to full load across all corners (excellent load regulation)
- **Post-layout DC loop gain:** 104.84 dB to 113.05 dB across TT/FF/SS, –40°C to +150°C, 19 V–47 V
- **Post-layout unity-gain bandwidth:** 182.6 kHz to 688.0 kHz across all corners and load conditions
- **Post-layout phase margin:** 64.2° (worst case, TT/27°C/19V/nos-load) to 101.8°
- **Post-layout gain margin:** 12.7 dB to 28.1 dB across all corners
- **Post-layout PSRR @ 1 MHz:** 16.4 dB to 20.6 dB across all corners
- **Operating temperature range:** –40°C to +150°C, verified at TT/FF/SS process corners
- Line- and load-transient response verified across all six process/temperature/voltage corners

DC Simulation Results (Post-Layout)

- **LDO Output Voltage (VOUT):** 13.15 V to 41.26 V
- **Total Current Consumption – No Load:** 28.3 µA to 47.18 µA
- **Total Current Consumption – Full Load:** 5.028 mA to 5.047 mA
- **Operating Conditions:** VIN = 19 V to 47 V, TA = –40°C to +150°C, TT/FF/SS corners
- **Regulator Core Supply:** 15 V to 16 V

Stability Simulation Results (Pre-Layout)

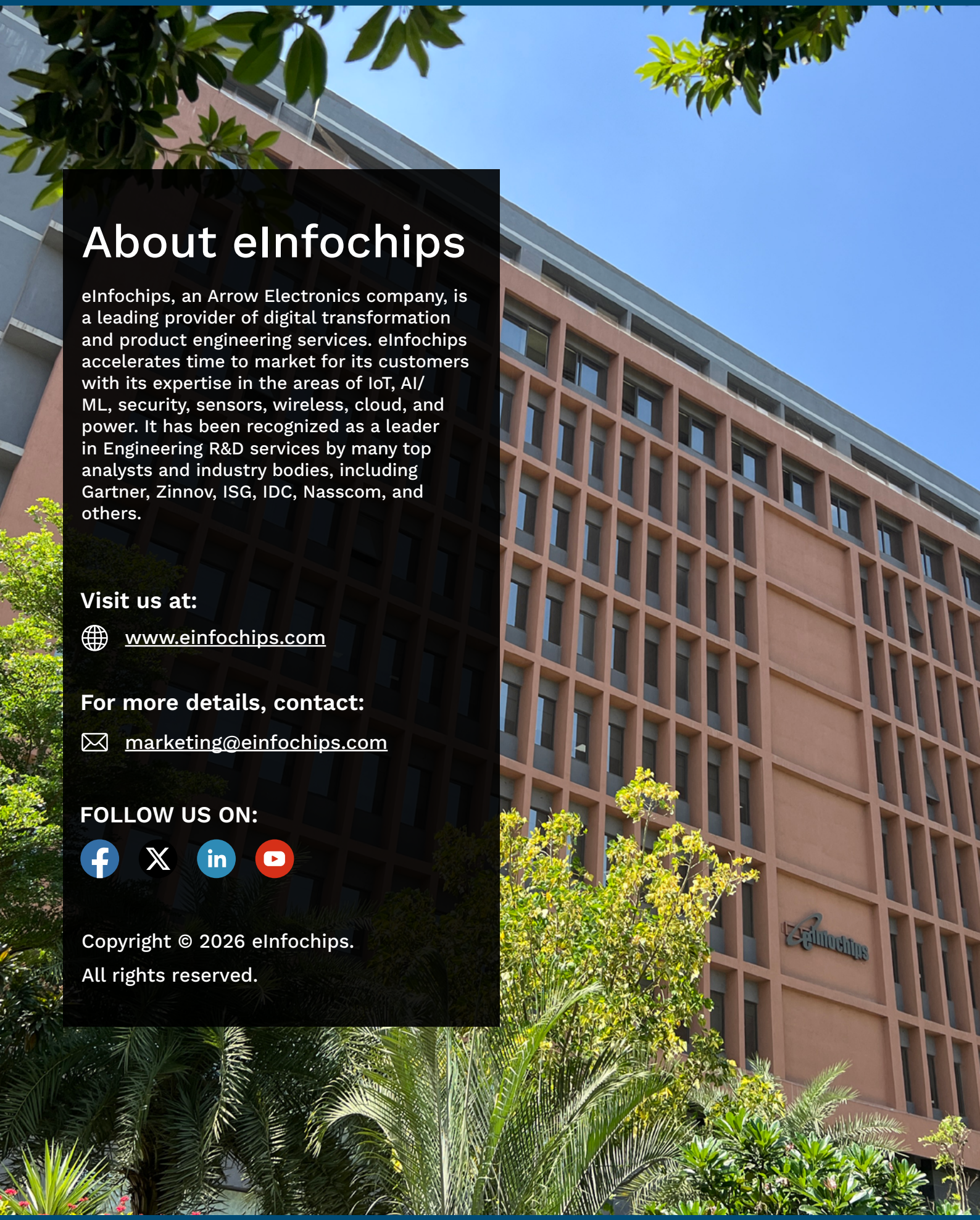
- **Phase Margin:** 74.35° to 110.4° (No Load/Full Load)
- **Unity-Gain Bandwidth (UGB):** 185.77 kHz to 673.48 kHz
- **Gain Margin:** 14.10 dB to 27.31 dB
- **Operating Conditions:** VIN = 19 V to 47 V, TA = –40°C to +150°C, TT/FF/SS corners
- **Load Conditions:** No Load to Full Load (5 mA)

Stability Simulation Results (Post-Layout)

- **Phase Margin:** 64.23° to 101.75° (No Load/Full Load)
- **Unity Gain Bandwidth (UGB):** 182.64 kHz to 687.98 kHz
- **Gain Margin:** 12.74 dB to 28.11 dB
- **Operating Conditions:** VIN = 19 V to 47 V, TA = –40°C to +150°C, TT/FF/SS corners
- **Load Conditions:** No Load to Full Load (5 mA)

AC Simulation Results (Pre and Post Layout)

- **PSR @ 1 MHz – No Load:** Pre-layout 17.72 to 22.73 dB; post-layout 16.41 to 20.60 dB
- **PSR @ 1 MHz – Full Load:** Pre-layout 18.35 to 23.64 dB; post-layout 16.66 to 20.09 dB
- **Operating Conditions:** VIN = 19 V to 47 V, TA = –40°C to +150°C, TT/FF/SS corners
- **Layout Comparison:** Post-layout results maintain positive PSR across all simulated conditions.



About eInfochips

eInfochips, an Arrow Electronics company, is a leading provider of digital transformation and product engineering services. eInfochips accelerates time to market for its customers with its expertise in the areas of IoT, AI/ML, security, sensors, wireless, cloud, and power. It has been recognized as a leader in Engineering R&D services by many top analysts and industry bodies, including Gartner, Zinnov, ISG, IDC, Nasscom, and others.

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