100G Ethernet Verification IP (VIP)

Comprehensive MAC-to-PCS Protocol Validation Solution

Technical Overview

The **100G Ethernet Verification IP (VIP),** developed by **eInfochips – An Arrow Company,** is a robust and high-performance solution for validating 100G Ethernet interfaces across the **MAC-to-PCS datapath,** in compliance with **IEEE 802.3ba** and related standards. It enables **generation, transmission, reception, and monitoring** of various Ethernet MAC frame types—including standard, jumbo, VLAN-tagged, pause, and control frames—ensuring protocol correctness and data integrity across physical lanes.

The VIP provides **complete visibility and control** over the **Physical Coding Sublayer (PCS),** which is responsible for block encoding, lane distribution, alignment, and synchronization before data reaches the PMA/PMD layers. With built-in **error injection and recovery capabilities,** the VIP supports comprehensive validation of encoding accuracy, lane alignment, and system robustness under fault conditions.

Developed in **SystemVerilog** and compliant with the **UVM 1.2** methodology, the VIP can be configured as a **transmitter, receiver, or passive monitor,** making it ideal for verification at the **IP, subsystem, or SoC level.**

MAC Frame Support

The 100G Ethernet VIP supports a broad spectrum of MAC frame types, including:

- Standard Ethernet frames (64–1518 bytes)
- Jumbo frames (up to 9K bytes)
- Pause and control frames
- VLAN-tagged and double-tagged (Q-in-Q) frames
- Custom and error-injected frames for stress testing

These frames are dynamically mapped and distributed over multiple PCS lanes in accordance with the PCS protocol. The VIP supports configurable error injection mechanisms (e.g., sync header corruption, alignment loss, invalid control blocks) to verify system behaviour under fault conditions and validate recovery logic.

Built using System Verilog and compliant with the UVM 1.2 methodology, this VIP offers reusable, modular components and can be instantiated in multiple roles—transmitter, receiver, or passive monitor—making it suitable for IP, subsystem, or SoC-level verification environments.

Its advanced configuration interface, along with built-in protocol checkers, assertions, and functional coverage, ensures that users can simulate, control, and analyse complex Ethernet scenarios efficiently and accurately.

Architecture

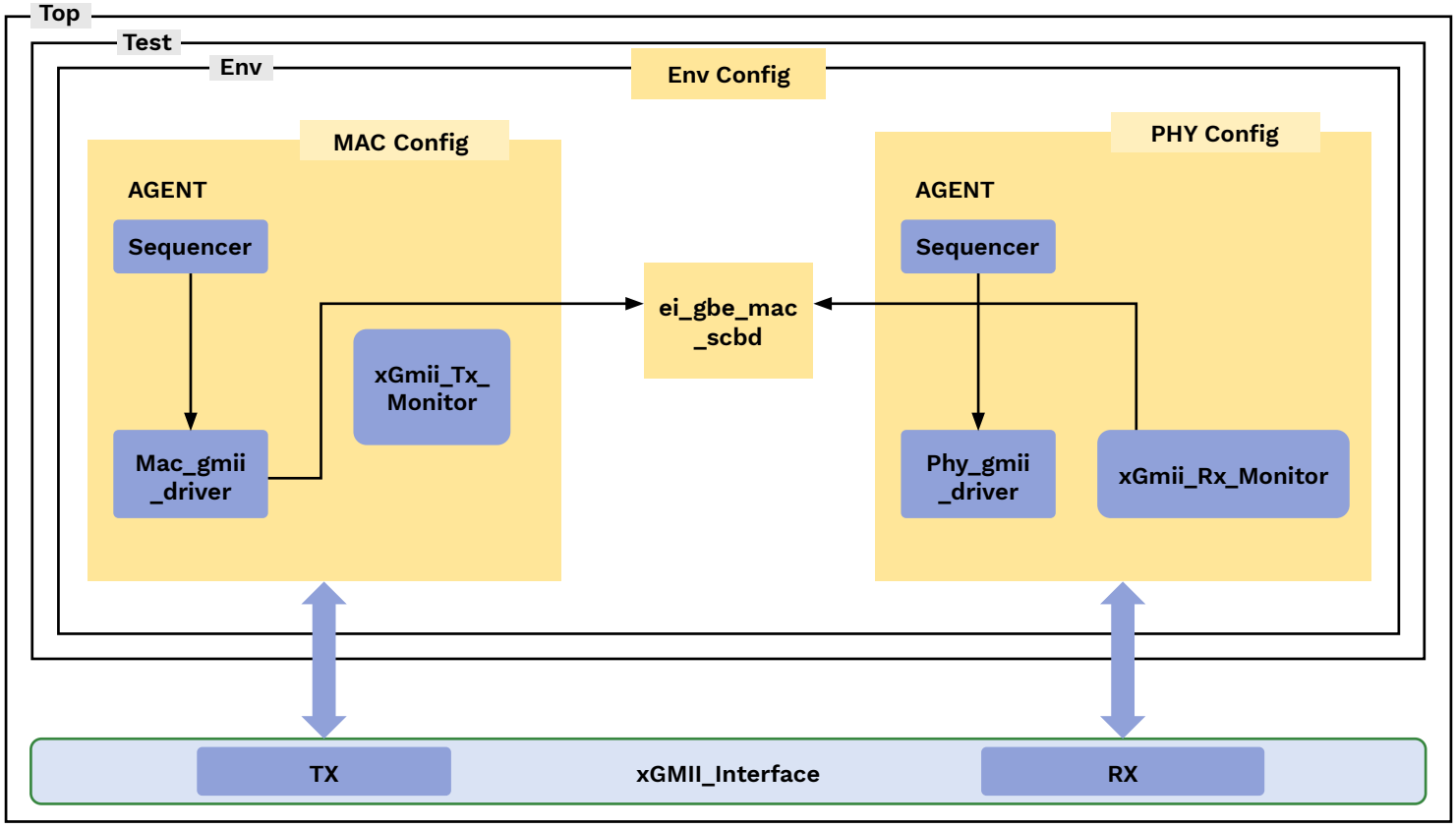

Figure 1: Ethernet VIP 100G Architecture

The 100G Ethernet Verification IP (VIP) is architected to support comprehensive verification of MAC-to-PCS Datapath as defined in the IEEE 802.3ba standard. It consists of configurable, modular UVM components, allowing reuse and adaptability across various verification environments—IP, subsystem, and SoC level.

Core Components Include:

- **Sequencer & Sequence Library:** Generates randomized and directed MAC frame traffic.
- **Driver (Transmitter):** Encodes and transmits MAC frames according to 64b/66b PCS encoding, lane distribution, and synchronization schemes.
- **Monitor (Receiver):** Captures and analyses PCS-aligned data, validates protocol correctness and reconstructs MAC frames.
- **Scoreboard & Reference Models:** Provide self-checking mechanism for data integrity, protocol behaviour, and alignment verification.
- **Error Injection Engine:** Enables insertion of protocol faults such as sync header corruption, alignment loss, disparity violations.
- **Configuration & Control Interface:** Allows full customization of lane parameters, traffic profile, injection modes, and protocol feature enablement.
- **Assertions & Coverage Collectors:** Built-in protocol checks and functional coverage enable metric-driven closure.

This layered structure allows the VIP to function in transmitter, receiver, or passive monitoring mode, making it highly adaptable for simulation of point-to-point and system-level Ethernet topologies.

Transmitter Architecture

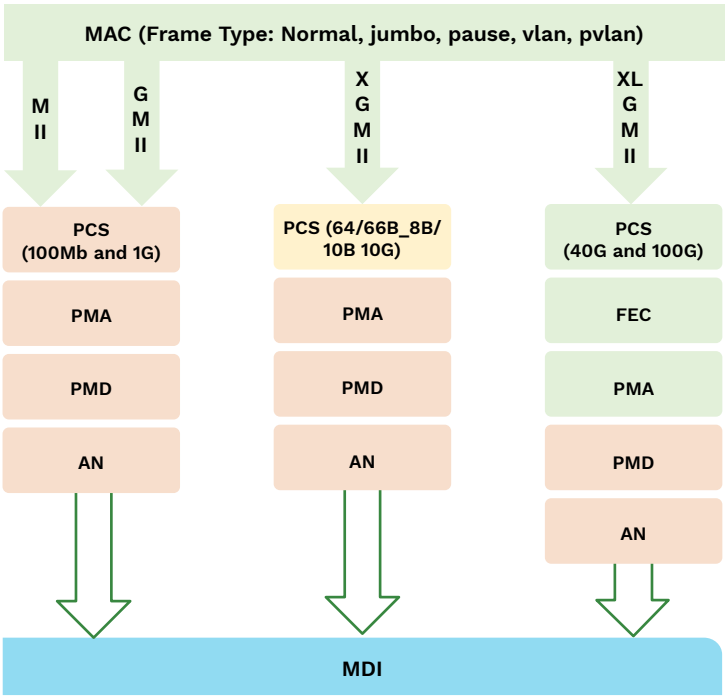

Figure 2: MAC to PHY

Receiver Architecture

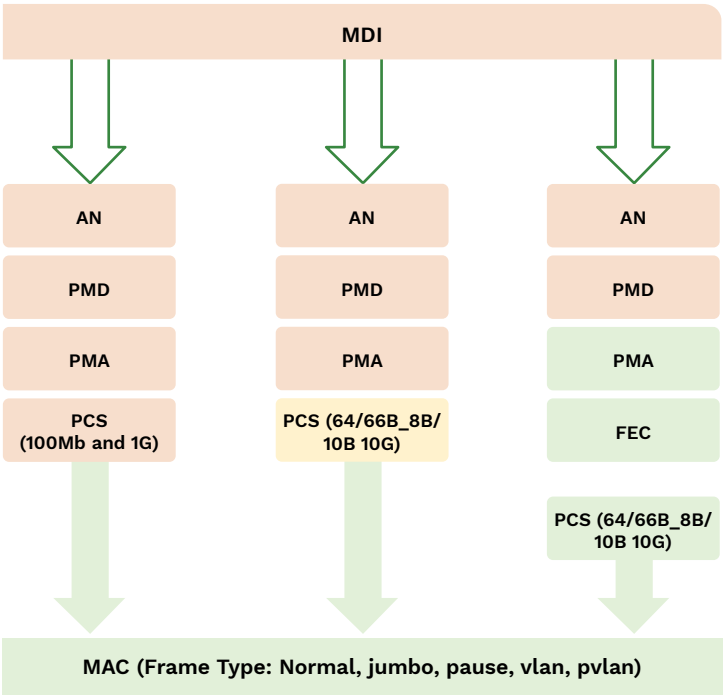

Figure 3: PHY to MAC

The **Transmitter (Driver)** component is responsible for generating valid 100G Ethernet PCS-compliant output from MAC-level Ethernet frames.

Key Functional Blocks:

- **MAC Frame Generator:** Generates standard, jumbo, VLAN-tagged, pause, and custom frames.
- **64b/66b Encoder:** Converts data into PCS blocks with proper sync headers and control blocks.
- **Lane Distribution Engine:** Maps encoded blocks across 20 PCS logical lanes and multiplexes them over 10 physical lanes.
- **Scrambler:** Applies self-synchronizing scrambling to enhance spectral characteristics.
- **Alignment Marker Inserter:** Periodically inserts alignment markers for downstream reassembly.
- **Error Injection Unit:** Supports fault scenarios such as:
  - Invalid sync headers
  - Lane misalignment
  - Block disparity errors
  - Lane skew beyond tolerance
- **User Controls:** Programmable lane count, skew parameters, scrambling enable/disable, inter-frame gaps, and burst configurations.

The transmitter supports flexible stimulus generation, including fully random, constrained random, and directed sequences for edge-case validation.

The **Receiver (Monitor)** component passively observes and reconstructs transmitted Ethernet frames, checking PCS layer compliance.

Key Functional Blocks:

- **Lane Deskew and Synchronization Unit:** Realigns skewed physical lanes into properly ordered PCS blocks.
- **64b/66b Decoder:** Extracts data/control blocks and validates sync headers and encoding.
- **Descrambler:** Reconstructs original MAC frame data post descrambling.
- **Alignment Marker Processor:** Ensures lane alignment and reassembly of the original data stream.
- **Error Detection Engine:** Identifies:
  - Sync header errors
  - Misaligned or out-of-order lanes
  - Disparity violations
  - CRC and block parity mismatches
- **Protocol Checker & Scoreboard Interface:** Compares output with expected reference model behavior, flags protocol violations.
- **Coverage Collection & Assertions:** Tracks protocol coverage metrics such as block types, frame types, and alignment events.

The receiver provides exhaustive visibility into MAC-to-PCS behavior and is essential for functional coverage closure and post-silicon validation planning.

Major Product Features:

- Fully compliant with IEEE 802.3ba 100G Ethernet specification
- Supports 64b/66b encoding and decoding
- Validates PCS Lane distribution, alignment, and deskew logic
- 10-lane PCS interface support (Clause 82 compliant)
- Verifies IDLE, Start, Terminate, Control, and Error block behavior
- Supports transmission and reception of:
  - Standard Ethernet frames (64–1518 bytes)
  - Jumbo frames (up to 9K bytes)
  - VLAN-tagged and double-tagged (Q-in-Q) frames
  - Pause frames and Control frames
  - Custom and error-injected MAC frames
- Validates Synchronous Scrambler/Descrambler logic
- Simulates Elastic Buffer and Lane Alignment FIFO behavior
- Configurable PCS Lane skew simulation with per-lane delay
- Supports Bit Slip and Frame Slip logic validation
- Supports Burst mode testing with configurable max/min burst lengths
- Enables Bit Error Rate (BER) injection per PCS lane
- PCS Sync Header error insertion for stress testing
- Lane Marker generation, checking, and corruption injection
- CRC check and CRC error injection at MAC level
- User-configurable End-of-Packet (EOP) behavior
- PRBS pattern generation support: PRBS9, PRBS23, PRBS31
- Optional support for FEC bypass or error injection scenarios
- Enables Multi-channel and Multi-port validation
- Supports Backpressure and In-band Flow Control conditions
- Built-in Protocol Compliance Checker for MAC-to-PCS interface
- Provides User-configurable PCS block-level error injection
- Configurable Logical-to-Physical lane mapping
- Supports Out-of-order lane testing scenarios
- Supports Real-time error monitoring and fault recovery validation
- UVM 1.2 compliant reusable architecture
- Supports use as Transmitter, Receiver, or Passive Monitor
- Integrated with assertions, coverage, and scoreboarding hooks

Extended Capabilities:

- Fully compliant with **UVM 1.2** methodology
- Supports **Directed, Constrained Random, and Fully Random** stimulus generation
- Generic **TLM interface** for layered sequence integration
  - Built-in support for:
  - Sync Header checkers
  - PCS Alignment FSM testing
  - Encoding/Decoding logic validation
- Custom callback hooks for injecting errors in encoding, alignment, or flow control logic
- Supports **Functional Coverage Collection** for PCS protocol and MAC frame transmission
- Built-in **Assertions and Score boarding Support** for PCS blocks
- Supports integration in **IP, subsystem,** or **SoC-level** testbenches
- Configurable for **active, passive, or passive-monitor** usage
- Suitable for **loopback** and **compliance test environments**

Deliverables

- 100G Ethernet VIP SystemVerilog source code
- UVM-compliant testbench components
- User Guide and Release Notes
- Test Plan and Sanity Test Cases
- Coverage Plan
- Sample Verification Environment
- Sanity test cases for quick bring-up and verification
- Example configurations for active, passive, and mixed topologies

Use Cases

- IP and SoC-level Ethernet MAC/PCS validation
- Stress and robustness testing with fault injection
- Corner-case testing using malformed or out-of-spec MAC frames
- Lane alignment and deskew verification
- PCS encoding/decoding accuracy testing