eInfochips
An Arrow Company

ENRICHING LIVES THROUGH ENGINEERING EXCELLENCE

Case Study

DESIGN AND DEVELOPMENT OF ADVANCED CHIPSETS FOR MOBILE TECHNOLOGIES

Executive Summary

The client, an American based multinational semiconductor and telecommunications company, is a world-leading provider of semiconductors, software, and services related to wireless technology. The company designs and manufactures advanced chipsets for mobile devices and other portable electronics. The client focuses on researching and developing innovations in wireless technology, enabling faster, more reliable, and more efficient communication and computing experiences. The client was developing their next-gen ASIC at the 5nm and 3nm technology nodes, which had stringent PPA (Power, Performance, Area) requirement. The client sought a technology partner with strong expertise in design implementation at lower geometry and tapeout experience with TSMC foundry.

Leveraging a strong technology partnership with the client, eInfochips took responsibility for the physical design and design for testability (DFT) of their next-generation ASICs.

Custom-designed Chips for Specific Mobile Applications

Fabrication with 5nm, 4nm, and 3nm semiconductor process nodes

Improved performance, lower power consumption, and higher efficiency

17+1 Metal Layers, 25+ functional blocks

Performance capabilities upto 1+ GHz

Client

The US-based client is an industry-leading semiconductor and telecom company. The client designs and manufactures advanced chipsets for mobile devices such as smartphones, tablets, and other portable electronics.

Challenge

The client needed a technology partner with expertise in silicon and prior experience in ASIC design and development, physical design, and DFT.

Solution

eInfochips leveraged its expertise in lower geometry designs and TSMC foundry exerts to help with the implementation, including:

- Physical design for Multiple Mobility ASICs at 3nm, 4nm and 5nm.
- Place and Route (PnR)
- Clock Tree Synthesis (CTS) network within the chip for distributing the clock equally among all sequential parts chip simultaneously
- Physical Verification (PV) closure for ensuring physical layout of the chip complies with all manufacturing and design rules
- Engineering Change Order (ECO) to resolve and closure
- Sign-off services

Benefits

eInfochips helped with the successful tape-out of 4 ASICs across the 5nm, 4nm and 3nm technology nodes. eInfochips was able to meet the stringent timeline by implementing more than 25 blocks within 6 months.

About eInfochips

eInfochips, an Arrow Electronics company, is a leading provider of digital transformation and product engineering services. eInfochips accelerates time to market for its customers with its expertise in the areas of IoT, AI/ML, security, sensors, wireless, cloud, and power. eInfochips has been ecognized as a leader in Engineering R&D services by many top analysts and industry bodies, including Gartner, Zinnov, ISG, IDC, Nasscom and others.

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