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JOB DESCRIPTION, ROLE & RESPONSIBILITES

POSITION TITLE: Technical Lead – Physical Design
LOCATION: Noida/ Bangalore/ Hyderabad/ Chennai/ Ahmedabad

POSITION SUMMARY

The candidate should have direct and first-hand experience working in managing 4 -10 members engineering team – and servicing clients in Project (ODC) based execution model as well as Staffing (Hyderabad Onsite requirements).

ROLE & RESPONSIBILITIES

- Engineer will be responsible for floor-planning, timing constraints, physical synthesis, formal verification, clock tree optimization, routing, extraction, timing closure, DFT, Antenna fixing &signal integrity, Power grid analysis etc in ASIC PNR Flow
- will be responsible for executing the block level place and route assignments from Netlist through GDS flow
- Responsible for full chip implementation of complex SoCs (RTL-to-GDSII)
- To Coordinate all timing budgeting required for physical design task
- To close STA timing across all corners and modes for blocks and should be able to generate ECO independently.
- Will be responsible to Work with design teams for closing CTS, IO timing, DFT timing.
- Responsible for digital design automation, flow-automation and regression across RTL-to-GDSII.
- To ensure successful delivery of his block(s) to customers
- To interface with other teams to understand design constraints, deliverable formats, customer requirements
- To contribute for enhancing the best practices of the physical design flow
- Should be able to lead 2-4 Engineers and ensuring their delivery including training (normal OR on the job), review and sign off.

ESSENTIAL SKILLS & EXPERIENCE

- Strong fundamentals on Physical design including Floorplan, power grid analysis, placement, cts, routing, DRC-LVS closure, timing closure, antenna fixing, signal integrity on 65nm, 45nm, 28nm, 16nm geometry.
- Sound expertise in Tcl, Perl, Shell scripting. Technically sound & good team player
- Hands-on experience with Place and Route tools (Synopsys - ICC , Cadence – Innovus / Encounter) is a must.
- Experience on latest technology (28nm,16nm,7 nm)
- Consistent track record of successful tapeouts of high performance networking ASICs

EDUCATION BACKGROUND

- B.E./ B.S./ B.Tech/ M.S./ M.Tech in VLSI/Electronics/Electrical/Computer/Instrumentation Engineering.

ABOUT eInfochips (An Arrow Company):

eInfochips, an Arrow company (A $30B, NASDAQ listed (ARW); Ranked #102 on the Fortune List), is a leading global provider of product engineering and semiconductor design services. 25+ years of proven track record, with a team of over 2500+ engineers, the team has been instrumental in developing over 500+ products and 40M deployments in 140 countries. Company's service offerings include Silicon Engineering, Embedded Engineering, Hardware Engineering & Digital Engineering services. eInfochips services 7 of the top 10 semiconductor companies and is recognized by NASSCOM, Zinnov and Gartner as a leading Semiconductor service provider.