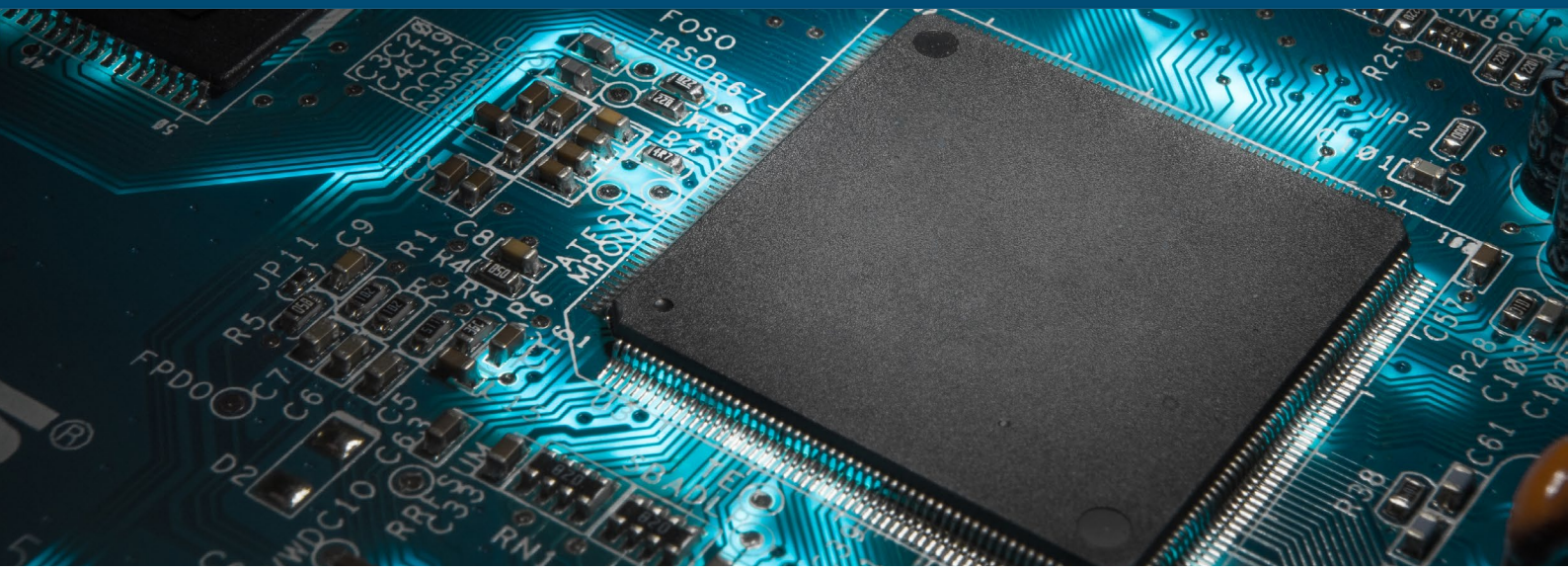
INTERLAKEN
Verification IP



Overview:

eInfochips's INTERLAKEN Verification IP Product is the comprehensive INTERLAKEN interface protocol validation solution. INTERLAKEN interface is widely used in networking based SoCs as scalable packet interface for packet transfer. INTERLAKEN VIP integrates automatic constrain random stimulus generation, assertion, protocol checking and functional coverage within a single extensible component, which incorporates INTERLAKEN protocol operation with full duplex packet transfer for channels that significantly reduces the time and cost of verifying complex INTERLAKEN based target system designs.

INTERLAKEN VIP provides a simple yet powerful user interface which drastically reduces the time and effort needed to create a verification environment and verify thoroughly to ensure first time right silicon. User can verify the complex design with few test cases in very short time instead of running multiple directed test cases.

INTERLAKEN VIP is reusable, highly configurable, pre-verified, plug-and-play verification component developed in System Verilog - UVM, which is solution for networking based SoC incorporating INTERLAKEN packet interface protocol at Module, Chip and System level.

Architecture:

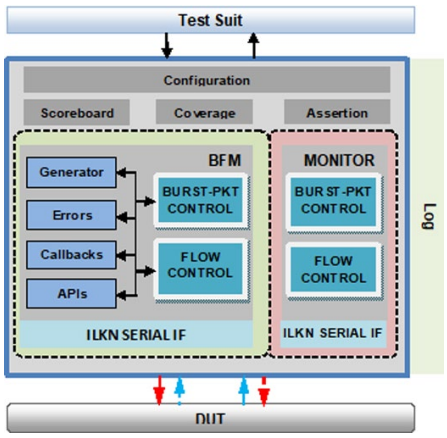


Figure 1: Interlaken VIP Architecture

INTERLAKEN VIP is developed using System Verilog, the unified language for Design & Verification and UVM reusable verification methodology.

INTERLAKEN VIP comprises of following major elements.

- Bus Function Model [BFM]
- Monitor
- Generator : Sequences & Sequencer
- Protocol Checkers
- APIs
- Callbacks
- Coverage Capability
- Assertions
- Configuration
- Report Generator

Application:

INTERLAKEN Verification IP provides quick and efficient way to verify INTERLAKEN packet protocol interface for design in various modes shown in figures. In active mode, it verifies INTERLAKEN in full duplex mode for VIP to DUT, in passive mode it verifies INTERLAKEN interface for single direction for VIP to DUT and in passive monitor only mode it verifies DUT to DUT INTERLAKEN full duplex communication.

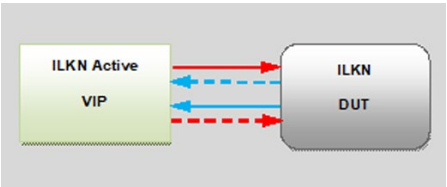


Figure 2: Interlaken VIP Active Mode

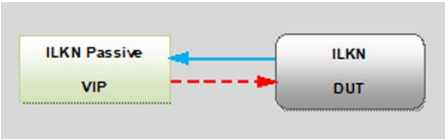


Figure 3: Interlaken VIP Passive Mode

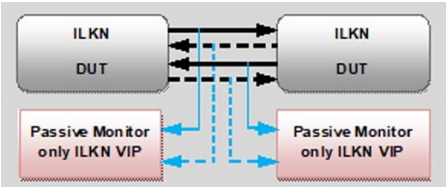
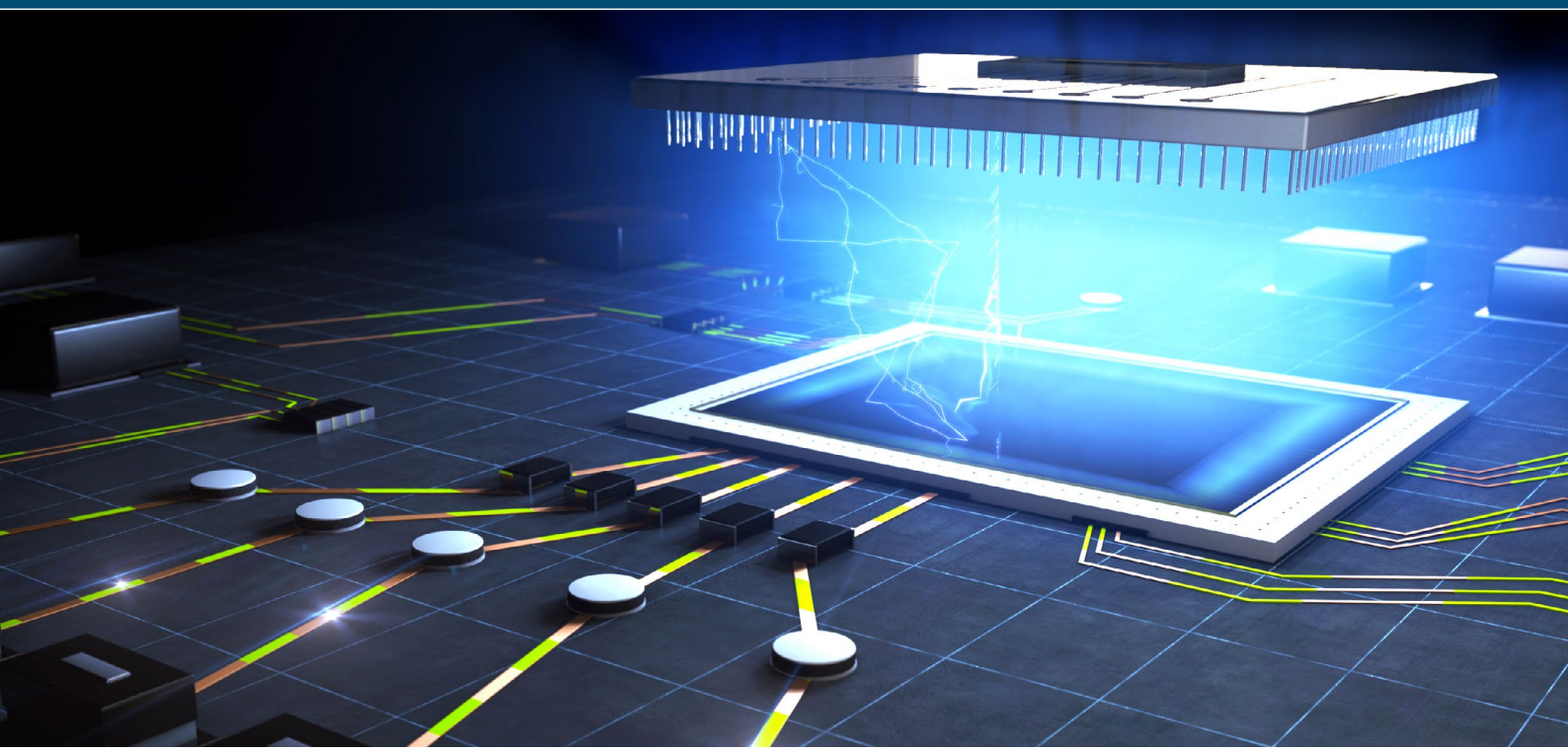


Figure 4: Interlaken VIP Passive Monitor Only Mode



Major Product Features:

- Configurable Burst Max and Burst Min
- 64/67B Encoding
- 64/67B Encoding with / without disparity
- IDLE - Other Control Words / Data Words
- Synchronous Scrambler
- Metaframe & Alignment
- Metaframe Lane Diagnostics
- Out Of Band Flow Control
- In Band Flow Control
- Configurable End Of Transmission (At packet boundary, in between the packet, or after transmitting N bytes)
- 1 to 256 logical number channels
- Lane Synchronization with multiple lane skews
- Configurable Serdes Lanes
- Multi Use Channel Extension
- Reset Calendar Sequence
- INTERLAKEN Interface Rate Limiting
- Rate Limiting by Skip Words
- Burst Enhance Packet Transfer Algorithm
- Configurable Serdes Bit Width - 1, 8, 10, 16, 20, 24, 32, 64, 67
- Configurable Meta Frames lengths. (Min 128 - Max 4096
- End Of Packet with Error
- Error before End Of Packet
- Burst Violation Error : Burst Max / Min Error
- Out Of Band CRC4 corruption
- CRC24 Corruption
- 64/67B Encoding Errors, Bad Control Words
- 64/67B Encoding Disparity Errors
- Bad Sync Word Error
- Bad Scramble Word Error
- Flow Control Errors
- Sync Word State machine testing sequence
- Scramble Word State machine testing sequence
- 64/67B Encoding state machine testing sequence

Extended Capabilities:

- Fully compliant to UVM Methodology
- Supports Directed, Constrain Random and Fully Random generation.
- Supports generic TLM interface for layered sequences support
- Supports variety of Error Injection via generators / callbacks in INTERLAKEN data bursts/packets and supports other protocol specific errors.
- Supports fully configurable INTERLAKEN protocol verification environment.
- Built-in assertions at INTERLAKEN data and flow control interface.
- Supports Functional Coverage collection.
- Supports hook-ups for end-to-end score boarding.
- Supports individual block functional verification.

Deliverables:

- INTERLAKEN VIP System-Verilog Source Code.
- User Guide and Release Notes.
- Test cases mentioned in the Test Plan along with the list of Sanity Test cases
- Test Plan + Coverage Plan
- Various prototype examples on topological usage of active, passive or passive monitor.
- Sample Verification Environment.