# TMDSEVM6474L / TMDSEVM6474LE Technical Reference Manual Version 2.0

Literature Number: SPRUGX2
Revised March 2011


## EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMER

**Not for Diagnostic Use: For Feasibility Evaluation Only in Laboratory/Development Environments**

The EVM may not be used for diagnostic purposes.

This EVM is intended solely for evaluation and development purposes. It is not intended for use and may not be used as all or part of an end equipment product.

This EVM should be used solely by qualified engineers and technicians who are familiar with the risks associated with handling electrical and mechanical components, systems and subsystems.

**Your Obligations and Responsibilities**

Please consult the EVM documentation, including but not limited to any user guides, set up guides or getting started guides and other warnings prior to using the EVM. Any use of the EVM outside of the specified operating range may cause danger to the users and/or produce unintended results, inaccurate operation, and permanent damage to the EVM and associated electronics. You acknowledge and agree that:

You are responsible for compliance with all applicable Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, UL, CSA, VDE, CE, RoHS and WEEE,) that relate to your use (and that of your employees, contractors or designees) of the EVM for evaluation, testing and other purposes.

You are responsible for the safety of you and your employees and contractors when using or handling the EVM. Further, you are responsible for ensuring that any contacts or interfaces between the EVM and any human body are designed to be safe and to avoid the risk of electrical shock.

You will defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, “Claims”) arising out of or in connection with any use of the EVM that is not in accordance with the terms of this agreement. This obligation shall apply whether Claims arise under the law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

**Warning**

The EVM board may get very hot during use. Specifically, the DSP, its heat sink and power supply circuits all heat up during operation. This will not harm the EVM. Use care when touching the unit when operating or allow it to cool after use before handling. If unit is operated in an environment that limits free air flow, a fan may be needed.

# Preface

**About this Document**
This document is a Technical Reference Manual for the TMS320C6474 Lite EVM designed and developed by eInfochips Limited for Texas Instruments, Inc.

**Notational Conventions**
This document uses the following conventions:

Program listings, program examples, and interactive displays are shown in a mono-spaced font. Examples use **bold** for emphasis, and interactive displays use bold to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Square brackets ( [ and ] ) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets. Unless the square brackets are in a bold typeface, do not enter the brackets themselves.

*Underlined, italicized non-bold* text in a command is used to mark place holder text that should be replaced by the appropriate value for the user's configuration.

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# Document Revision History

| Release | Chapter | Description of Change |
|---|---|---|
| 1.0 | All | First Draft |
| 2.0 | All | Updated for TMDSEVM6474LE |
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# Acronyms

| Acronym | Description |
|---|---|
| AMC or AdvancedMC | Advanced Mezzanine Card |
| AIF | Antenna Interface |
| CCS | Code Composer Studio |
| DDR2 | Double Data Rate 2 Interface |
| DIP | Dual-In-Line Package |
| DSP | Digital Signal Processor |
| DTC | Debug and Trace Controller |
| DTE | Data Terminal Equipment |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| EMAC | Ethernet Media Access Controller |
| EMIF | External Memory Interface |
| EVM | Evaluation Module |
| FPGA | Field Programmable Gate Array |
| FSYNC | Frame Synchronization |
| HPI | Host Port Interface |
| HPI DC | Host Port Interface Daughter Card |
| I2C | Inter Integrated Circuit |
| IPMB | Intelligent Platform Management Bus |
| IPMI | Intelligent Platform Management Interface |
| JTAG | Joint Test Action Group |
| LED | Light Emitting Diode |
| McBSP | Multi Channel Buffered Serial Port |
| MCH | MicroTCA Carrier Hub |
| MTCA or MicroTCA | Micro Telecommunication Computing Architecture |
| MMC | Module Management Controller |
| NU | Not Used (Not Assembled) |
| PICMG® | PCI Industrial Computer Manufacturers Group |
| SDRAM | Synchronous Dynamic Random Access Memory |
| SERDES | Serializer-Deserializer |
| SGMII | Serial Gigabit Media Independent Interface |
| SRIO | Serial RapidIO |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| XDS560v2 | Texas Instruments' System Trace Emulator |

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# 1. Overview

This chapter provides an overview of the C6474 Lite EVM along with the key features and block diagram.



## 1.1 Key Features

The C6474 Lite EVM is a high performance, cost-efficient, standalone development platform that enables users to evaluate and develop applications for the Texas Instruments' Multicore TMS320C6474 Digital Signal Processor (DSP). The Evaluation Module (EVM) also serves as a hardware reference design platform for the TMS320C6474 DSP. The EVM's form-factor is equivalent to a single-wide PICMG® AMC.0 R2.0 AdvancedMC module.

TMDSEVM6474L comes with an onboard XDS100 emulator. TMDSEVM6474LE comes with an integrated, high speed, system trace capable XDS560v2_Mezzanine emulator.

Schematics, code examples and application notes are available, to ease the hardware development process and to reduce the time to market.

The key features of the C6474 Lite EVM are:

- Texas Instruments' Fixed-Point Multicore (3 C64x+ Cores) DSP - TMS320C6474
- 256 Mbytes of DDR2 Memory
- 128 Mbytes of NAND Flash
- One Gigabit Ethernet port supporting 10/100/1000 Mbps data-rate
- 170 pin B+ style AMC Interface
- I2C EEPROM for booting
- 2 User LEDs and 3 User Switches
- 8 I2C controlled LEDs
- RS232 Serial interface on 3-Pin header or UART over mini-USB connector
- GPIO, McBSP, Timer, FSYNC, UART and I2C signals on 80-pin test header
- On Board FPGA (Actel's ProASIC 3) for DSP boot-strapping and NAND Flash interface
- On-Board XDS100 type Emulation using USB 2.0 interface[1]
- TI 60-Pin JTAG header to support External Emulator[1]
- High Speed Integrated XDS560v2 Mezzanine Emulator[2]
- Module Management Controller (MMC) for Intelligent Platform Management Interface (IPMI)
- Powered by DC power-brick adaptor (12V/2.5A) or AMC Carrier back-plane
- AMC like form factor

Note: [1] - Available in TMDSEVM6474L only
[2] - Available in TMDSEVM6474LE only

## 1.2 Functional Overview

The C6474 Lite EVM contains single TMS320C6474 fixed point Digital Signal Processor. TMS320C6474 device is based on the third-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture, making these DSPs an excellent choice for applications including video and telecom infrastructure, imaging/medical, and wireless infrastructure (WI). The C64x+ devices are upward code-compatible from previous devices that are part of the C6000™ DSP platform.

The functional block diagram of TMDSEVM6474L is shown in figure 1.1:

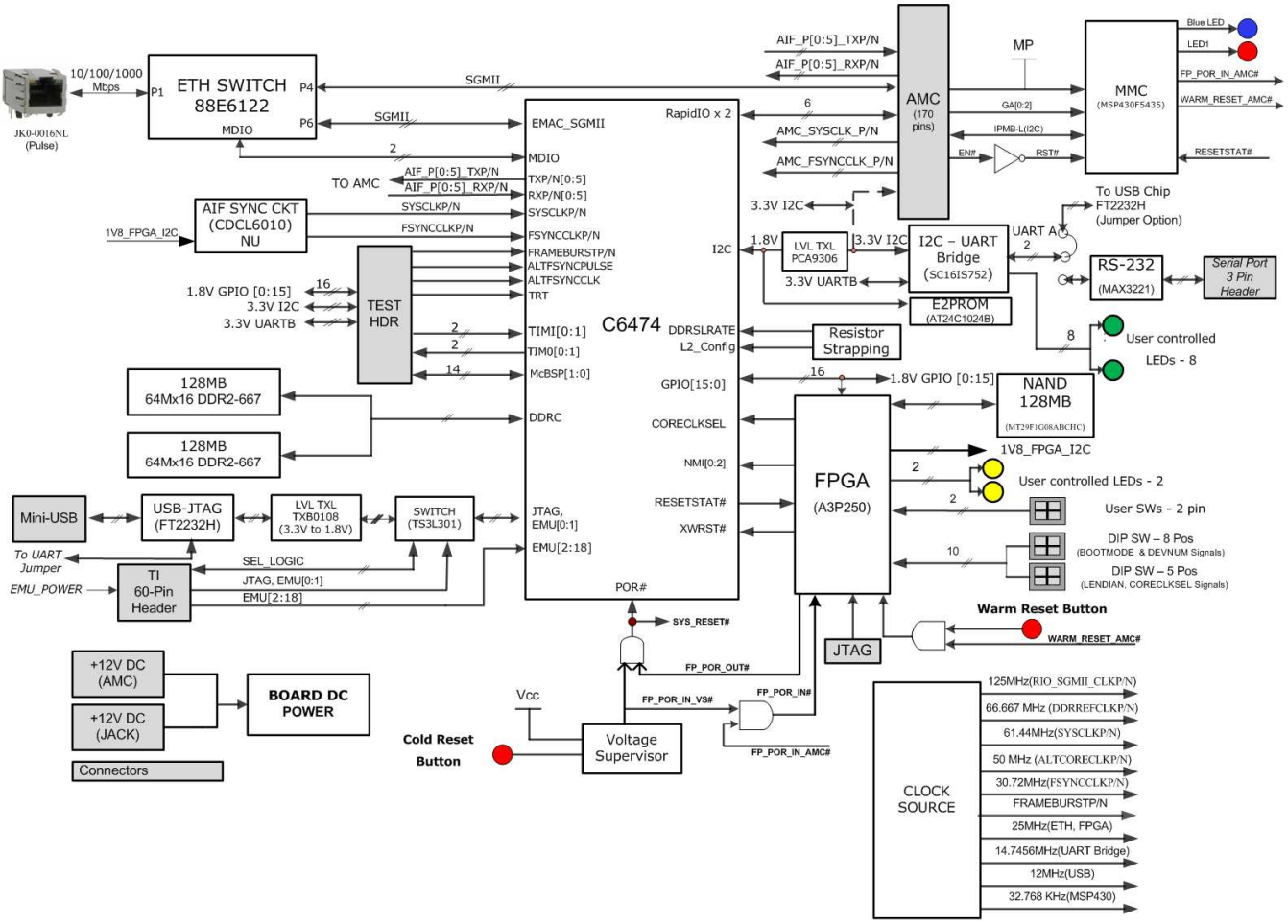


**Figure 1.1: Block Diagram of TMDSEVM6474L**

The functional block diagram of TMDSEVM6474LE is shown in figure 1.2:

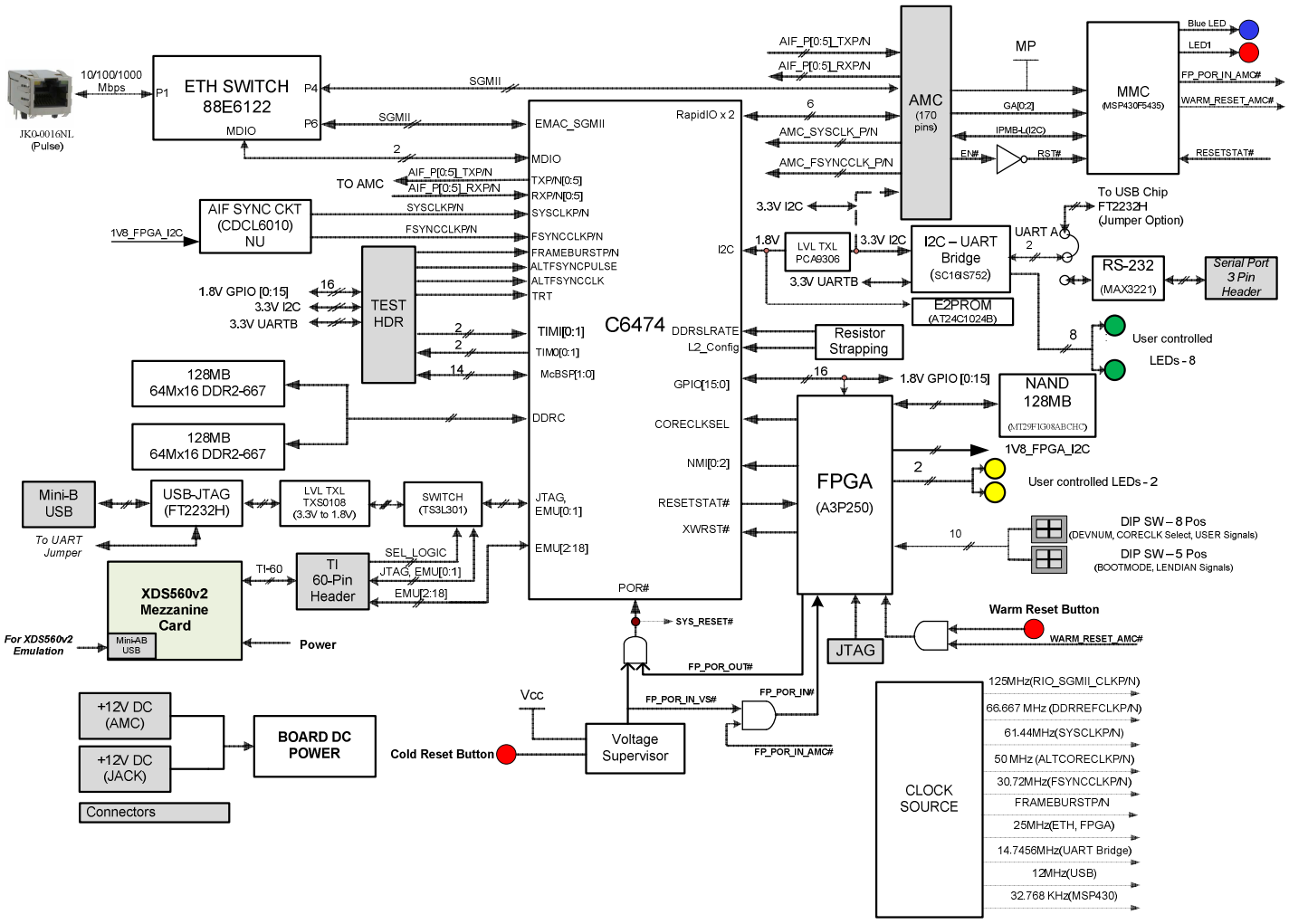


**Figure 1.2: Block Diagram of TMDSEVM6474LE**

## 1.3 Basic Operation

The C6474 Lite EVM platform is designed to work with TI's Code Composer Studio version 4 (CCSv4) development environment and is shipped with the latest version with all necessary emulation drivers. For TMDSEVM6474L, CCSv4 interfaces with the board via on-board emulation circuitry using the USB cable supplied along with this EVM or through external emulator. For TMDSEVM6474LE, CCSv4 interfaces with the board only via XDS560v2 System Trace emulator using the USB cable supplied.

To start operating the board, follow instructions in the Quick Setup Guide. Follow the instruction in BIOS MCSDK Getting Started Guide to install all the necessary development tools, drivers and documentation.

After the installation is completed, follow below steps to run Code Composer Studio.

1. Power ON the board using power brick adaptor (12V/2.5A) supplied along with this EVM or Insert this EVM board into MicroTCA chassis or AMC carrier back-plane.
2. Connect USB cable from host PC to EVM board for TMDSEVM6474L or to XDS560v2 Mezzanine emulator for TMDSEVM6474LE.
3. Launch Code Composer Studio from host PC by double clicking on its icon at PC desktop.

Detailed information about the EVM including examples and reference material is available in the DVD available with this EVM kit.

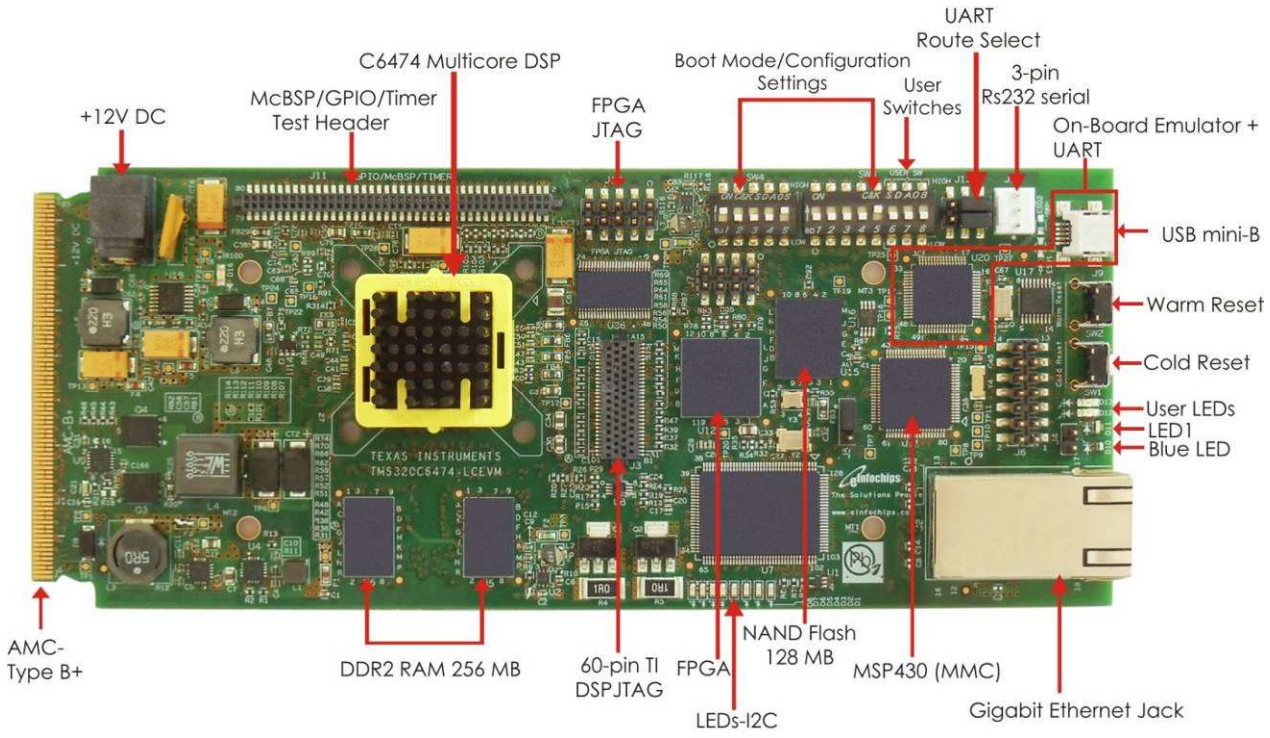


**Figure 1.3: TMDSEVM6474L**

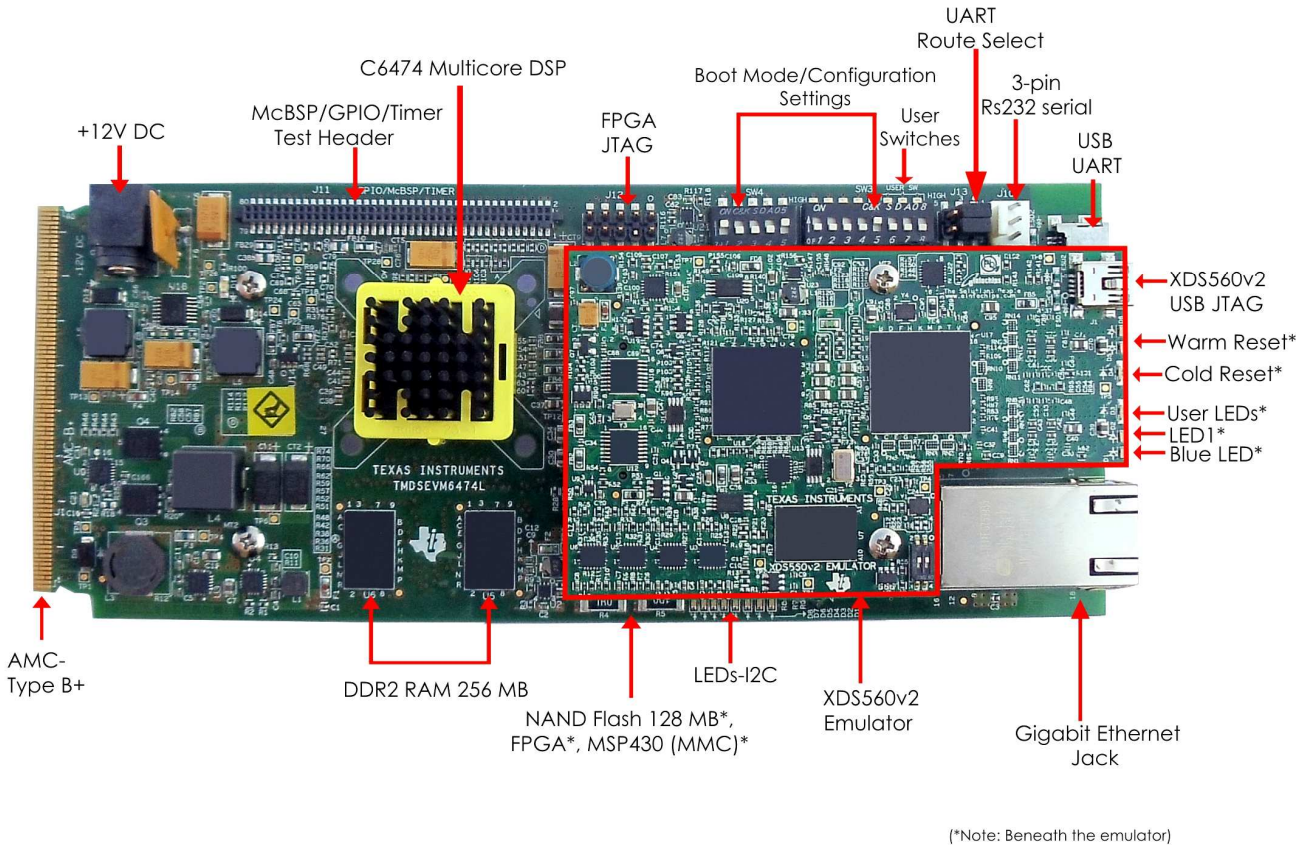


**Figure 1.4: TMDSEVM6474LE**

## 1.4 Power Supply

The C6474 Lite EVM can be powered from a single +12V / 2.5A DC (30W) external power supply connected to the DC power jack (J8). Internally, +12V input is converted into desired voltage levels such as, +5V, +3.3V, +2.5V, +1.8V, +1.5V, +1.1V and CVDD (0.9V ~ 1.2V) using local DC-DC converters.

- CVDD is used for DSP Core (Smart Reflex support)
- +1.5V is used for FPGA core
- +1.8V is used for DSP GPIOs, DDR2 / FPGA IO, NAND flash interface
- +2.5V is used for Ethernet Switch
- +3.3V is used for Oscillators, MSP430, Test Header
- The DC power jack connector is a 2.5mm barrel-type plug with center-tip as positive polarity.

The C6474 Lite EVM can also draw power from the AMC edge connector (J1). If the board is inserted into a PICMG® MicroTCA.0 R1.0 compliant system chassis or AMC Carrier back-plane, an external +12V supply from DC jack (J8) is not required.

# 2. Introduction to the C6474 Lite EVM board

This chapter provides an introduction and details of interfaces for the C6474 Lite EVM board. It contains:



## 2.1 Memory Map

The memory map of the TMS320C6474 device is as shown in Table 1. It provides a combined view of both local and global addresses. The C64x+ Megamodule local memories have both local and global addresses. The Megamodule registers have only local addresses which can be resolved within the Megamodule and cannot be accessed outside Megamodule. All other addresses listed in this table are global addresses which can be accessed from any bus master including all three C64x+ Megamodules, transfer controllers within the EDMA block and any peripheral that can master the bus.

**Table 1: TMS320C6474 Memory Map**

| Six Address Range | Memory Block Description |
|---|---|
| 0x 00000000 - 007FFFFF | Reserved |
| 0x 00800000 – 008FFFFF | L2 SRAM |
| 0x 00900000 – 00FFFFFF | L1P and L1D SRAM, Reserved |
| 0x 01000000 - 01BFFFFF | C64x+ Megamodule Registers |
| 0x 01C00000 - 027FFFFF | Reserved |
| 0x 02800000 - 0FFFFFFF | Control Registers on CFG SCR, Reserved |
| 0x 10000000 - 1FFFFFFF | Global RAM, Reserved |
| 0x 20000000 - 6FFFFFFF | Data space on EDMA SCR, Reserved |
| 0x 70000000 - 7FFFFFFF | DDR2 EMIF Config, Reserved |
| 0x 80000000 - 9FFFFFFF | DDR2 EMIF Data |
| 0x A0000000 - AFFFFFFF | AIF Data |
| 0x B0000000 - FFFFFFFF | Reserved |

## 2.2 EVM Boot mode and Boot configuration switch settings

The C6474 Lite EVM has 13 sliding DIP switches (Board Ref. SW3 and SW4) to determine boot mode, device number, Endian mode and DSP Core clock select (System/Alternate) options at every reset of the DSP.

The EVM contains DSP configuration options that are both user-defined and fixed which need to be known during DSP software development. The fixed configuration options are set up for proper EVM operation while user-defined parameters can be set by using configuration switches SW3 and SW4; SW3 determines device number and core clock source for DSP while SW4 determines DSP boot mode and little or big endian mode.

Whenever the user presses a Cold or Warm Reset button or power-cycles the board, an on-board FPGA latches the state of configuration inputs switches and presents them to DSP during reset period.

The configuration inputs which are multiplexed with GPIO pins are driven out from the FPGA only when RESETSTAT is low. This allows these configuration inputs to be latched by DSP when reset is released. Thereafter, they can be used in the GPIO mode to perform communication with FPGA.

For more information on the boot mode, refer TMS320C6474 Datasheet and TMS320C6474 Bootloader User's Guide (TMS320C645x/C647x DSP Bootloader User's Guide).

SW4 defines the DSP boot mode and DEVNUM pins for the EVM. There are 5 positions, which are described below:

- SW4 – positions 4, 3, 2 and 1 → Boot Mode Selection (BOOTMODE [3:0])
- SW4 – position 5 → Device Endian mode (LENDIAN)

SW3 defines DEVNUM pins and core clock select. There are 8 positions, which are described below:

- SW3 – positions 4, 3, 2 and 1 → Device Number (DEVNUM[3:0])
- SW3 – position 5 → Core clock select (CORECLKSEL)
- SW3 – position 8, 7, 6 → User Switches

Please refer section 4.3.3 of this document for default switch setting and details of each switch.

## 2.3 Clock Configuration

Table 3 shows clock configuration information of the EVM.

**Table 2: Clock Configurations**

| Clock | Frequency | Description |
|---|---|---|
| ALTCORECLKN/P | 50.000MHz | Clock Input for PLL1 (Differential) |
| DDRREFCLKN/P | 66.000MHz | DDR Reference Clock Input to DDR PLL (Differential) |

## 2.4 Board Revision ID

Board PCB (Printed Circuit Board) and PCA (Printed Circuit Assembly) revision are located below RJ-45 Jack in bottom silk, as shown below.

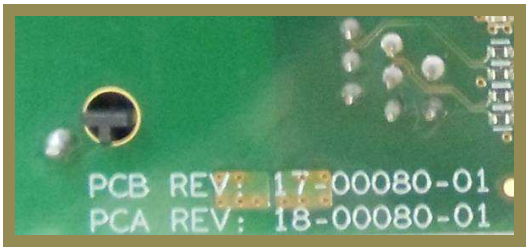


**Figure 2.1: EVM Board Revision**

Table 3 indicates the interpretation of PCA/PCB revisions; last two digits represent major PCB / PCA revision number.

**Table 3: PCA/PCB revision description**

| PCA REV | PCB REV | Description |
|---|---|---|
| 18-00080-01 | 17-00080-01 | Proto boards (Initial engineering samples) |
| 18-00080-02 | 17-00080-02 | Production boards |

## 2.5 JTAG - Emulation Overview

### 2.5.1 JTAG – TMDSEVM6474L

The EVM supports two different types of DSP Emulation - “USB mini-B” and “60-pin TI JTAG-DSP”.

USB emulation is supported through an on-board, optimized XDS100-class embedded emulation circuit. On-board (embedded) USB emulation is accessible through the USB mini-B connector (J9); hence any external emulator is not necessary to connect EVM with Code Composer Studio. User can connect CCS with target DSP in EVM with USB cable supplied along with this board.

TI 60-pin JTAG header (J3) is provided on-board to allow user to connect to external emulator for high speed real-time emulation. External/mezzanine emulators as XDS560v2 emulators and standard XDS510 or XDS560 emulators with 60 to 20-pin or 60 to 14-pin adapter boards from TI and 3rd-party vendors are supported. Please refer to the documentation supplied with your emulator for connection assistance.

Both emulator configurations are enabled by default and there is dynamic switching between them. On-board embedded JTAG emulator is default connection to DSP, however when external emulator is connected to EVM, board circuitry automatically switches to give access to external emulator. When both are connected at the same time, external emulator is given priority and on-board emulator is disconnected from DSP.

The interface between DSP, on-board and external emulator is shown in figure below:

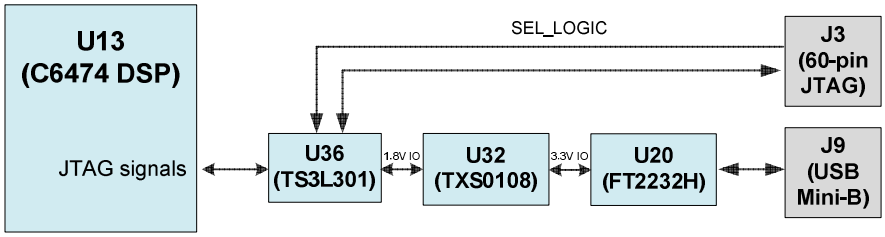


**Figure 2.2: TMDSEVM6474L JTAG emulation**

### 2.5.2 JTAG – TMDSEVM6474LE

In TMDSEVM6474LE, high speed real time emulation can be performed without needing an external emulator as it has an integrated, system trace capable XDS560v2 Mezzanine Emulator mounted on its TI 60-pin JTAG header (J3). User can connect the EVM to CCS by connecting the USB port of XDS560 Mezzanine emulator to PC using USB cable supplied with an EVM.

As high speed XDS560v2 Emulator is already mounted on TI 60-pin JTAG header of the EVM, the low speed XDS100 emulation is no longer required and not available to user.

It is important to note that for XDS560v2 emulation, the USB cable needs to be connected to the mini-AB connector (J1) on XDS560v2 Mezzanine emulator and not to mini-B connector (J9) on the main board. For TMDSEVM6474LE, the mini-B connector (J9) on the main board can be used to access UART-over-USB; please refer to section 2.12 of this document for more details.

The interface between DSP and XDS560v2 Mezzanine Emulator is shown in figure 2.3:

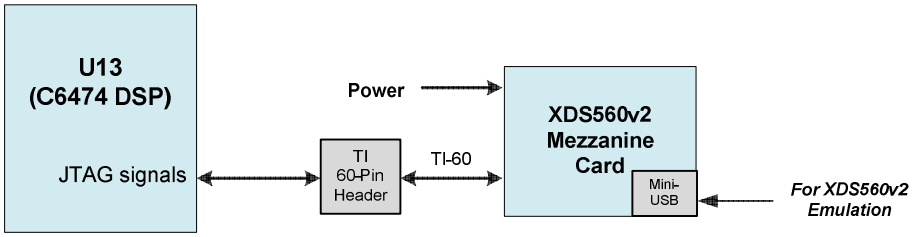


**Figure 2.3: TMDSEVM6474LE JTAG emulation**

#### 2.5.2.1 XDS560v2 Mezzanine Emulator Booting

When TMDSEVM6474LE is powered ON, the XDS560v2 mezzanine emulator starts booting. It takes approximately half minute to boot-up. The successful booting of XDS560v2 mezzanine emulator is indicated by following LEDs sequence:

- Green LED (D3) turns ON
- Yellow LED (D2) and Red LED (D1) turns ON
- Green LED (D3) blinks and turns OFF

After the completion of booting XDS560v2 mezzanine emulator is ready to interface with CCS. Once CCS is connected to the target DSP Green LED D4 turns ON.

The boot failure is indicated by simultaneous blinking of Red LED (D1), Yellow LED (D2) and Green LED (D3). In this case CCS can't be connected to XDS560v2 mezzanine emulator. The boot failure can happen when mezzanine emulator is attempted to mount over a non-compatible base EVM.

## 2.6 Clock Domains

The EVM incorporates variety of clocks to the TMS320C6474 as well as other devices which are configured automatically during the power up configuration sequence. The figure below illustrates the clocking for the system in EVM module. Please note that Y9 and U34 are not normally installed on the EVM.

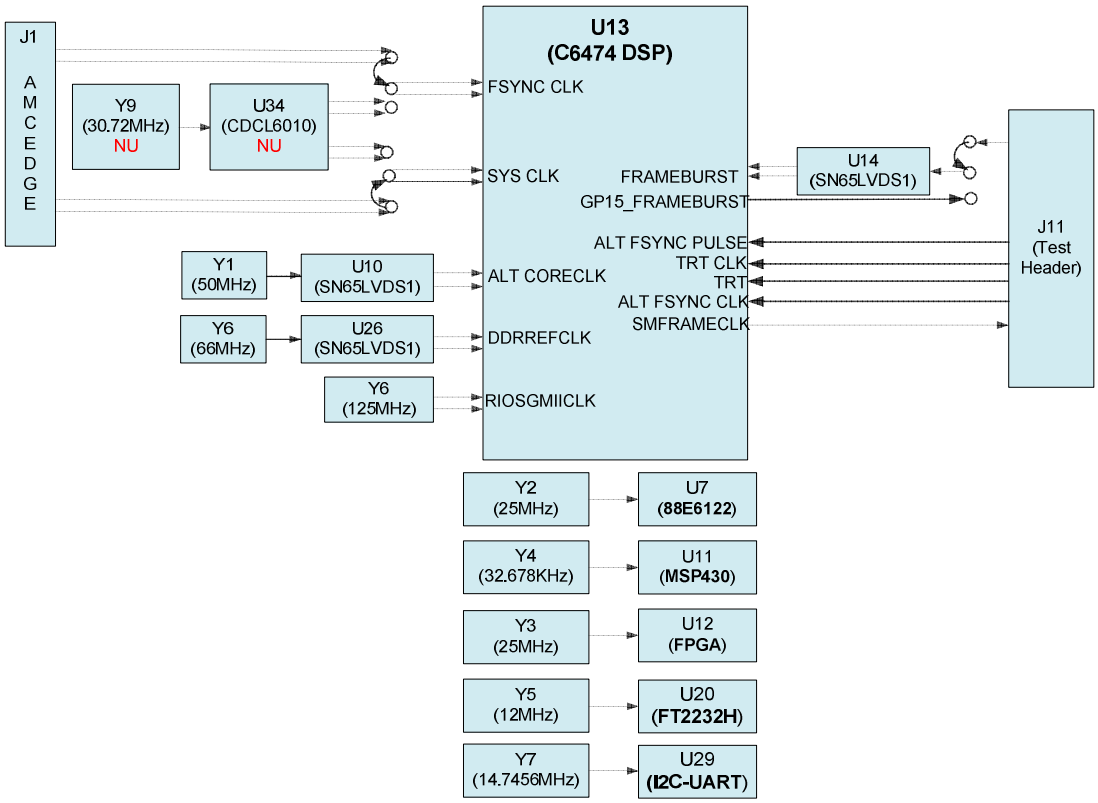


**Figure 2.4: C6474 Lite EVM Clock Domains**

## 2.7 I2C Boot EEPROM

The I2C EEPROM address 0x50 contains Power on Self Test (POST) program and I2C address 0x51 contains second level boot-loader program. The second level boot-loader reads the Out-Of-Box Demo program from the NAND FLASH memory.

## 2.8 FPGA

The FPGA (Actel #A3P250-FGG144) interface provides reset control circuitry and latching of device configuration pins. The logic level of these pins is latched at reset to determine the device configuration. These switch-controlled inputs are driven to the DSP at reset time.

FPGA supports two modes; Normal mode and NAND pass through mode. These modes are mutually exclusive modes. In Normal mode, FPGA provides access to FPGA registers through DSP's GPIO pins. FPGA supports 2 user LEDs and 3 User Switches through control registers.

In NAND pass through mode, DSP GPIOs are directly assigned to NAND pins. NAND access is only possible in NAND pass through mode. Details of these are provided in chapter 3 FPGA Functional Specification.

Below figure shows interface between C6474 DSP and FPGA.

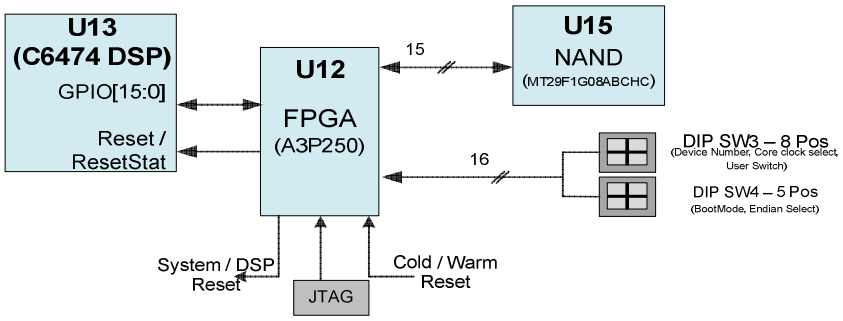


**Figure 2.5: C6474 Lite EVM FPGA Connections**

## 2.9 Ethernet Switch

The C6474 Lite EVM incorporates an Ethernet Switch 88E6122 with 2 Gigabit PHYs. Ethernet Switch's Port 6 is configured for SGMII interface with DSP, Port 1 is configured for copper interface to interface with external world through RJ-45 connector and port 4 is taken to the AMC connector in SGMII mode. RJ45 connector (J2) and Port 0 of AMC edge connector allows Gigabit Ethernet access to the SGMII port of C6474 DSP. At Power On, the Ethernet switch will be configured by the configuration EEPROM (U22). The default configuration will ensure the connectivity of DSP SGMII port to RJ45 connector and Port 0 of AMC edge connector.

Interface between DSP (U13) and Switch (U7) is shown in figure below.

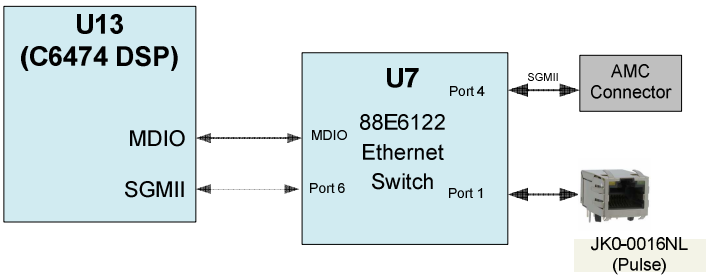


**Figure 2.6: C6474 Lite EVM Ethernet Switch Routing**

## 2.10 Serial RapidIO (SRIO) Interface

The C6474 Lite EVM supports high speed SERDES based Serial RapidIO (SRIO) interface. There are total two 1x RapidIO ports available on C6474. All SRIO ports are routed to AMC edge connector on board as per the PICMG AMC.0 R2.0 specifications. The SRIO ports 1-2 are routed to AMC ports 8-9 respectively. Below figure shows RapidIO connections between the DSP and AMC edge connector.

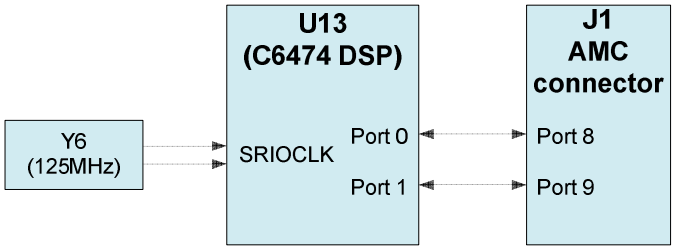


**Figure 2.7: C6474 Lite EVM SRIO Port Connections**

## 2.11 Antenna Interfaces

The C6474 Lite EVM has a high speed SERDES based Antenna Interface (AIF). There are total 6 AIF ports available on C6474. All AIF ports are taken to AMC edge connector on board. The figure below shows the AIF connections between DSP and AMC connector.

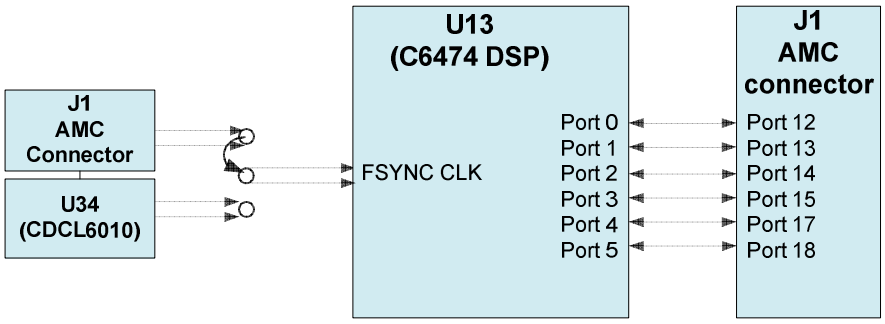


**Figure 2.8: C6474 Lite EVM AIF Port Connections**

## 2.12 UART Interface

A serial port is provided for debugging purpose using an I2C-UART bridge. This serial port can be accessed either through USB connector (J9) or through 3-pin serial port header (J10). The selection can be made through UART Route Select shunt J13 as follows:

- UART over mini-USB Connector (J9) - Shunts installed over J13.3-J13.1 and J13.4 -J13.2 **(Default)**
- UART over 3-Pin Header J10 - Shunts installed over J13.3-J13.5 and J13.4 -J13.6

A 3-pin to 9-pin DTE (Data Terminal Equipment) serial cable is provided in the EVM kit to connect the J10 serial port to PC. An additional UART port is also routed from I2C-UART Bridge to 80 pin header J11.

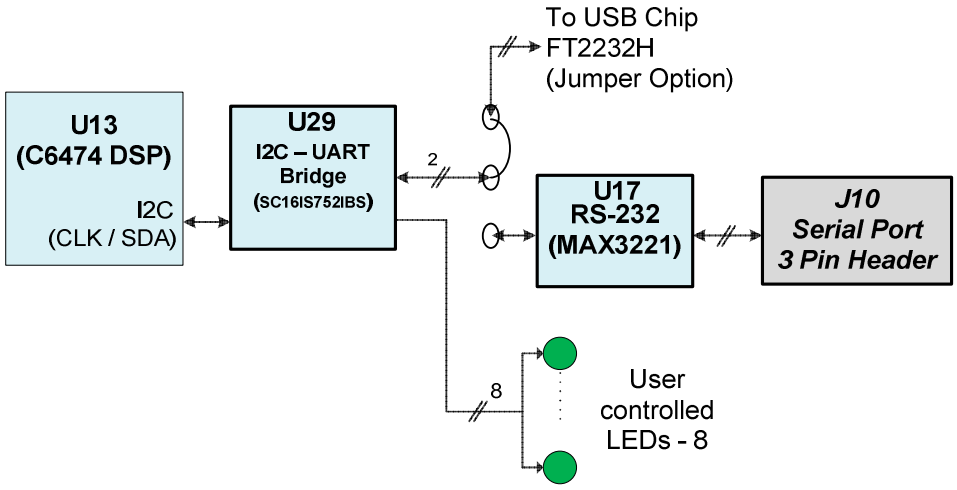


**Figure 2.9: C6474 Lite EVM UART Connections**

## 2.13 Module Management Controller (MMC) for IPMI

The C6474 Lite EVM supports limited set of Intelligent Platform Management Interface (IPMI) commands using Module Management Controller (MMC) based on Texas Instruments MSP430F5435 mixed signal processor.

The MMC will communicate with MicroTCA Carrier Hub (MCH) over IPMB (Intelligent Platform Management Bus) when inserted into AMC slot of a PICMG® MTCA.0 R1.0 compliant chassis. The primary purpose of the MMC is to provide necessary information to MCH, to enable the payload power to the C6474 Lite EVM when it is inserted into the MicroTCA chassis.

The EVM also supports a Blue LED and LED1 on the front panel as specified in PICMG® AMC.0 R2.0 AdvancedMC base specification. Both of these LEDs will blink as part of initialization process when the MMC will receive management power.

Blue LED:

Blue LED will turn ON when MicroTCA chassis is powered ON and an EVM is inserted into it. The blue LED will turn OFF when payload power is enabled to the EVM by the MCH.

LED1:

Red colored LED1 will normally be OFF. It will turn ON to provide basic feedback about failures and out of service.

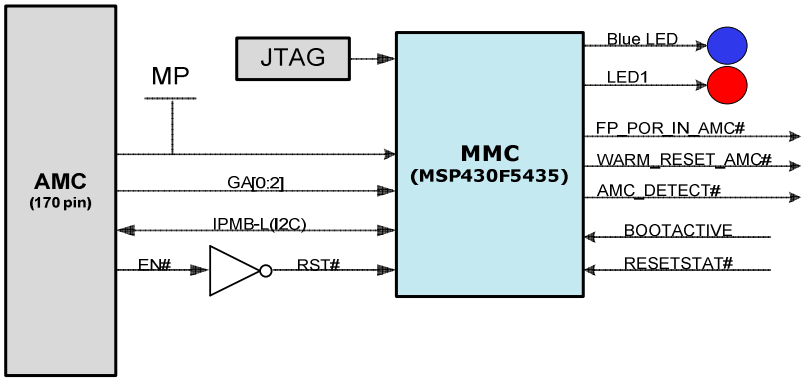


**Figure 2.10: C6474 Lite EVM MMC Connections for IPMI**

## 2.14 Additional Headers

The C6474 Lite EVM contains an 80 pin header (J11) which has GPIO, McBSP, Timer, FSYNC, I2C and UART signal connections. It shall be noted that I2C and UART connections to this header (J11) are of 3.3V level whereas GPIO, McBSP, Timer and FSYNC signals are of 1.8V level.

# 3. FPGA Functional Specification

This chapter contains an overview of the FPGA



## 3.1 FPGA modes

The FPGA can be configured in two modes. They are:

1. Normal mode
2. NAND pass through mode

After the completion of booting, DSP GPIO 14 is used to select between the Normal mode and the NAND Pass through mode.

If DSP GPIO 14 is 1'b0, then normal mode is selected. FPGA registers can be accessed in normal mode of operation only.

If DSP GPIO 14 is 1'b1, then Pass-Through mode is selected. In this mode DSP GPIO pins are directly mapped to the pins of the NAND Flash memory except Write-Protect Pin. The Write-Protect pin is not mapped due to unavailability of a GPIO pin in NAND pass through mode. The Write-Protect Pin of NAND Flash is mapped to the bit [4] of NAND_CWR_REGH FPGA register. The user application will require to disable write protect using the FPGA normal mode and then switch to NAND pass through mode to write to the NAND flash.

## 3.2 FPGA – DSP communication signals

The GPIO signals used for communication between FPGA and DSP when FPGA is in Normal mode are described in Table 2. The GP [12:13] are not used.

**Table 4: GPIO pin mapping in Normal mode**

| GPIO# | Function | Direction | Description |
|---|---|---|---|
| GP[7:0] | Data | Bidirectional | This is 8-bit wide bidirectional bus, shared for address and data. Whether the signals currently carry address, read data, or write data is defined by the Command signals. |
| GP[9:8] | Command | Input | These bits define the bus operation for the current strobe period.<br>00 - NOP<br>01 - address cycle<br>10 - read cycle<br>11 - write cycle |
| GP10 | Strobe | Input | This signal is used to synchronize the bus activity between the DSP and FPGA. The DSP is always master of the bus timing. |
| GP11 | Ready | Output | A low value on this pins during a read or write cycle will cause the DSP to extend the cycle until the signal goes high. This signal is not monitored for address and NOP cycles |
| GP14 | FPGA mode select | Input | This signal selects the mode of communication with the NAND Flash Memory. If it is 1'b1, then pass-through mode is enabled whereby the DSP GPIO pins are directly mapped to the pins of NAND Flash Memory. If it is 1'b0, then Normal Mode of operation is selected in which FPGA Configuration Registers will be accessed. |
| GP 15 | I2C-UART interrupt | Output | This signal directly follows the Bridge Interrupt input to FPGA. |

The GPIO signals used for communication between FPGA and DSP when FPGA is used in NAND pass through mode are described in Table 3.

**Table 5: GPIO pin mapping in NAND pass through mode**

| GPIO# | Function | Direction | Description |
|---|---|---|---|
| GP[7:0] | Data | Bidirectional | This 8-bit data bus is mapped to the 8-bit data bus of NAND Flash Memory. |
| GP[9:8] | Command | Input | GP[8] pin is mapped to the Command Latch Enable (CLE) pin of NAND Flash Memory.<br>GP[9] pin is mapped to the Address Latch Enable (ALE) pin of NAND Flash Memory. |
| GP10 | Write enable | Input | This signal is mapped to the Write Enable (nWE) pin of the NAND Flash Memory. |
| GP11 | Ready | Output | This signal is mapped to the Ready/Busy (RB) pin of the NAND Flash Memory. |
| GP12 | Read enable | Input | This signal is mapped to the Read Enable (nRE) pin of the NAND Flash Memory. |
| GP13 | Chip enable | Input | This signal is mapped to the Chip Enable (nCE) pin of the NAND Flash Memory. |
| GP14 | FPGA mode select | Input | This signal selects the mode of communication with the NAND Flash Memory. If it is 1'b1, then pass-through mode is enabled whereby the DSP GPIO pins are directly mapped to the pins of NAND Flash Memory. If it is 1'b0, then Normal Mode of operation is selected in which FPGA Configuration Registers will be accessed. |
| GP 15 | I2C-UART interrupt | Output | This signal directly follows the Bridge Interrupt input to FPGA. |

## 3.3 FPGA memory map

Table 4 describes the memory map of FPGA when FPGA is configured in Normal mode of operation.

**Table 6: FPGA Memory Map**

| GPIO[7:0] | Memory |
|---|---|
| 0x00 – 0x22 | Configuration Memory Space |

## 3.4 FPGA configuration registers

The following table enlists the FPGA configuration register and its description:

**Table 7: FPGA configuration Registers set**

| Name | Address | Read / Write | Default value | Data bits | Description |
|---|---|---|---|---|---|
| Reserved | 0x00 - 0x05 | - | - | 7:0 | Reserved for future use. |
| BITFILE_VER_REG | 0x06 | Read | 0x01 | 7:0 | Shows the BITFILE version |
| RTL_VER_REG | 0x07 | Read | 0x01 | 7:0 | Shows the RTL version |
| - | 0x08 | - | 0x00 | 7:0 | Reserved for future use. |
| CONTROL_REGH | 0x09 | Read / Write | 0x70 | 3:0 | Reserved for future use. |
| | | | | 4 | Write Protect Bit<br>1 => Disable<br>0 => Enable<br>This bit is mapped to the Write-Protect pin of NAND Flash Memory if the Pass-Through Mode is enabled. |
| | | | | 5 | User LED 0 Data. The bit value that is written at this location is driven on the User LED 0, if the User LED is enabled via NAND_CWR_REGH[7]. |
| | | | | 6 | User LED 1 Data. The bit value that is written at this location is driven on the User LED 1, if the User LED is enabled via NAND_CWR_REGH[7]. |
| | | | | 7 | User LED's Enable/Disable<br>0 => FPGA drives 1'b1 on User LED's (Disable)<br>1 => Data present in NAND_CWR_REGH [6:5] is driven on the User LED's (Enable). |
| Reserved | 0x0A – 0x21 | - | - | 7:0 | Reserved for future use. (RFU) |
| USER_SW_REG | 0x22 | Read | 0x00 | 0 | tievm_user_sw1_i |
| | | | | 1 | tievm_user_sw2_i |
| | | | | 3 | tievm_user_sw3_i |
| | | | | 4:2 | Reserved for future use |
| | | | | 7:5 | tievm_board_ver_i[2:0] |

## 3.5 FPGA-DSP communication protocol in FPGA Normal mode

At system reset FPGA becomes master and DSP becomes slave. The FPGA will provide the boot parameters to DSP. Once booting is done the FPGA will become slave and DSP will become master, at this point the below mentioned protocol is implemented.

The 16 bit bus from DSP GPIO to FPGA is divided in

- 8-bit bi-directional bus which is shared between data and address.
- 4-bit for control and handshaking signals.
- 2-bits are not used.

DSP to FPGA has strobe based asynchronous communication.

After the DSP reset and boot sequence, the GPIO pins will transition from their configuration role to their role in the GPIO Bus. The DSP is the master of the GPIO BUS. The DSP will initiate bus cycles, define how long they last and when they will complete. The FPGA can extend a read or write cycle if needed.

The normal write sequence is for the DSP to issue an address cycle followed by a write cycle. The normal read sequence is for the DSP to issue an address cycles followed by a read cycle. If a read or write cycle is not preceded by an address cycle, the address of the last cycle is used. This allows repeated reads or writes to a given register.

To initiate an address cycle the DSP will:

1. Set the value of cmd
2. Set the direction of data_io as output from DSP
3. Set the address value on data_io
4. Set stb_o active
5. Wait a minimum of 50 ns
6. Set stb_o inactive
7. Wait a minimum of 50 ns before the next cycle starts

**Procedure 3-1: Address cycle Initiation by DSP**

To initiate a write cycle the DSP will:

1. Set the value of cmd
2. Set the direction of data_io as output from DSP
3. Set the write data value on data_io
4. Set stb_o active
5. Wait a minimum of 50 ns
6. If rdy_o is low wait until it is high
7. Set stb_o inactive
8. Wait a minimum of 50 ns before the next cycle starts

**Procedure 3-2: Write cycle Initiation by DSP**

To initiate a read cycle the DSP will:

1. Set the value of cmd
2. Set the direction of data_io as input to DSP
3. Set stb_o active
4. Wait a minimum of 50 ns
5. If rdy_o is low wait until it is high
6. read data_io and store as the read cycle result
7. Set stb_o inactive
8. Wait a minimum of 50 ns before the next cycle starts

**Procedure 3-3: Read Cycle Initiation by DSP**

The FPGA will only enable its data_io drive when cmd == READ and stb_o is active. The FPGA must ensure that its driver is off no later than 40 ns after stb_o goes inactive.

The bus may idle after any of the above cycles; an explicit NOP cycle is not needed

## 3.6 Sequence of Operation

Following section provides details of FPGA sequence of operation.

### 3.6.1 Boot sequence – Power-On (Cold) Reset

1. On system reset (power-on reset), available through the global FPGA system reset pin, assert POR# and XWRST# pin active low
2. Wait for the FPGA internal PLL to stabilize
3. Once the PLL is locked, user defined configuration pins and fixed configuration pins are latched by FPGA and pin status are provided to C6474 device configuration pins. For device configuration settings please refer sections 4.3.3 DSP Configurations and 4.3.4 DSP boot mode.
4. Wait for 50 µS. As the frequency of operation of the FPGA is 25MHz, the internal counters would count 2000 clock cycles
5. De-assert XWRST#. Keep POR# asserted.
6. Wait for 200 mS. As the frequency of operation of the FPGA is 25MHz, the internal counters would count 8000000 clock cycles. De-assert POR#.
7. Wait for RESETSTAT# signal from DSP to go from low to high. GPIO lines to GIC modules would be put in tri-state condition
8. If boot modes are for EMAC boot (0'b0100, 0'b0101, 0'b0110) on boot mode DIP input switch, wait for 4 seconds. Assert XWRST# and wait for 50 µS. De-assert XWRST#.
9. Indicate GIC module that the boot mode is over

**Procedure 3-1: Power on Reset**

### 3.6.2 Boot sequence – Warm Reset

1. On warm reset, available through the push button switches on-board, assert XWRST# pin active low
2. Once the PLL is locked, user defined configuration pins and fixed configuration pins are latched by FPGA and pin status are provided to C6474 device configuration pins. For device configuration settings please refer sections 4.3.3 DSP Configurations and 4.3.4 DSP boot mode.
3. Wait for 50 µS. As the frequency of operation of the FPGA is 25MHz, the internal counters would count 2000 clock cycles
4. De-assert XWRST#
5. Wait for RESETSTAT# signal from DSP to go from low to high. GPIO lines to GIC modules would be put in tri-state condition
6. Indicate GIC module that the boot mode is over

**Procedure 3-1: Warm Reset**

# 4. EVM Board Physical Specifications

This chapter describes the physical layout of the C6474 Lite EVM board and its connectors, switches and test points. It contains:



## 4.1 Board Layout

The C6474 Lite EVM board dimension is 7.11” x 2.89” (180.6mm x 73.5mm). It is a 12 layer board and powered through connector J8. Figure 3-1 and 3-2 shows assembly layout of the C6474 Lite EVM Board.

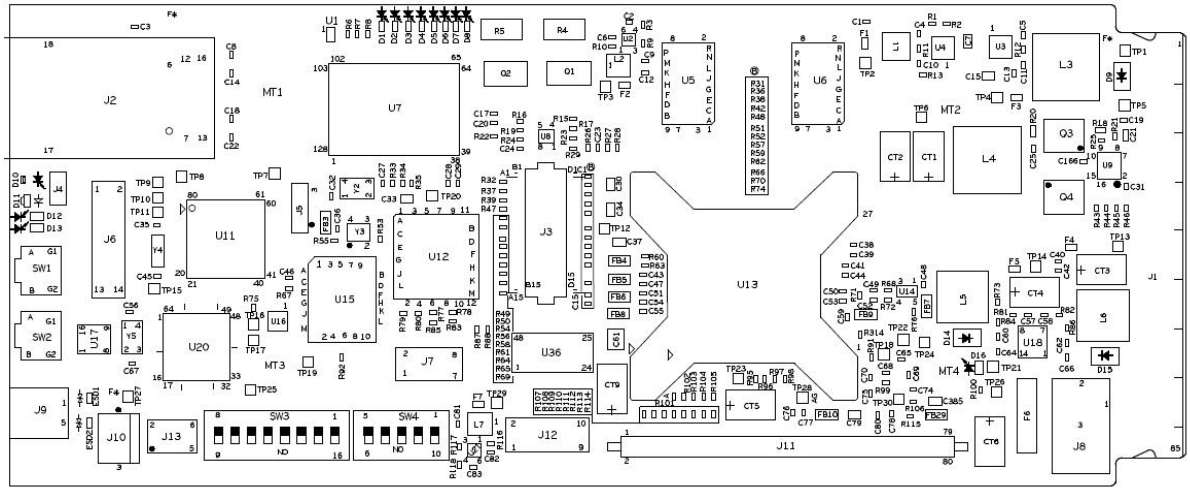

**Figure 4.1: C6474 Lite EVM Board Assembly Layout – TOP view**

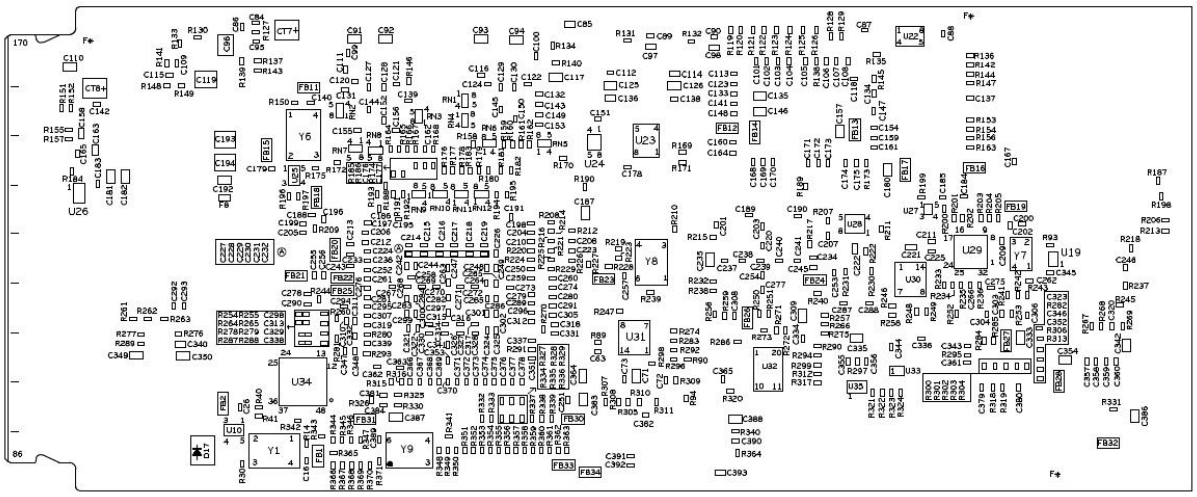

**Figure 4.2: C6474 Lite EVM Board layout – Bottom view**

## 4.2 Connector Index

The C6474 Lite EVM Board has several connectors which provide access to various interfaces on the board.

**Table 8: TMS320C6474 Board Connectors**

| Connector | Pins | Function |
|---|---|---|
| J1 | 170 | AMC Edge Connector |
| J2 | 18 | Ethernet RJ-45 Connector |
| J3 | 60 | TI 60-Pin DSP JTAG Connector [3] |
| J4 | 2 | MSP Reset Jumper |
| J5 | 3 | Power selection for MSP430 |
| J6 | 14 | MSP430 JTAG Connector |
| J8 | 3 | Power Input Jack Connector |
| J9 | 5 | Mini-B USB Connector |
| J10 | 3 | UART 3-Pin Connector |
| J11 | 80 | McBSP/GPIO/Timer Test Header |
| J12 | 10 | FPGA JTAG Connector |
| J13 | 6 | UART Path Select Connector |
| J1 | 5 | Mini-AB USB Connector [4] |

Note: [3] – Not Available in TMDSEVM6474LE.
[4] – Present on XDS5602v2 Mezzanine Card. Available in TMDSEVM6474LE only.

### 4.2.1 J1, AMC Edge Connector

The J1 card edge connector plugs into an AMC compatible carrier board and provides a high speed Serial RapidIO, AIF, SGMII and I2C interfaces to the carrier board. This connector is the 170-pin B+ style AMC connector. The signals on this connector are shown in the table below.

**Table 9: AMC Edge Connector**

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | GND | Ground Signal | 170 | GND | Ground Signal |
| 2 | VCC12 | +12V Power | 169 | NC | |
| 3 | PS1# | Presence 1 | 168 | NC | |
| 4 | MP | Management Power | 167 | NC | |
| 5 | GA0 | Geographic Address 0 | 166 | NC | |
| 6 | NC | | 165 | NC | |
| 7 | GND | Ground Signal | 164 | GND | Ground Signal |
| 8 | NC | | 163 | NC | |
| 9 | VCC12 | +12V Power | 162 | NC | |
| 10 | GND | Ground Signal | 161 | GND | Ground Signal |
| 11 | P4_SGMII_TXP | | 160 | I2C_SDA | I2C_SDA |
| 12 | P4_SGMII_TXN | | 159 | I2C_SCL | I2C_SCL |
| 13 | GND | Ground Signal | 158 | GND | Ground Signal |
| 14 | P4_SGMII_RXP | | 157 | ALT_FSYNC_CLKP | Alternate Frame |
| 15 | P4_SGMII_RXN | | 156 | ALT_FSYNC_CLKP | System clock |
| 16 | GND | Ground Signal | 155 | GND | Ground Signal |
| 17 | GA1 | Geographic Address 1 | 154 | ALT_SYSCLKP | Alternate |
| 18 | VCC12 | +12V Power | 153 | ALT_SYSCLKP | System clock |
| 19 | GND | Ground Signal | 152 | GND | Ground Signal |
| 20 | NC | | 151 | AIF_TXP5 | AIF Port 5-TX |
| 21 | NC | | 150 | AIF_TXN5 | AIF Port 5-TX |
| 22 | GND | Ground Signal | 149 | GND | Ground Signal |
| 23 | NC | | 148 | AIF_RXP5 | AIF Port 5-RX |
| 24 | NC | | 147 | AIF_RXN5 | AIF Port 5-RX |
| 25 | GND | Ground Signal | 146 | GND | Ground Signal |
| 26 | GA2 | Geographic Address 2 | 145 | AIF_TXP4 | AIF Port 4-TX |
| 27 | VCC12 | +12V Power | 144 | AIF_TXN4 | AIF Port 4-TX |
| 28 | GND | Ground Signal | 143 | GND | Ground Signal |
| 29 | NC | | 142 | AIF_RXP4 | AIF Port 4-RX |
| 30 | NC | | 141 | AIF_RXN4 | AIF Port 4-RX |
| 31 | GND | Ground Signal | 140 | GND | Ground Signal |
| 32 | NC | | 139 | NC | |
| 33 | NC | | 138 | NC | |
| 34 | GND | Ground Signal | 137 | GND | Ground Signal |
| 35 | NC | | 136 | NC | |
| 36 | NC | | 135 | NC | |
| 37 | GND | Ground Signal | 134 | GND | Ground Signal |
| 38 | NC | | 133 | AIF_TXP3 | AIF Port 3-TX |
| 39 | NC | | 132 | AIF_TXN3 | AIF Port 3-TX |
| 40 | GND | Ground Signal | 131 | GND | Ground Signal |
| 41 | ENABLE# | Enable Signal | 130 | AIF_RXP3 | AIF Port 3-RX |
| 42 | VCC12 | +12V Power | 129 | AIF_RXN3 | AIF Port 3-RX |

| | | | | | |
|---|---|---|---|---|---|
| 43 | GND | Ground Signal | 128 | GND | Ground Signal |
| 44 | NC | | 127 | AIF_TXP2 | AIF Port 2-TX |
| 45 | NC | | 126 | AIF_TXN2 | AIF Port 2-TX |
| 46 | GND | Ground Signal | 125 | GND | Ground Signal |
| 47 | NC | | 124 | AIF_RXP2 | AIF Port 2-RX |
| 48 | NC | | 123 | AIF_RXN2 | AIF Port 2-RX |
| 49 | GND | Ground Signal | 122 | GND | Ground Signal |
| 50 | NC | | 121 | AIF_TXP1 | AIF Port 1-TX |
| 51 | NC | | 120 | AIF_TXN1 | AIF Port 1-TX |
| 52 | GND | Ground Signal | 119 | GND | Ground Signal |
| 53 | NC | | 118 | AIF_RXP1 | AIF Port 1-RX |
| 54 | NC | | 117 | AIF_RXN1 | AIF Port 1-RX |
| 55 | GND | Ground Signal | 116 | GND | Ground Signal |
| 56 | SCL_IPMB | | 115 | AIF_TXP0 | AIF Port 0-TX |
| 57 | VCC12 | +12V Power | 114 | AIF_TXN0 | AIF Port 0-TX |
| 58 | GND | Ground Signal | 113 | GND | Ground Signal |
| 59 | NC | | 112 | AIF_RXP0 | AIF Port 0-RX |
| 60 | NC | | 111 | AIF_RXN0 | AIF Port 0-RX |
| 61 | GND | Ground Signal | 110 | GND | Ground Signal |
| 62 | NC | | 109 | NC | |
| 63 | NC | | 108 | NC | |
| 64 | GND | Ground Signal | 107 | GND | Ground Signal |
| 65 | NC | | 106 | NC | |
| 66 | NC | | 105 | NC | |
| 67 | GND | Ground Signal | 104 | GND | Ground Signal |
| 68 | NC | | 103 | NC | |
| 69 | NC | | 102 | NC | |
| 70 | GND | Ground Signal | 101 | GND | Ground Signal |
| 71 | SDA_IPMB | | 100 | NC | |
| 72 | VCC12 | +12V Power | 99 | NC | |
| 73 | GND | Ground Signal | 98 | GND | Ground Signal |
| 74 | NC | | 97 | RIO_TXP1 | SRIO Port 1-TX |
| 75 | NC | | 96 | RIO_TXN1 | SRIO Port 1-TX |
| 76 | GND | Ground Signal | 95 | GND | Ground Signal |
| 77 | NC | | 94 | RIO_RXP1 | SRIO Port 1-RX |
| 78 | NC | | 93 | RIO_RXN1 | SRIO Port 1-RX |
| 79 | GND | Ground Signal | 92 | GND | Ground Signal |
| 80 | NC | | 91 | RIO_TXP0 | SRIO Port 0-TX |
| 81 | NC | | 90 | RIO_TXN0 | SRIO Port 0-TX |
| 82 | GND | Ground Signal | 89 | GND | Ground Signal |
| 83 | PS0# | Presence 0 | 88 | RIO_RXP0 | SRIO Port 0-RX |
| 84 | VCC12 | +12V Power | 87 | RIO_RXN0 | SRIO Port 0-RX |
| 85 | GND | Ground Signal | 86 | GND | Ground Signal |

### 4.2.2 J2, Ethernet Connector

J2 is Gigabit RJ45 Ethernet connector with integrated magnetic. It is driven from the 88E6122 Marvell Switch device. The connections are shown in the table below.

**Table 10: Ethernet Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | Center Tap 2 |
| 2 | MD2- |
| 3 | MD2+ |
| 4 | MD1- |
| 5 | MD1+ |
| 6 | Center Tap 1 |
| 7 | Center Tap 3 |
| 8 | MD3+ |
| 9 | MD3- |
| 10 | MD0- |
| 11 | MD0+ |
| 12 | Center Tap 0 |
| 13 | LED1- |
| 14 | LED1+ |
| 15 | LED2- |
| 16 | LED2+ |
| 17 | Shield 1 |
| 18 | Shield 2 |

### 4.2.3 J3, DSP JTAG Connector

J3 is a standard TI 60 pin JTAG connector for XDS560v2 Emulator. The onboard switch multiplexes this interface with the onboard emulation interface. When an external emulator is plugged into J5, the external emulator can connect with the DSP. The I/O voltage level on these pins is 1.8V. So any 1.8V compatible emulator can be used to interface to the C6474 device. Note, that when an external emulator is plugged into this connector (J3), the onboard emulation circuitry will be disabled. The pin out for the connector is shown in the table below.

**Table 11: DSP JTAG Connector pin out**

| Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|
| B1 | ID0 | D1 | NC |
| A1 | Ground | C1 | ID2 |
| B2 | TMS | D2 | Ground |
| A2 | Ground | C2 | EMU18 |
| B3 | EMU17 | D3 | Ground |
| A3 | Ground | C3 | TRST |
| B4 | TDI | D4 | Ground |
| A4 | Ground | C4 | EMU16 |
| B5 | EMU14 | D5 | Ground |
| A5 | Ground | C5 | EMU15 |
| B6 | EMU12 | D6 | Ground |
| A6 | Ground | C6 | EMU13 |
| B7 | TDO | D7 | Ground |
| A7 | Ground | C7 | EMU11 |
| B8 | TVD | D8 | Type1 (Ground) |
| A8 | Type0 (NC) | C8 | TCLKRTN |
| B9 | EMU9 | D9 | Ground |
| A9 | Ground | C9 | EMU10 |
| B10 | EMU7 | D10 | Ground |
| A10 | Ground | C10 | EMU8 |
| B11 | EMU5 | D11 | Ground |
| A11 | Ground | C11 | EMU6 |
| B12 | TCLK | D12 | Ground |
| A12 | Ground | C12 | EMU4 |
| B13 | EMU2 | D13 | Ground |
| A13 | Ground | C13 | EMU3 |
| B14 | EMU0 | D14 | Ground |
| A14 | Ground | C14 | EMU1 |
| B15 | ID1 | D15 | Ground |
| A15 | TRGRSTz | C15 | ID3 |

### 4.2.4 J4, MSP430 Reset 2-Pin Connector

J4 is 2-pin male connector to Reset MSP430 during testing. By shorting both the pins, MSP430 will go into reset. The pin out for the connector is shown in the table below.

**Table 12: MSP Reset Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | Enable |
| 2 | Ground |

### 4.2.5 J5, MSP430 Power Selection 3-Pin Connector

J5 is 3-pin male connector for MSP430 Power Selection. By shorting Pin 2 with Pin 1, MSP430 will be powered from AMC Power (Default) and by shorting Pin 2 with Pin3; MSP430 will be powered from On board 3.3V regulator. The pin out for the connector is shown in the table below.

**Table 13: MSP430 Power Selection Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | AMC 3.3V Power |
| 2 | MSP430 Power |
| 3 | On Board 3.3V Power |

### 4.2.6 J6, MSP430 JTAG Connector

J6 is a 14 pin JTAG connector for MSP430 only. The pin out for the connector is shown in the table below.

**Table 14: MSP430 JTAG Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | TDO |
| 2 | NC |
| 3 | TDI |
| 4 | VCC |
| 5 | TMS |
| 6 | No Pin (**Key**) |
| 7 | TCK |
| 8 | TEST |
| 9 | NC |
| 10 | RESET# |
| 11 | NC |
| 12 | NC |
| 13 | NC |
| 14 | NC |

### 4.2.7 J8, Power Input Jack Connector

J8 is a 3 pin, 2.5mm power jack with the center tip as positive polarity. Do NOT use this connector, if powering the board from the AMC carrier back-plane.

The pin out for the connector is shown in the table below.

**Table 15: Power Input Jack Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | Ground |
| 2 | Transmit |
| 3 | Receive |

### 4.2.8 J9, Mini-B USB Connector

In TMDSEVM6474L, J9 is available to connect CCS with C6474 DSP using on-board XDS100 type emulation circuitry as well as to access UART-over-USB. In TMDSEVM6474LE, J9 is available for UART-over-USB only.

The pin out for the connector is shown in the table below.

**Table 16: Mini-B USB Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | VBUS |
| 2 | D- |
| 3 | D+ |
| 4 | ID |
| 5 | Ground |

### 4.2.9 J10, UART 3-Pin Connector

J10 is 3-pin male connector for RS232 serial interface. A 3-Pin female to 9-Pin DTE female cable will be needed to connect this to a PC. The pin out for the connector is shown in the table below.

**Table 17: UART Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | Ground |
| 2 | Transmit |
| 3 | Receive |

### 4.2.10 J11, GPIO McBSP, I2C, UART and Timer Test Connector

Connector J11 provides the GPIO, McBSP, I2C, UART and Timer Interfaces of the DSP. The signals on this connector are shown in the table below.

**Table 18: GPIO, McBSP, I2C, UART and Timer Test Connector**

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | VCC5 | +5V Power | 2 | VCC3.3 | +3.3V Power |
| 3 | GND | Ground Signal | 4 | VCC3.3 | +3.3V Power |
| 5 | VCC5 | +5V Power | 6 | VCC1.8 | +1.8V Power |
| 7 | GND | Ground Signal | 8 | GND | Ground Signal |
| 9 | GPIO 1 | GPIO | 10 | VCC1.8 | +1.8V Power |
| 11 | GPIO 3 | GPIO | 12 | GPIO 0 | GPIO |
| 13 | GPIO 5 | GPIO | 14 | GPIO 2 | GPIO |
| 15 | GPIO 7 | GPIO | 16 | GPIO 4 | GPIO |
| 17 | GND | Ground Signal | 18 | GPIO 6 | GPIO |
| 19 | GPIO 9 | GPIO | 20 | GND | Ground Signal |
| 21 | GPIO 11 | GPIO | 22 | GPIO 8 | GPIO |
| 23 | GPIO 13 | GPIO | 24 | GPIO 10 | GPIO |
| 25 | GPIO 15 | GPIO | 26 | GPIO 12 | GPIO |
| 27 | GND | Ground Signal | 28 | GPIO 14 | GPIO |
| 29 | FRAMEBURST | FSYNC Frame Burst signal | 30 | GND | Ground Signal |
| 31 | GND | Ground Signal | 32 | DSP_SMFRAMECLK | Frame Sync Clock Output |
| 33 | DSP_TRTCLK | Multi-standard FSYNC Clock | 34 | GND | Ground Signal |
| 35 | GND | Ground Signal | 36 | DSP_TRT | Multi-standard FSYNC Tick |
| 37 | FSYNC_PULSE | Alternate FSYNC input | 38 | GND | Ground Signal |
| 39 | GND | Ground Signal | 40 | ALT_FSYNC_CLK | Alternate Fsync Clock Input |
| 41 | NC | | 42 | GND | Ground Signal |
| 43 | GND | Ground Signal | 44 | NC | |
| 45 | NC | | 46 | GND | Ground Signal |
| 47 | GND | Ground Signal | 48 | MCBSP0_CLKR | MCBSP0 RX Clock |
| 49 | NC | | 50 | MCBSP0_FSR | MCBSP0 RX Frame Sync |
| 51 | McBSP1_CLKR | McBSP1 RX Clock | 52 | MCBSP0_DR | MCBSP0 RX Data |
| 53 | McBSP1_FSR | McBSP1 RX Frame Sync | 54 | MCBSP0_CLKX | McBSP0 TX Clock |
| 55 | McBSP1_DR | McBSP1 RX data | 56 | GND | Ground Signal |
| 57 | McBSP1_CLKX | McBSP1 TX Clock | 58 | MCBSP0_FSX | MCBSP0 TX Frame Sync |
| 59 | McBSP1_FSX | McBSP1 TX Frame Sync | 60 | MCBSP0_DX | MCBSP0 TX Data |
| 61 | GND | Ground Signal | 62 | MCBSP0_CLKS | McBSP0 Module Clock |
| 63 | McBSP1_DX | McBSP1 TX data | 64 | I2C_3V3_SDA | I2C Data |
| 65 | McBSP1_CLKS | McBSP1 Module Clock | 66 | I2C_3V3_SCL | I2C Clock |
| 67 | UARTB_3V3_TX | UARTB Transmit | 68 | TIM_0_IN | Timer 0 Input |
| 69 | UARTB_3V3_RX | UARTB Receive | 70 | GND | Ground Signal |
| 71 | GND | Ground Signal | 72 | TIM_1_IN | Timer 1 Input |
| 73 | NC | | 74 | GND | Ground Signal |
| 75 | GND | Ground Signal | 76 | TIM_0_OUT | Timer 0 Output |
| 77 | NC | | 78 | GND | Ground Signal |
| 79 | GND | Ground Signal | 80 | TIM_1_OUT | Timer 1 Output |

**Note: I2C and UART signals (highlighted in blue) are of 3.3V level. McBSP, Timer and GPIO signals (highlighted in green) are 1.8V level.**

### 4.2.11 J12, FPGA JTAG Connector

J12 is a 10 pin JTAG connector for FPGA only. The pin out for the connector is shown in the table below.

**Table 19: FPGA JTAG Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | TCK |
| 2 | GND |
| 3 | TDO |
| 4 | NC |
| 5 | TMS |
| 6 | VJTAG |
| 7 | VPUMP |
| 8 | TRST# |
| 9 | TDI |
| 10 | GND |

### 4.2.12 J13, UART Path Select Connector

UART port can be accessed either through USB connector (J9) or through 3-pin serial port header (J10). The selection can be made through UART path select connector J13 as follows:

- UART over USB Connector (Default): Shunt installed over J13.3-J13.1 and J13.4 -J13.2
- UART over 3-Pin Header J10 - Shunt installed over J13.3-J13.5 and J13.4 -J13.6

The pin out for the connector is shown in the table below.

**Table 20: UART Path Select Connector pin out**

| Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|
| 1 | FT2232 Transmit | 2 | FT2232 Receive |
| 3 | UART Transmit | 4 | UART Receive |
| 5 | MAX3221 Transmit | 6 | MAX3221 Receive |

### 4.2.13 J1, Mini-AB USB Connector – In TMDSEVM6474LE only

Mini-AB USB connector (J1) mounted on Mezzanine Card, is available to connect EVM to CCS for XDS560v2 type emulation. The pin out for the connector is shown in the table below.

**Table 21: Mini-B USB Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | VBUS |
| 2 | D- |
| 3 | D+ |
| 4 | ID |
| 5 | Ground |

## 4.3 Switches

The C6474 Lite EVM has two DIP and two push button switches, SW1 to SW4. SW1 and SW2 are push button switches and SW3 and SW4 are DIP switches. The function of each of the switches is listed in the table below.

**Table 22: C6474 Lite EVM Board Switches**

| Switch | Function |
|---|---|
| SW1 | Cold Reset |
| SW2 | Warm Reset |
| SW3 | DSP Device Number, Core select, User Switch |
| SW4 | DSP Boot mode, Endianess select |

### 4.3.1 SW1, Cold Reset

Push button Switch SW1 asserts DSP's POR# and global board reset when pressed. This is equivalent to a power cycle of the board and will have following effects:

- Resets DSP
- Resets FPGA
- Resets Ethernet Switch
- Resets I2C-UART bridge
- Reloads boot parameters

### 4.3.2 SW2, Warm Reset

Push button Switch SW2 asserts DSP's RESET# input when pressed. This will reset the DSP and boot parameters will be reloaded.

Re-launch and/or re-connect of CCS application may be required after pressing warm or cold reset buttons.

**Note:** User may refer TMS320C6474 Datasheet to check difference between assertion of DSP RESET# and DSP POR# signals.

### 4.3.3 SW3, DSP Configurations

SW3 is an 8 position DIP switch that is used for setting DSP Device Number. A diagram of SW3 switch (with factory default settings) is shown below.

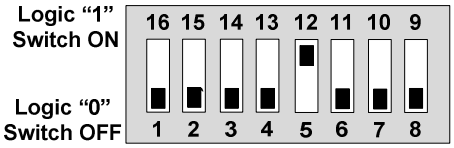


**Figure 4.3: SW3 default settings**

The following table describes the positions and corresponding function on SW1.

**Table 23: SW3, DSP Configuration Switch**

| SW3 Position | Description | Default Value | Function |
|---|---|---|---|
| 4 - 1 | Device Number [3:0] | 0000 | Device number selection for multiple DSPs |
| 5 | CORECLKSEL | 1(ON) | OFF – System clock is shared between AIF and input to PLLCTL1<br>ON – Alternate core clock is used as the input to PLLCTL1 and SYSCLK is used only for the AIF |
| 8-6 | USER SW[1:3] | 000 | DSP can read user switch value by accessing FPGA's internal registers |

### 4.3.4 SW4, DSP Boot mode

SW4 is a 5 position DIP switch that is used for DSP boot mode selection and Endian selection after Reset. A diagram of the SW4 switch (with factory default settings) is shown below.

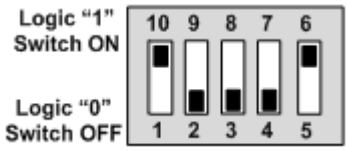


**Figure 4.4: SW4 default settings**

The following table describes the positions and corresponding function on SW4.

**Table 24: SW4, DSP Boot Mode Selection Switch**

| SW4 Position | Description | Default Value | Function |
|---|---|---|---|
| 4 - 1 | Boot Mode[3:0] | 0001 | Boot mode selection pins for DSP<br>Master I2C boot mode for I2C address 50h<br>Refer TMS320C6474 Datasheet for details of other boot modes supported. |
| 5 | LENDIAN | 1(ON) | OFF - Big Endian mode<br>ON - Little Endian mode(Default) |

**Note**: Please change Boot Mode [3:0] to "0010" for NAND boot mode of this EVM. "0010" is primarily a Master I2C boot mode for I2C address 51h for DSP, which works as NAND boot mode in this EVM.

## 4.4 Test Points

TMS320C6474 Board has 30 test points. The position of each test point is shown in the figure below.

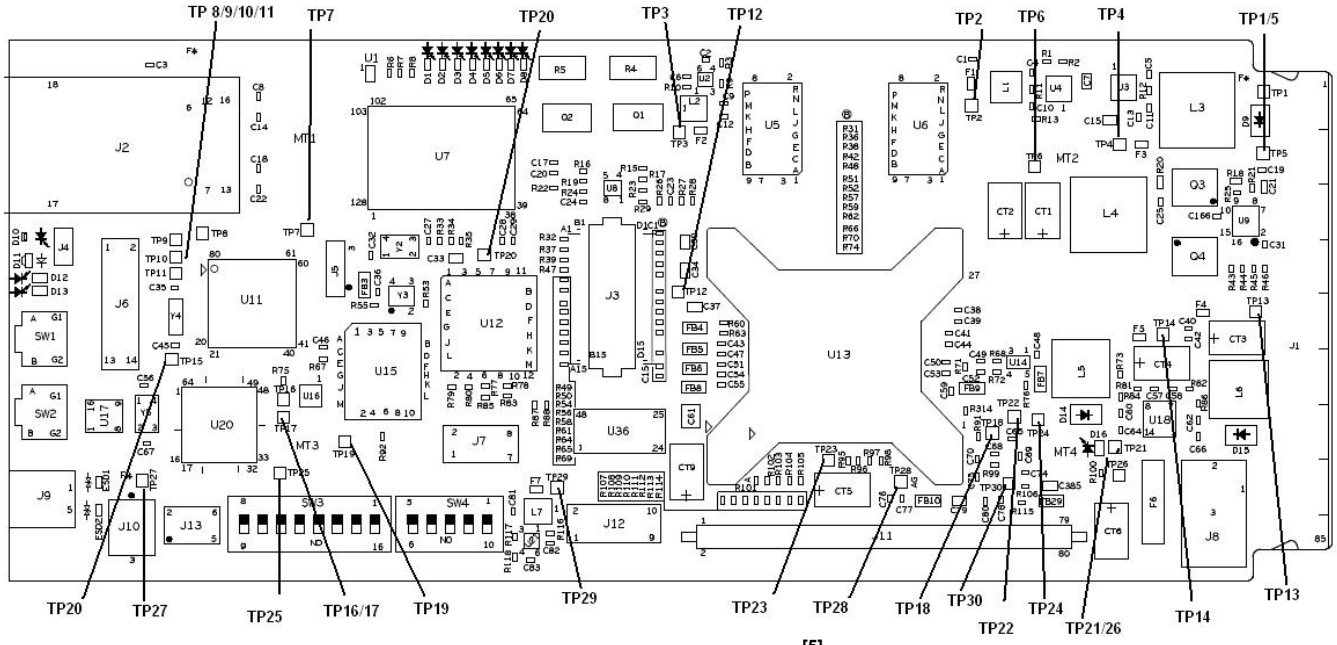


**Figure 4.5: Board Test Points [5]**

Note: [5] - Some of these TPs may not be visible in TMDSEVM6474LE

**Table 25: C6474 Lite EVM Board Test Points**

| Test Point | Signal | Test Point | Signal |
|---|---|---|---|
| TP1 | Management Power (+3.3V) | TP16 | FT2232H, GPIOH0 |
| TP2 | +2.5V Supply | TP17 | FT2232H, SUSPEND# |
| TP3 | +1.1V Supply | TP18 | CDCL6010 STATUS |
| TP4 | +5V Supply | TP19 | SYSTEM_RESET# |
| TP5, TP6, TP8, TP20, TP21, TP27 | Ground | TP22 | DSP_SYSCLKOUT |
| TP7 | Enable# | TP23 | DVDD1.8V_MON |
| TP9 | MSP430 MCLK | TP24 | CDCL6010 - YP10 |
| TP10 | MSP430 ACLK | TP25 | FT2232H, GPIOH1 |
| TP11 | MSP430 SMCLK | TP26 | +12V Input Supply |
| TP12 | System (Cold) Reset | TP28 | +CVDD Supply |
| TP13 | +1.8V Supply | TP29 | +1.5 Supply |
| TP14 | +3.3 Supply | TP30 | CDCL6010 - YN10 |
| TP15 | FT2232H, PWREN# | | |

## 4.5 System LEDs

The C6474 Lite EVM board has 13 LEDs. Their positions on the board are indicated in figure 4.7 and their descriptions are listed in table 26.

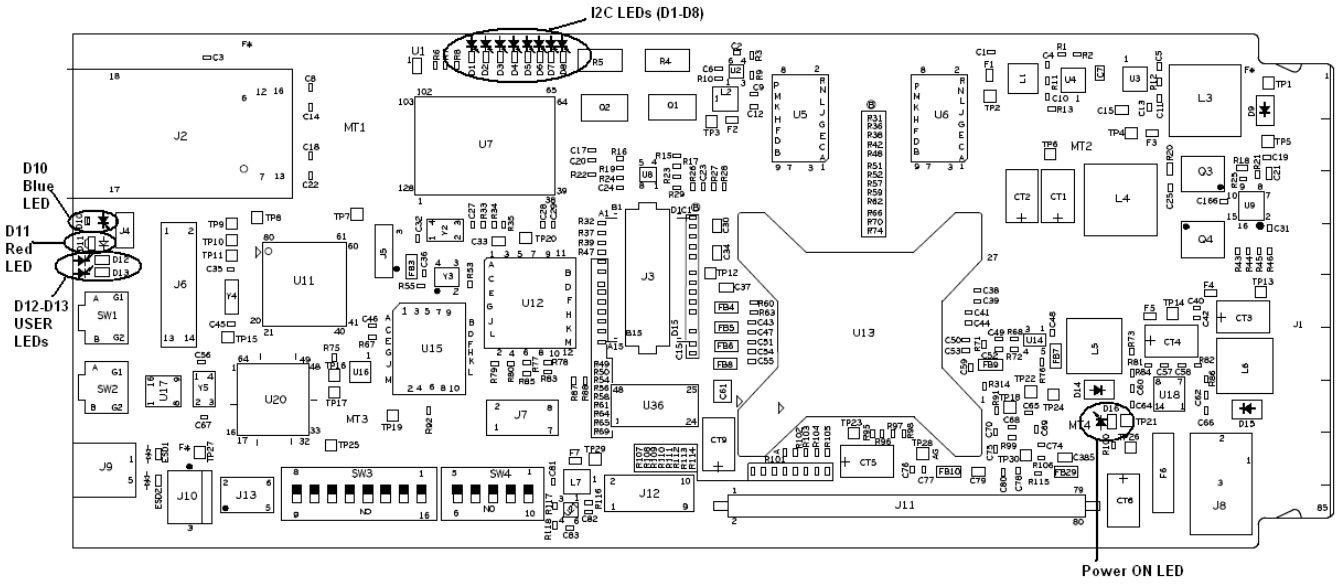


**Figure 4.6: TMS320C6474 Board LEDs**

**Table 26: TMS320C6474 Board LEDs**

| LED# | Color | Description |
|---|---|---|
| D1 – D8 | Green | I2C LEDs |
| D10 | Blue | Hot Swap status in AMC chassis |
| D11 | Red | Failure and Out of service status in AMC chassis |
| D12, D13 | Orange | User LEDs |
| D16 | Green | Board Powered ON Indicator |

Additional LEDs on TMDSEVM6474LE (XDS560v2 Mezzanine) board are highlighted in figure 4.7 and their description is listed in table 27.

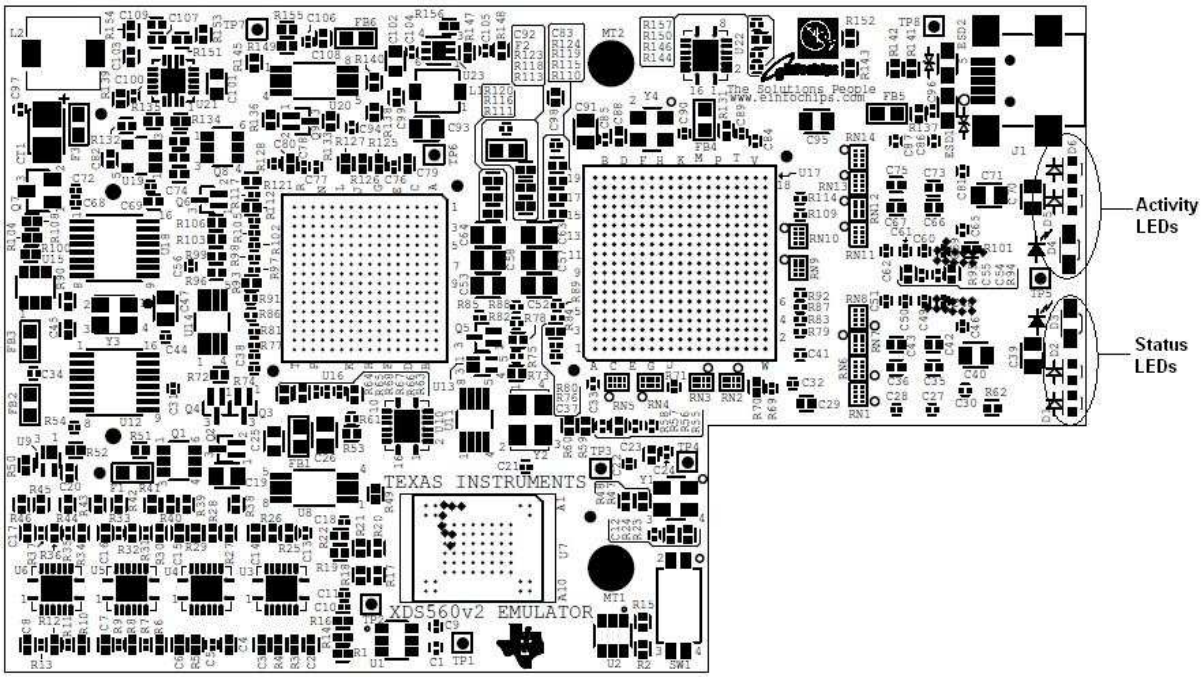


**Figure 4.7: TMDSEVM6474LE Board Additional LEDs**

**Table 27: TMDSEVM6474LE Board Additional LEDs**

| LED# | Color | Description |
|---|---|---|
| D1 (Activity LED 1) | Red | ON - DTC Ready<br>OFF - DTC Not Ready |
| D2 (Activity LED 2) | Yellow | ON - FPGA Programmed<br>OFF - FPGA Not Programmed |
| D3 (Activity LED 3) | Green | Reserved |
| D4 (Status LED 3) | Green | ON =CCS Connected<br>OFF= CCS Disconnected |
| D5 (Status LED 2) | Yellow | DTC to Host Activity |
| D6 (Status LED 1) | Orange | Target to DTC Trace Activity |

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