# TMDSEVM6472 / TMDSEVM6472LE Technical Reference Manual Version 2.0

Literature Number: SPRUFU2
Revised March 2011


**EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMER**

**Not for Diagnostic Use: For Feasibility Evaluation Only in Laboratory/Development Environments.**

The EVM may not be used for diagnostic purposes.

This EVM is intended solely for evaluation and development purposes. It is not intended for use and may not be used as all or part of an end equipment product.

This EVM should be used solely by qualified engineers and technicians who are familiar with the risks associated with handling electrical and mechanical components, systems and subsystems.

**Your Obligations and Responsibilities.**

Please consult the EVM documentation, including but not limited to any user guides, set up guides or getting started guides and other warnings prior to using the EVM. Any use of the EVM outside of the specified operating range may cause danger to the users and/or produce unintended results, inaccurate operation, and permanent damage to the EVM and associated electronics. You acknowledge and agree that:

You are responsible for compliance with all applicable Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, UL, CSA, VDE, CE, RoHS and WEEE,) that relate to your use (and that of your employees, contractors or designees) of the EVM for evaluation, testing and other purposes.

You are responsible for the safety of you and your employees and contractors when using or handling the EVM. Further, you are responsible for ensuring that any contacts or interfaces between the EVM and any human body are designed to be safe and to avoid the risk of electrical shock.

You will defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, “Claims”) arising out of or in connection with any use of the EVM that is not in accordance with the terms of this agreement. This obligation shall apply whether Claims arise under the law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

**Warning**

The EVM board may get very hot during use. Specifically, the DSP, its heat sink and power supply circuits all heat up during operation. This will not harm the EVM. Use care when touching the unit when operating or allow it to cool after use before handling. If unit is operated in an environment that limits free air flow, a fan may be needed.

## Preface

### About this Document

This document is a Technical Reference Manual for TMS320C6472 EVM designed and developed by eInfochips Limited for Texas Instruments, Inc.

### Notational Conventions

This document uses the following conventions:

Program listings, program examples, and interactive displays are shown in a mono-spaced font. Examples use **bold** for emphasis, and interactive displays use bold to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Square brackets ( [ and ] ) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets. Unless the square brackets are in a bold typeface, do not enter the brackets themselves.

*Underlined, italicized non-bold* text in a command is used to mark place holder text that should be replaced by the appropriate value for the user's configuration.

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# Document Revision History

| Release | Chapter | Description of Change |
|---|---|---|
| 1.0 | All | First Draft |
| 2.0 | All | Updated for TMDSEVM6472LE |
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# Acronyms

| Acronym | Description |
|---|---|
| AMC or AdvancedMC | Advanced Mezzanine Card |
| CCS | Code Composer Studio |
| DDR2 | Double Data Rate 2 Interface |
| DIP | Dual-In-Line Package |
| DSP | Digital Signal Processor |
| DTE | Data Terminal Equipment |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| EMAC | Ethernet Media Access Controller |
| EMIF | External Memory Interface |
| EVM | Evaluation Module |
| FPGA | Field Programmable Gate Array |
| HPI | Host Port Interface |
| HPI DC | Host Port Interface Daughter Card |
| I2C | Inter Integrated Circuit |
| IPMB | Intelligent Platform Management Bus |
| IPMI | Intelligent Platform Management Interface |
| JTAG | Joint Test Action Group |
| LED | Light Emitting Diode |
| McBSP | Multi Channel Buffered Serial Port |
| MCH | MicroTCA Carrier Hub |
| MTCA or MicroTCA | Micro Telecommunication Computing Architecture |
| MMC | Module Management Controller |
| PICMG® | PCI Industrial Computer Manufacturers Group |
| SDRAM | Synchronous Dynamic Random Access Memory |
| SERDES | Serializer-Deserializer |
| SGMII | Serial Gigabit Media Independent Interface |
| SRIO | Serial RapidIO |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| XDS560v2 | Texas Instruments' System Trace Emulator |

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# 1. Overview

This chapter provides an overview of the C6472 EVM along with the key features and block diagram.



## 1.1 Key Features

The C6472 EVM is a high performance, standalone development platform that enables users to evaluate and develop applications for the Texas Instruments' TMS320C6472 multicore Digital Signal Processor (DSP). The Evaluation Module (EVM) also serves as a hardware reference design platform for the TMS320C6472 DSP. The EVM's form-factor is equivalent to a single-width AMC (PICMG's AdvancedTCA Mezzanine Card) module.

TMDSEVM6472 comes with an onboard XDS100 emulator. TMDSEVM6472LE comes with an integrated, high speed, system trace capable XDS560v2 Mezzanine Emulator.

Schematics, logic equations and application notes are available to ease the hardware development process and reduce time to market.

The key features of the C6472 EVM are:

- EVM contains Texas Instruments' next-generation six core, fixed point DSP - TMS320C6472. C6472 DSP contains six on-chip C64x+ Megamodules.
- 256 Mbytes of DDR2 Memory
- 128 Mbytes of NAND Flash
- 2 Gigabit Ethernet ports supporting 10/100/1000 Mbps data-rate
- 170 pin B+ style AMC Interface
- I2C EEPROM for booting
- 2 user LEDs and 2 user switches
- 8 I2C controlled LEDs
- RS232 Serial port on 3-Pin header
- Host port interface (HPI) connector
- On Board FPGA (Actel's ProASIC 3) for DSP boot-strapping and NAND Flash interface
- On-Board XDS100 type Emulation using USB 2.0 interface[1]
- TI 60-Pin JTAG header to support External Emulator[1]
- High Speed plugged XDS560v2 Mezzanine Emulator[2]
- MMC interface for IPMI
- AMC like form factor

**Note: [1] - Available in TMDSEVM6472 only**
**[2] - Available in TMDSEVM6472LE only**

## 1.2 Functional Overview

The C6472 EVM is a single width AMC module with Texas Instruments' six core C6472 DSP, working as a bridge between circuit switched network (telecom serial interface ports) and packet switched network (Ethernet). Alternatively, it can be used for voice or video transcoding solely through the Ethernet interfaces.

The functional block diagram of TMDSEVM6472 is shown in figure 1.1:

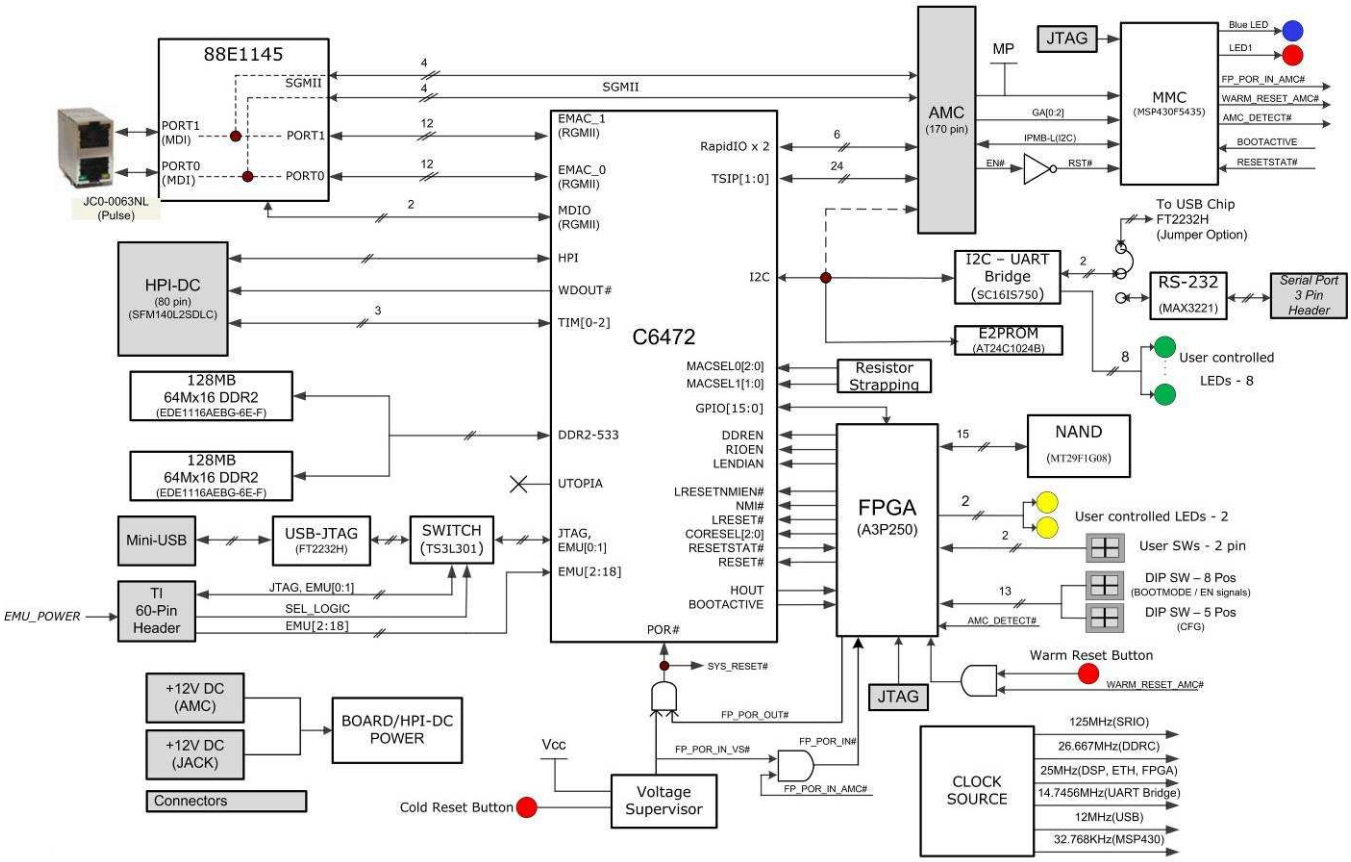


**Figure 1.1: Block Diagram of TMDSEVM6472**

The functional block diagram of TMDSEVM6472LE is shown in figure 1.2:

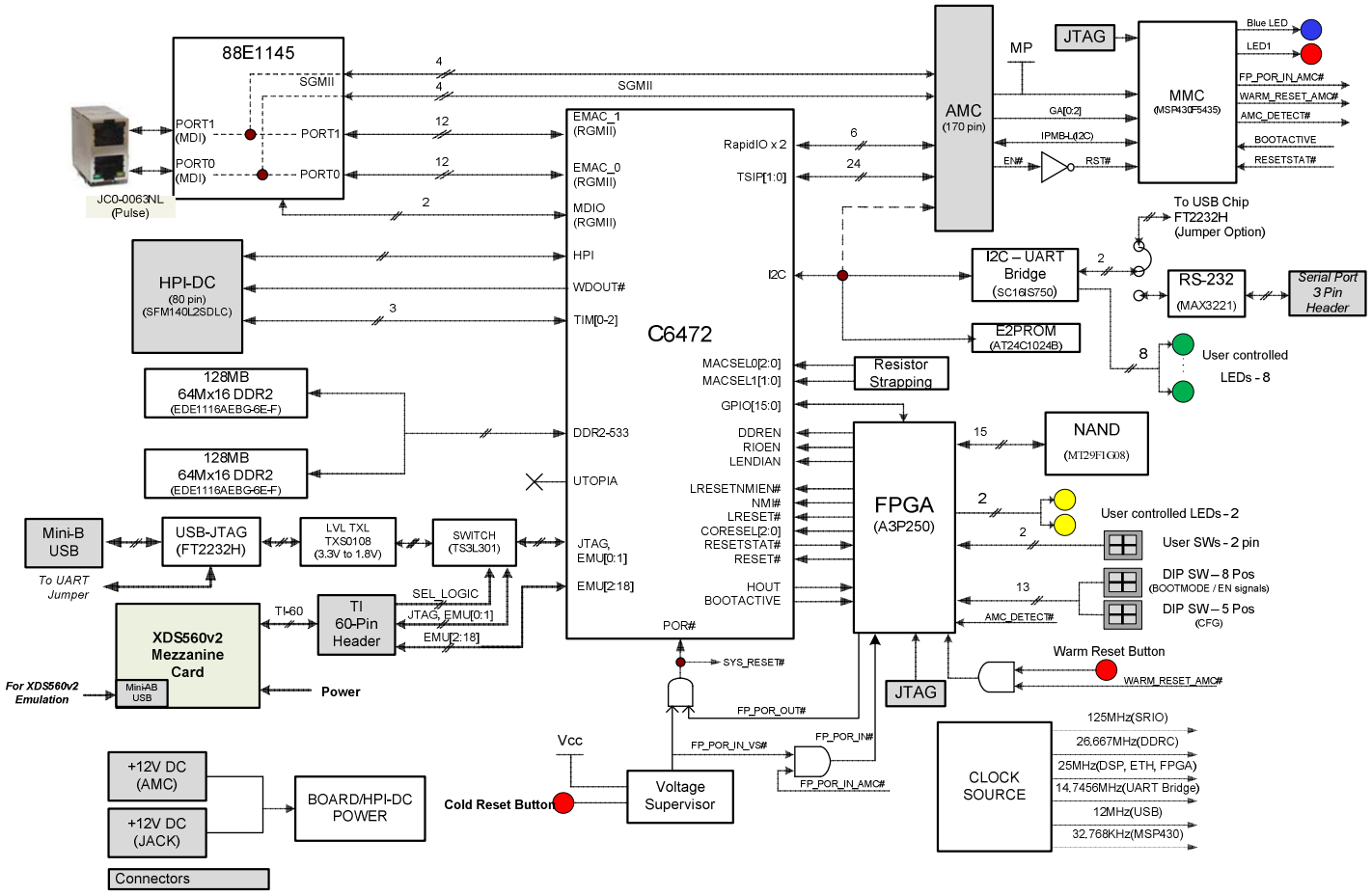


**Figure 1.2: Block Diagram of TMDSEVM6472LE**

## 1.3 Basic Operation

The C6472 EVM platform is designed to work with TI's Code Composer Studio version 4 (CCSv4) development environment and is shipped with the latest version with all necessary emulation drivers. For TMDSEVM6472, CCSv4 interfaces with the board via on-board emulation circuitry using the USB cable supplied along with this EVM or through external emulator. For TMDSEVM6472LE, CCSv4 interfaces with the board only via XDS560v2 System Trace emulator using the USB cable supplied.

To start operating the board, follow instructions in the Quick Setup Guide. Follow the instruction in BIOS MCSDK Getting Started Guide to install all the necessary development tools, drivers and documentation.

After the installation is completed, follow the steps below to run Code Composer Studio.

1. Power ON the board using power brick adaptor (12V/2.5A) supplied along with this EVM or insert this EVM board into standard AMC carrier back-plane.
2. Connect USB cable from host PC to EVM board for TMDSEVM6472 or to XDS560v2 Mezzanine emulator for TMDSEVM6472LE.
3. Launch Code Composer Studio from host PC by double clicking on its icon at PC desktop.

Detailed information about the EVM including examples and reference material is available in the DVD available with this package.

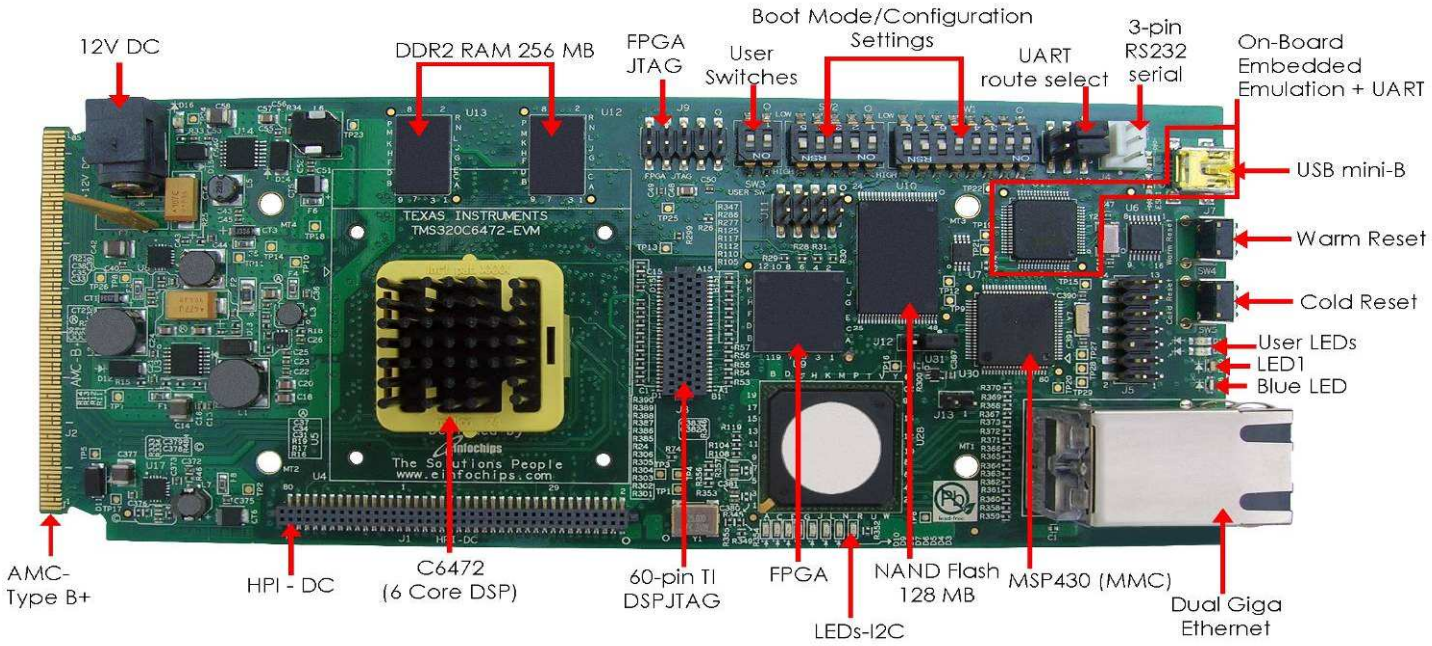


**Figure 1.3: TMDSEVM6472**

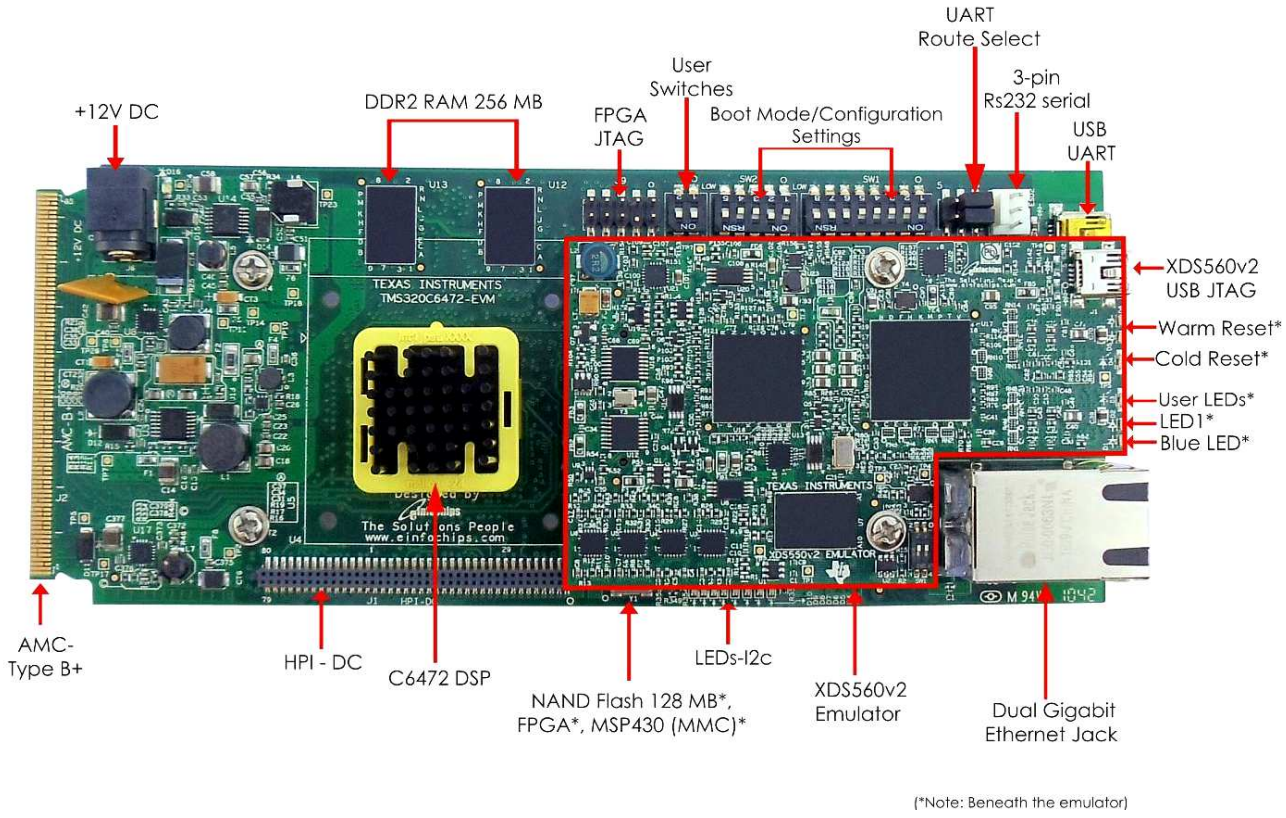


**Figure 1.4: TMDSEVM6472LE**

## 1.4 Boot Mode and Boot Configuration Switch Setting

The C6472 EVM has 15 sliding DIP switches (Board Ref. SW1, SW2 and SW3) to determine boot mode, boot configuration, endian mode, system clock out enable and DDR/SRIO interface enable options at every reset of the DSP.

## 1.5 Power Supply

The C6472 EVM can be powered from a single +12V / 2.5A DC (30W) external power supply connected to the DC power jack (J6). Internally, +12V input is converted into desired voltage levels such as, +5V, +3.3V, +1.8V, +1.5V and +1.2V using local DC-DC converters.

- +1.2V is used for DSP Core (CVDDx) and Ethernet PHY transceiver.
- +1.5V is used for FPGA core.
- +1.8V is used for DDR2 / Ethernet RGMII interface.
- +3.3V is used for DSP GPIOs.
- The DC power jack connector is a 2.5mm barrel-type plug with center-tip as positive polarity.

The C6472 EVM can also draw power from the AMC edge connector (J2). If the board is inserted into an AMC Carrier or AMC-compatible chassis, the external +12V supply from DC jack (J6) is not required and should not be connected in that case.

# 2. Introduction to the C6472 EVM Board

Chapter two provides an introduction and interface details for the C6472 EVM board. It contains:



## 2.1 Memory Map

The memory map of the TMS320C6472 device is as shown in Table 1. It provides a combined view of both local and global addresses. The C64x+ Megamodule local memories have both local and global addresses. The Megamodule registers have only local addresses which can be resolved within the Megamodule and cannot be accessed outside Megamodule. All other addresses listed in this table are global addresses which can be accessed from any bus master including all six C64x+ Megamodules, transfer controllers within the EDMA3 block and any peripheral that can master the bus.

**Table 1: TMS320C6472 Memory Map**

| Six Address Range | Memory Block Description |
|---|---|
| 0x 00000000 - 001FFFFF | Reserved |
| 0x 00200000 - 002BFFFF | SL2 RAM |
| 0x 002C0000 - 007FFFFF | Reserved |
| 0x 00800000 - 017FFFFF | Local L1 / L2 SRAM, Reserved |
| 0x 01800000 - 01BFFFFF | C64x+ Megamodule Registers |
| 0x 01C00000 - 0FFFFFFF | Control Registers, Reserved |
| 0x 10000000 - 1FFFFFFF | Global Memory Map, Reserved |
| 0x 20000000 - 77FFFFFF | Reserved |
| 0x 78000000 - DFFFFFFF | DDR2 EMIF Config, Reserved |
| 0x E0000000 - FFFFFFFF | CE0-CE1 DDR2 SDRAM |

## 2.2 EVM Boot mode and Boot Configuration Switch Settings

The C6472 EVM has two configuration switches SW1 and SW2. Whenever user presses a Cold or Warm Reset button or if the board is power-cycled, an on-board FPGA latches the state of configuration signals from SW1 and SW2 and presents them to the DSP during the reset period.

SW1 determines general DSP configuration, little or big endian mode, DDR interface enable and SRIO interface enable. SW2 determines DSP boot mode and system clock out enable options. Please refer to section 4.3 of this document for default switch setting and details of each switch.

## 2.3 Clock Configuration Options

Table below shows clock configuration information of the EVM.

**Table 2: Clock Configurations**

| Clock | Frequency | Description |
|---|---|---|
| CLKIN1 | 25.000MHz | CPU core clock input for PLL1, multiplier normally x20 for 500MHz, x25 for 625MHz and x28 for 700MHz |
| CLKIN2 | 25.000MHz | EMAC clock input for PLL2, multiplier fixed at x20 |
| CLKIN3 | 26.667MHz | DDR clock input for PLL3, multiplier fixed at x20 for DDR2-533 operation |

## 2.4 Board Revision ID

Board PCB (Printed Circuit Board) and PCA (Printed Circuit Assembly) revision are located below RJ-45 Jack in bottom silk, as shown in Figure 2.1. Table 3 describes the PCA/PCB revisions.

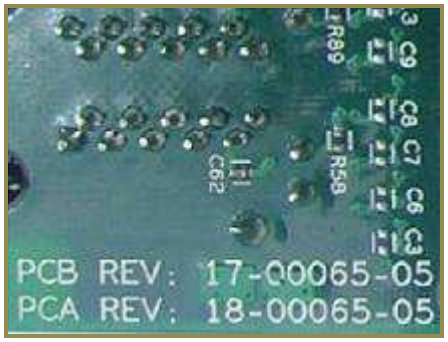


**Figure 2.1: EVM Board Revision**

**Table 3: PCA/PCB revision description**

| PCA REV | PCB REV | Description |
|---|---|---|
| 18-00065-01 | 17-00065-01 | Internal - Proto boards (Initial engineering samples) |
| 18-00065-02 | 17-00065-02 | Production build – Released in October-2009<br>- Modified TSIP connections to AMC edge connector<br>- Addition of Reset control from AMC carrier |
| 18-00065-03 | 17-00065-03 | Internal - Proto boards with Ethernet PHY changed to 88E1145 for SGMII feature addition |
| 18-00065-04 | 17-00065-04 | Production build – Released in March-2010<br>- Differential AMC Telecom clock input supported |
| 18-00065-05 | 17-00065-05 | Production build – Released in July-2010<br>- MMC and IPMI supported using TI MSP430 microcontroller |
| 18-00065-06 | 17-00065-06 | Production build – Released in December-2010<br>- TCLKC/D used for Frame Sync |

**Note:** Last two digits represent major PCB / PCA revision number.

## 2.5 JTAG - Emulation Overview

### 2.5.1 JTAG – TMDSEVM6472

The EVM supports two different types of DSP Emulation - “USB mini-B” and “60-pin TI JTAG-DSP”.

USB emulation is supported through an on-board, optimized XDS100-class embedded emulation circuit. On-board (embedded) USB emulation is accessible through the USB mini-B connector (J7); hence any external emulator is not necessary to connect EVM with Code Composer Studio. User can connect CCS with target DSP in EVM with USB cable supplied along with this board.

TI 60-pin JTAG header (J8) is provided on-board to allow user to connect to external emulator for high speed real-time emulation. External/mezzanine emulators as XDS560v2 emulators and standard XDS510 or XDS560 emulators with 60 to 20-pin or 60 to 14-pin adapter boards from TI and 3rd-party vendors are supported. Please refer to the documentation supplied with your emulator for connection assistance.

Both emulator configurations are enabled by default and there is dynamic switching between them. On-board embedded JTAG emulator is default connection to DSP, however when external emulator is connected to EVM, board circuitry automatically switches to give access to external emulator. When both are connected at the same time, external emulator is given priority and on-board emulator is disconnected from DSP.

The interface between DSP, on-board and external emulator is shown in figure below:

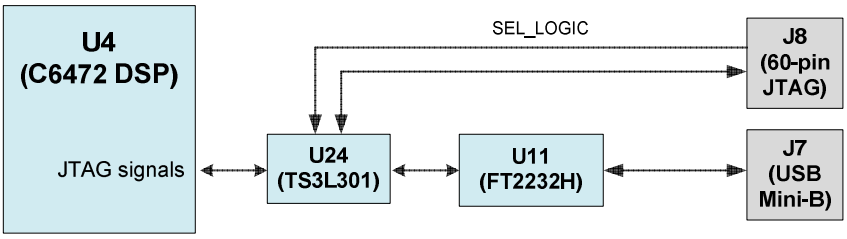


**Figure 2.2: TMDSEVM6472 JTAG emulation**

### 2.5.2 JTAG – TMDSEVM6472LE

In TMDSEVM6472LE, high speed real time emulation can be performed without needing an external emulator as it has an integrated, system trace capable XDS560v2 Mezzanine Emulator mounted on its TI 60-pin JTAG header (J3). User can connect the EVM to CCS by connecting the USB port of XDS560 Mezzanine emulator to PC using USB cable supplied with an EVM.

As high speed XDS560v2 Emulator is already mounted on TI 60-pin JTAG header of the EVM, the low speed XDS100 emulation is no longer required and not available to user.

It is important to note that for XDS560v2 emulation, the USB cable needs to be connected to the mini-AB connector (J1) on XDS560v2 Mezzanine Emulator and not to mini-B connector (J7) on the main board. For TMDSEVM6472LE, the mini-B connector (J7) on the main board can be used to access UART-over-USB; please refer to section 2.12 of this document for more details.

The interface between DSP and XDS560v2 Mezzanine Emulator is shown in figure 2.3:

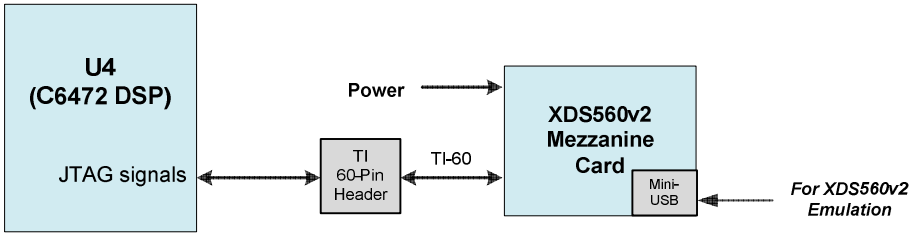


**Figure 2.3: TMDSEVM6472LE JTAG emulation**

#### 2.5.2.1 XDS560v2 Mezzanine Emulator Booting

When TMDSEVM6472LE is powered ON, the XDS560v2 Mezzanine Emulator starts booting. It takes approximately half minute to boot-up. The successful booting of XDS560v2 Mezzanine Emulator is indicated by following LED sequence:

- Green LED (D3) turns ON
- Yellow LED (D2) and Red LED (D1) turns ON
- Green LED (D3) blinks and turns OFF

After the completion of booting XDS560v2 mezzanine emulator is ready to interface with CCS. Once CCS is connected to the target DSP Green LED D4 turns ON.

The boot failure is indicated by simultaneous blinking of Red LED (D1), Yellow LED (D2) and Green LED (D3). In this case CCS can't be connected to XDS560v2 mezzanine emulator. The boot failure can happen when mezzanine emulator is attempted to mount over a non-compatible base EVM.

## 2.6 Clock Domains

The EVM incorporates variety of clocks to the TMS320C6472 device which are configured automatically during the power up configuration sequence. The figure below illustrates the clocking for the system in EVM module.

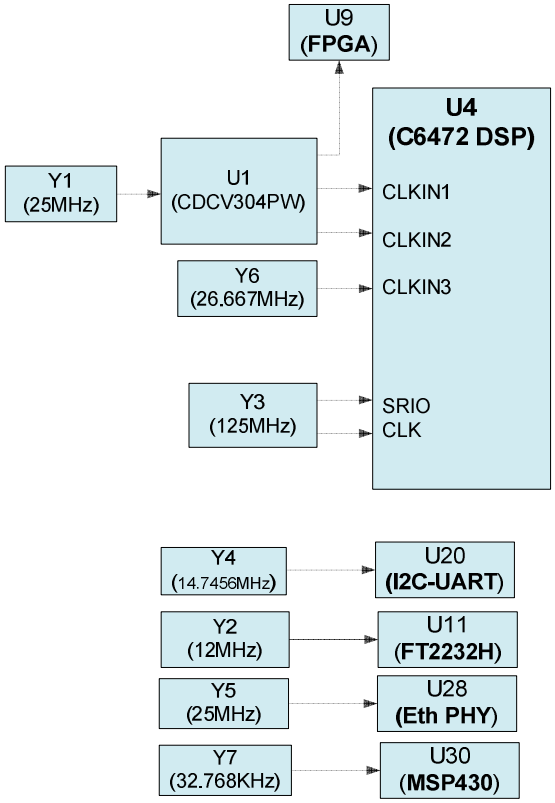


**Figure 2.4: C6472 EVM Clock Domains**

## 2.7 I2C Boot EEPROM

The I2C EEPROM address 0x50 contains Power on Self Test (POST) program and I2C address 0x51 contains second level boot-loader program. The second level boot-loader reads the Out-Of-Box Demo program from the NAND FLASH memory. The I2C address 0x51 also contains two unique MAC addresses reserved for your C6472 EVM. These MAC addresses are flashed into the EEPROM at address offset of 0xF400 to 0xF40B.

## 2.8 FPGA

The FPGA (Actel #A3P250-FGG144) interface provides reset control circuitry and latching of device configuration pins. The logic level of these pins is latched at reset to determine the device configuration. These switch-controlled inputs are driven to the DSP at reset time.

FPGA supports two modes; Normal mode and NAND pass through mode. These modes are mutually exclusive modes. In Normal mode, FPGA provides access to FPGA registers through DSP's GPIO pins. FPGA supports 2 user LEDs and 3 User Switches through control registers.

In NAND pass through mode, DSP GPIOs are directly assigned to NAND pins. NAND access is only possible in NAND pass through mode. Details of these are provided in chapter 3 FPGA Functional Specification.

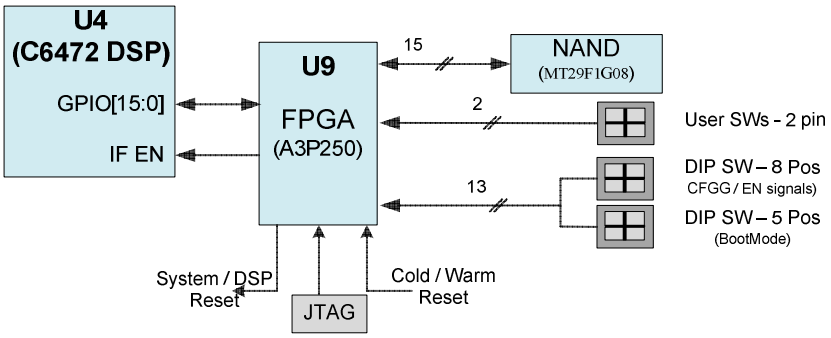


**Figure 2.5: C6472 EVM FPGA Connections**

## 2.9 Gigabit Ethernet PHY

The C6472 EVM incorporates a quad-port Marvell 88E1145 Ethernet PHY transceiver. The DSP can configure PHY (U28) over MDIO interface. Dual (stacked) port RJ45 connector (J3) allows Gigabit Ethernet access to the EMAC0 and EMAC1 ports of the DSP. Both EMAC0 (lower port) and EMAC1 (upper port) on the DSP are configured to use RGMII interface with their common MDIO interface. The Ethernet PHY has the ability to convert RGMII EMAC to SGMII EMAC; the converted SGMII EMAC ports are routed to the AMC connector.

The C6472 EVM is interfaced with PHY as shown in figure below.

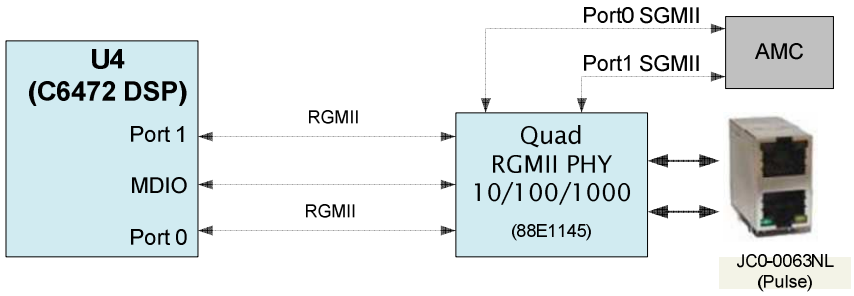


**Figure 2.6: C6472 EVM Ethernet PHY Routing**

At Power On, Port0 of Ethernet PHY will be configured as "RGMII to SGMII" mode and Port1 will configured as "RGMII to Copper" mode. This will be ensured by hardware strapping of Ethernet PHY. After DSP boot-up, user has the flexibility to change above configuration by re-configuring the drivers. The POST program when executed, will determine if the board is installed in an AMC connector and accordingly it will configure both EMAC ports to AMC connector or to RJ45 connector.

## 2.10 TSIP Interface

TMS320C6472 has three independent Telecom Serial Interface Ports (TSIP[0:2]). TSIP is a multi-link serial interface consisting of a maximum of 8 transmit data signals (or links), 8 receive data signals (or links), two frame sync input signals, and two serial clock inputs. The TSIP module in DSP offers support for a maximum of 1024 timeslots for transmit and receive. Typically, 672 timeslots for transmit and receive are utilized on these links. TSIP module can be configured to use frame sync signals and serial clocks as redundant sources for all transmit and receive data signals, or one frame sync and one serial clock can be configured for transmit and the other frame sync and clock can be configured for receive.

In C6472 EVM, two TSIP ports (TSIP0 and TSIP1) are routed to AMC edge connector. Four active links from each of TSIP0 and TSIP1 ports are routed to AMC edge connector. Below is the interface diagram for TSIP signals in The C6472 EVM.

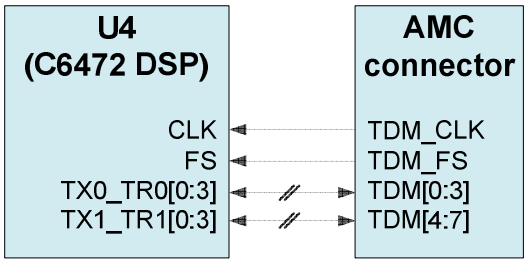


**Figure 2.7: C6472 EVM TSIP Connections**

## 2.11 Serial RapidIO (SRIO) Interface

TMS320C6472 supports high speed SERDES based Serial RapidIO (SRIO) interface. There are two independent x1 SRIO interfaces: Lane 0 and Lane 1 available on C6472. All SRIO ports are routed to AMC edge connector on board as per the PICMG AMC.0 R2.0 specifications; SRIO ports 1-2 are routed to AMC ports 8-9 respectively. Below figure shows RapidIO connections between the DSP and AMC edge connector.

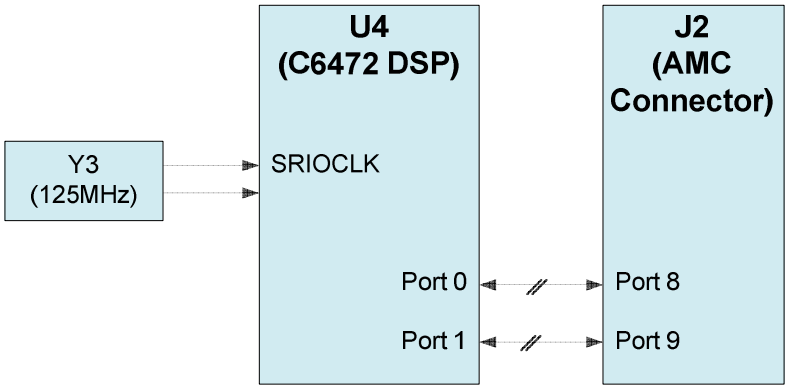


**Figure 2.8: C6472 EVM SRIO Port Connections**

## 2.12 UART Interface

A serial port is provided for debugging purpose using an I2C-UART bridge. This serial port can be accessed either through USB connector (J7) or through 3-pin serial port header (J4). The selection can be made through UART Route Select shunt J10 as follows:

- UART over USB Connector (Default): Shunt installed over J10.3-J10.1 and J10.4 -J10.2
- UART over 3-Pin Header J5 - Shunt installed over J10.3-J10.5 and J10.4 -J10.6

A 3-pin to 9-pin DTE (Data Terminal Equipment) serial cable is provided in the EVM kit to connect the J4 serial port to PC. An additional UART port is also routed from I2C-UART Bridge to 80 pin header J1.

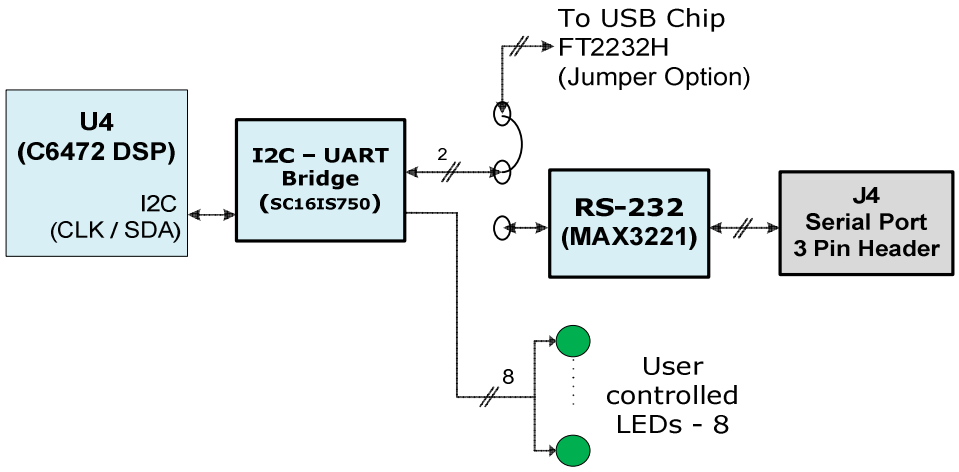


**Figure 2.9: C6472 EVM UART Connections**

## 2.13 Module Management Controller (MMC) for IPMI

The C6472 EVM supports limited set of Intelligent Platform Management Interface (IPMI) commands and a Module Management Controller (MMC) in AMC form-factor design.

The MMC will communicate with MicroTCA Carrier Hub (MCH) over IPMB (Intelligent Platform Management Bus) when inserted into an AMC slot of a PICMG® MTCA.0 Micro Telecommunications Computing Architecture (MicroTCA.0) specification compliant chassis. The primary purpose of the MMC is to provide necessary information to MCH, to enable the payload power to the C6472 EVM when it is inserted into the µTCA chassis.

The EVM also support a Blue LED and LED1 on the front panel as specified in PICMG® AMC.0 R2.0 Advanced Mezzanine Card Base Specification. Both of these LEDs will blink as part of initialization process when the MMC will receive management power.

Blue LED – Blue LED will turn ON when µTCA chassis is powered ON and an EVM is inserted into it. The blue LED will turn OFF when payload power is enabled to the EVM by the MCH.

LED1 – Red colored LED1 will normally be OFF. It will turn ON to provide basic feedback about failures and out of service.

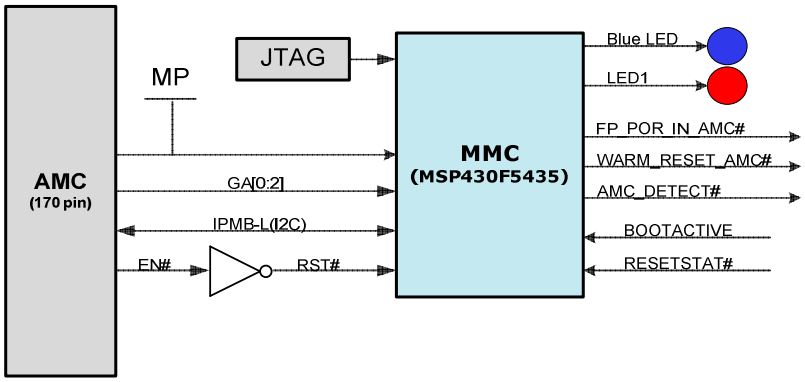


**Figure 2.10: C6472 EVM MMC Connections for IPMI**

## 2.14 HPI

The C6472 EVM has an HPI interface, which can be accessed by an external host controller. This HPI interface is available on the HPI Daughter Card (DC) connector J1 of the EVM.

# 3. FPGA Functional Specification

This chapter contains:



## 3.1 FPGA modes

The FPGA can be configured in two modes. They are:

- Normal mode
- NAND pass through mode

After the completion of booting, DSP GPIO 14 is used to select between the Normal mode and the NAND Pass through mode.

If DSP GPIO 14 is 1'b0, then normal mode is selected. FPGA registers can be accessed in normal mode of operation only.

If DSP GPIO 14 is 1'b1, then Pass-Through mode is selected. In this mode DSP GPIO pins are directly mapped to the pins of the NAND Flash memory except Write-Protect Pin. The Write-Protect pin is not mapped due to unavailability of a GPIO pin in NAND pass through mode. The Write-Protect Pin of NAND Flash is mapped to the bit [4] of NAND_CWR_REGH FPGA register. The user application will require to disable write protect using the FPGA normal mode and then switch to NAND pass through mode to write to the NAND flash.

## 3.2 FPGA – DSP Communication Signals

The GPIO signals used for communication between FPGA and DSP when FPGA is in Normal mode are described in Table 4. The GP[12:13] are not used.

**Table 4: GPIO pin mapping in Normal mode**

| GPIO# | Function | Direction | Description |
|---|---|---|---|
| GP[7:0] | Data | Bidirectional | This is 8-bit wide bidirectional bus, shared for address and data. Whether the signals currently carry address, read data, or write data is defined by the Command signals. |
| GP[9:8] | Command | Input | These bits define the bus operation for the current strobe period.<br>00 - NOP<br>01 - address cycle<br>10 - read cycle<br>11 - write cycle |
| GP10 | Strobe | Input | This signal is used to synchronize the bus activity between the DSP and FPGA. The DSP is always master of the bus timing. |
| GP11 | Ready | Output | A low value on this pins during a read or write cycle will cause the DSP to extend the cycle until the signal goes high. This signal is not monitored for address and NOP cycles |
| GP14 | FPGA mode select | Input | This signal selects the mode of communication with the NAND Flash Memory. If it is 1'b1, then pass-through mode is enabled whereby the DSP GPIO pins are directly mapped to the pins of NAND Flash Memory. If it is 1'b0, then Normal Mode of operation is selected in which FPGA Configuration Registers will be accessed. |
| GP 15 | I2c-UART interrupt | Output | This signal directly follows the IRQ line from the I2C UART chip |

The GPIO signals used for communication between FPGA and DSP when FPGA is used in NAND pass through mode are described in Table 5.

**Table 5: GPIO pin mapping in NAND pass through mode**

| GPIO# | Function | Direction | Description |
|---|---|---|---|
| GP[7:0] | Data | Bidirectional | This 8-bit data bus is mapped to the 8-bit data bus of NAND Flash Memory. |
| GP[9:8] | Command | Input | GP[8] pin is mapped to the Command Latch Enable (CLE) pin of NAND Flash Memory.<br>GP[9] pin is mapped to the Address Latch Enable (ALE) pin of NAND Flash Memory. |
| GP10 | Write enable | Input | This signal is mapped to the Write Enable (nWE) pin of the NAND Flash Memory. |
| GP11 | Ready | Output | This signal is mapped to the Ready/Busy (RB) pin of the NAND Flash Memory. |
| GP12 | Read enable | Input | This signal is mapped to the Read Enable (nRE) pin of the NAND Flash Memory. |
| GP13 | Chip enable | Input | This signal is mapped to the Chip Enable (nCE) pin of the NAND Flash Memory. |
| GP14 | FPGA mode select | Input | This signal selects the mode of communication with the NAND Flash Memory. If it is 1'b1, then pass-through mode is enabled whereby the DSP GPIO pins are directly mapped to the pins of NAND Flash Memory. If it is 1'b0, then Normal Mode of operation is selected in which FPGA Configuration Registers will be accessed. |
| GP 15 | I2c-UART interrupt | Output | This signal directly follows the IRQ line from the I2C UART chip |

## 3.3 FPGA Memory Map

Table 6 describes the memory map of FPGA when FPGA is configured in Normal mode of operation.

**Table 6: FPGA Memory Map**

| GPIO[7:0] | Memory |
|---|---|
| 0x00 – 0x22 | Configuration Memory Space |

## 3.4 FPGA Configuration Registers

The following table enlists the FPGA configuration register and its description:

**Table 7: FPGA Configuration Registers Set**

| Name | Address | Read / Write | Default value in HEX | Data bits | Description |
|---|---|---|---|---|---|
| Reserved | 0x00 - 0x05 | - | - | 7:0 | Reserved for future use. |
| BITFILE_VER_REG | 0x06 | Read | 0x01 | 7:0 | Shows the BITFILE version |
| RTL_VER_REG | 0x07 | Read | 0x01 | 7:0 | Shows the RTL version |
| - | 0x08 | - | 0x00 | 7:0 | Reserved for future use. |
| CONTROL_REGH | 0x09 | Read / Write | 0x70 | 3:0 | Reserved for future use. |
| | | | | 4 | Write Protect Bit<br>1 => Disable<br>0 => Enable<br>This bit is mapped to the Write-Protect pin of NAND Flash Memory if the Pass-Through Mode is enabled. |
| | | | | 5 | User LED 0 Data. The bit value that is written at this location is driven on the User LED 0, if the User LED is enabled via NAND_CWR_REGH[7]. |
| | | | | 6 | User LED 1 Data. The bit value that is written at this location is driven on the User LED 1, if the User LED is enabled via NAND_CWR_REGH[7]. |
| | | | | 7 | User LED's Enable/Disable<br>0 => FPGA drives 1'b1 on User LED's (Disable).<br>1 => Data present in the NAND_CWR_REGH[6:5] is driven on the User LED's (Enable). |
| Reserved | 0x0A – 0x21 | - | - | 7:0 | Reserved for future use. (RFU) |
| USER_SW_REG | 0x22 | Read | 0x00 | 0 | tievm_user_sw1_i |
| | | | | 1 | tievm_user_sw2_i |
| | | | | 2 | AMC detect signal |
| | | | | 4:3 | Reserved for future use |
| | | | | 7:5 | tievm_board_ver_i[2:0] |

## 3.5 FPGA-DSP Communication Protocol in FPGA Normal Mode

At system reset FPGA becomes master and DSP becomes slave. The FPGA will provide the boot parameters to DSP. Once booting is done the FPGA will become slave and DSP will become master, at this point the below mentioned protocol is implemented.

The 16 bit bus from DSP GPIO to FPGA is divided in

- 8-bit bi-directional bus which is shared between data and address.
- 4-bit for control and handshaking signals.
- 2-bits are not used.

DSP to FPGA has strobe based asynchronous communication.

After the DSP reset and boot sequence the GPIO pins will transition from their configuration role to their role in the GPIO Bus.

The DSP is the master of the GPIO BUS. The DSP will initiate bus cycles, define how long they last and when they will complete. The FPGA can extend a read or write cycle if needed.

The normal write sequence is for the DSP to issue an address cycle followed by a write cycle. The normal read sequence is for the DSP to issue an address cycles followed by a read cycle. If a read or write cycle is not preceded by an address cycle, the address of the last cycle is used. This allows repeated reads or writes to a given register.

To initiate an address cycle the DSP will:

1. Set the value of cmd
2. Set the direction of data_io as output from DSP
3. Set the address value on data_io
4. Set stb_o active
5. Wait a minimum of 50 ns
6. Set stb_o inactive
7. Wait a minimum of 50 ns before the next cycle starts

**Procedure 3-1: Address cycle Initiation by DSP**

To initiate a write cycle the DSP will:

1. Set the value of cmd
2. Set the direction of data_io as output from DSP
3. Set the write data value on data_io
4. Set stb_o active
5. Wait a minimum of 50 ns
6. If rdy_o is low wait until it is high
7. Set stb_o inactive
8. Wait a minimum of 50 ns before the next cycle starts

**Procedure 3-2: Write cycle Initiation by DSP**

To initiate a read cycle the DSP will:

1. Set the value of cmd
2. Set the direction of data_io as input to DSP
3. Set stb_o active
4. Wait a minimum of 50 ns
5. If rdy_o is low wait until it is high
6. read data_io and store as the read cycle result
7. Set stb_o inactive
8. Wait a minimum of 50 ns before the next cycle starts

**Procedure 3.5-3: Read Cycle Initiation by DSP**

The FPGA will only enable its data_io drive when cmd == READ and stb_o is active. The FPGA must ensure that its driver is off no later than 40 ns after stb_o goes inactive.

The bus may idle after any of the above cycles; an explicit NOP cycle is not needed

## 3.6 Sequence of Operation

Following section provides details of FPGA sequence of operation.

### 3.6.1 Boot Sequence – Power-On (Cold) Reset

1. On system reset (power-on reset), available through the global FPGA system reset pin, assert POR# pin active low
2. Wait for the FPGA internal PLL to stabilize
1. Once the PLL is locked, user defined configuration pins and fixed configuration pins are latched by FPGA and pin status are provided to C6472 device configuration pins. For device configuration settings please refer to sections 4.3.1 DSP Configurations and 4.3.2 DSP boot mode.
3. Wait for 20 µS. As the frequency of operation of the FPGA is 40MHz, the internal counters would count 800 clock cycles
4. De-assert POR#
5. Wait for RESETSTAT# signal from DSP to go from low to high. GPIO lines to GIC modules would be put in tri-state condition
6. Indicate GIC module that the boot mode is over

**Procedure 3-1: Power on Reset**

### 3.6.2 Boot Sequence – Warm Reset

2. On warm reset, available through the push button switches on board, assert RESET# pin active low
3. Wait for the FPGA internal PLL to stabilize
4. Once the PLL is locked, user defined configuration pins and fixed configuration pins are latched by FPGA and pin status are provided to C6472 device configuration pins. For device configuration settings please refer to sections 4.3.1 DSP Configurations and 4.3.2 DSP boot mode.
5. Wait for 20 µS. As the frequency of operation of the FPGA is 40MHz, the internal counters would count 800 clock cycles
6. De-assert RESET#
7. Wait for RESETSTAT# signal from DSP to go from low to high. GPIO lines to GIC modules would be put in tri-state condition
8. Indicate GIC module that the boot mode is over

**Procedure 3-1: Warm Reset**

# 4. EVM Board Physical Specifications

This chapter describes the physical layout of the C6472 EVM board and its connectors, switches and test points. It contains:



## 4.1 Board Layout

The C6472 EVM Board is a 7.11” x 2.89” (180.6 x 73.5 mm2) multi-layer board which is powered through connector J6. Figure 3-1 and 3-2 shows the layout of the C6472 EVM Board.

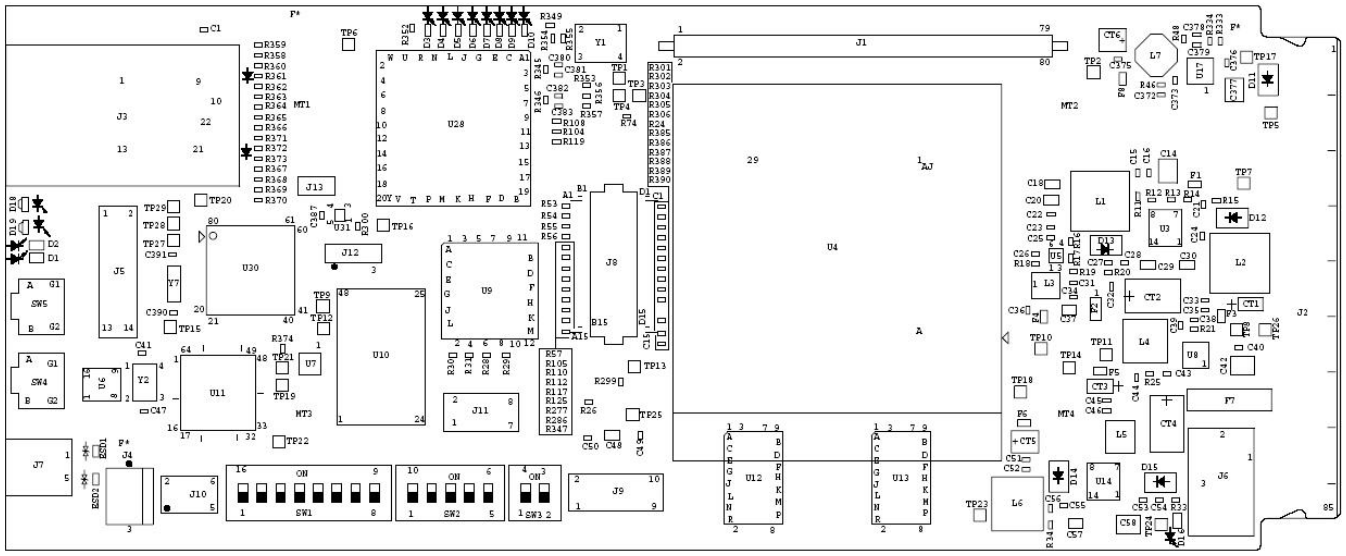

**Figure 4.1: C6472 EVM Board layout – TOP view**

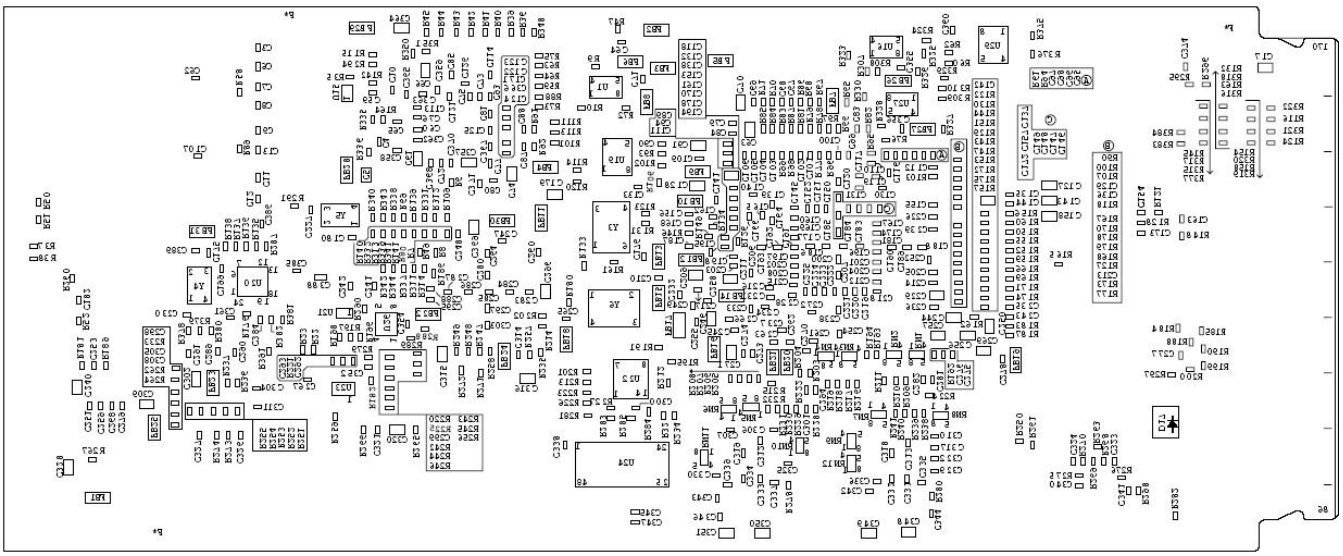

**Figure 4.2: C6472 EVM Board layout – Bottom view**

## 4.2 Connector Index

The C6472 EVM board has several connectors which provide access to various interfaces on the board.

**Table 8: TMS320C6472 EVM Board Connectors**

| Connector | Pins | Function |
|---|---|---|
| J1 | 80 | HPI DC Connector |
| J2 | 170 | AMC Edge Connector |
| J3 | 28 | Ethernet Connector |
| J4 | 3 | UART 3-Pin Connector |
| J5 | 14 | MSP430 JTAG Connector |
| J6 | 3 | Power Input Jack Connector |
| J7 | 5 | Mini-B USB Connector |
| J8 | 60 | TI 60-Pin DSP JTAG Connector [3] |
| J9 | 10 | FPGA JTAG Connector |
| J10 | 6 | UART Path Select Connector |
| J1 | 5 | Mini-AB USB Connector [4] |

**Note: [3] – Not Available in TMDSEVM6472LE.**
**[4] – Present on XDS5602v2 Mezzanine Card. Available in TMDSEVM6472LE only.**

### 4.2.1 J1, HPI DC Connector

Connector J1 provides the HPI Interface of the DSP to an external host. The signals on this connector are shown in the table below. This connector is identical to the HPI connector implemented on previous AMC EVMs of TI, so that any previous test fixtures will connect without revision. The signals on this connector are shown in the table below.

**Table 9: HPI DC Connector**

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | VCC5 | +5V Power | 2 | VCC3.3 | +3.3V Power |
| 3 | GND | Ground Signal | 4 | VCC3.3 | +3.3V Power |
| 5 | VCC5 | +5V Power | 6 | VCC1.8 | +1.8V Power |
| 7 | GND | Ground Signal | 8 | GND | Ground Signal |
| 9 | HPI_D1 | Data Signal - 1 | 10 | VCC1.8 | +1.8V Power |
| 11 | HPI_D3 | Data Signal – 3 | 12 | HPI_D0 | Data Signal – 0 |
| 13 | HPI_D5 | Data Signal – 5 | 14 | HPI_D2 | Data Signal – 2 |
| 15 | HPI_D7 | Data Signal – 7 | 16 | HPI_D4 | Data Signal – 4 |
| 17 | GND | Ground Signal | 18 | HPI_D6 | Data Signal – 6 |
| 19 | HPI_D9 | Data Signal – 9 | 20 | GND | Ground Signal |
| 21 | HPI_D11 | Data Signal - 11 | 22 | HPI_D8 | Data Signal – 8 |
| 23 | HPI_D13 | Data Signal – 13 | 24 | HPI_D10 | Data Signal – 10 |
| 25 | HPI_D15 | Data Signal - 15 | 26 | HPI_D12 | Data Signal – 12 |
| 27 | GND | Ground Signal | 28 | HPI_D14 | Data Signal - 14 |
| 29 | HPI_DS2# | Data Strobe - 2 | 30 | GND | Ground Signal |
| 31 | GND | Ground Signal | 32 | HPI_HAS# | |
| 33 | HPI_DS1# | Data Strobe - 1 | 34 | GND | Ground Signal |
| 35 | GND | Ground Signal | 36 | HPI_CNTL0 | Control Select 0 |
| 37 | HPI_CS | Chip Select | 38 | GND | Ground Signal |
| 39 | GND | Ground Signal | 40 | NC | |
| 41 | HPI_CNTL1 | Control Select 1 | 42 | GND | Ground Signal |
| 43 | GND | Ground Signal | 44 | HPI_INT | Interrupt |
| 45 | HPI_RDY# | Ready indication | 46 | GND | Ground Signal |
| 47 | GND | Ground Signal | 48 | NC | |
| 49 | HPI_RW# | Read / Write select | 50 | NC | |
| 51 | NC | | 52 | NC | |
| 53 | NC | | 54 | NC | |
| 55 | NC | | 56 | GND | Ground Signal |
| 57 | NC | | 58 | NC | |
| 59 | NC | | 60 | NC | |
| 61 | GND | Ground Signal | 62 | NC | |
| 63 | NC | | 64 | NC | |
| 65 | NC | | 66 | NC | |
| 67 | NC | | 68 | TIMI0 | Timer Input |
| 69 | NC | | 70 | GND | Ground Signal |
| 71 | GND | Ground Signal | 72 | TIMI1 | Timer Input |
| 73 | WDOUT# | Watchdog timer output | 74 | GND | Ground Signal |
| 75 | GND | Ground Signal | 76 | TIMO2 | Timer Output |
| 77 | HPI_HWIL | Half Word Select | 78 | GND | Ground Signal |
| 79 | GND | Ground Signal | 80 | NC | |

### 4.2.2 J2, AMC Edge Connector

The J2 card edge connector plugs into an AMC compatible carrier board and provides a high speed Serial RapidIO, TSIP and I2C interfaces to the carrier board. This connector is the 170 pin B+ style. The pin out for the connector is shown in the figure below.

**Table 10: AMC Edge Connector**

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | GND | Ground Signal | 170 | GND | Ground Signal |
| 2 | VCC12 | +12V Power | 169 | NC | |
| 3 | PS1# | Presence 1 | 168 | NC | |
| 4 | MP | Management Power | 167 | NC | |
| 5 | GA0 | Geographic Address 0 | 166 | NC | |
| 6 | NC | | 165 | NC | |
| 7 | GND | Ground Signal | 164 | GND | Ground Signal |
| 8 | NC | | 163 | NC | |
| 9 | VCC12 | +12V Power | 162 | NC | |
| 10 | GND | Ground Signal | 161 | GND | Ground Signal |
| 11 | P0_SG_OUT_P | | 160 | NC | |
| 12 | P0_SG_OUT_M | | 159 | NC | |
| 13 | GND | Ground Signal | 158 | GND | Ground Signal |
| 14 | P0_SG_IN_P | | 157 | NC | |
| 15 | P0_SG_IN_M | | 156 | NC | |
| 16 | GND | Ground Signal | 155 | GND | Ground Signal |
| 17 | GA1 | Geographic Address 1 | 154 | NC | |
| 18 | VCC12 | +12V Power | 153 | NC | |
| 19 | GND | Ground Signal | 152 | GND | Ground Signal |
| 20 | P1_SG_OUT_P | | 151 | NC | |
| 21 | P1_SG_OUT_M | | 150 | NC | |
| 22 | GND | Ground Signal | 149 | GND | Ground Signal |
| 23 | P1_SG_IN_P | | 148 | NC | |
| 24 | P1_SG_IN_M | | 147 | NC | |
| 25 | GND | Ground Signal | 146 | GND | Ground Signal |
| 26 | GA2 | Geographic Address 2 | 145 | NC | |
| 27 | VCC12 | +12V Power | 144 | NC | |
| 28 | GND | Ground Signal | 143 | GND | Ground Signal |
| 29 | NC | | 142 | NC | |
| 30 | NC | | 141 | NC | |
| 31 | GND | Ground Signal | 140 | GND | Ground Signal |
| 32 | NC | | 139 | NC | |
| 33 | NC | | 138 | NC | |
| 34 | GND | Ground Signal | 137 | GND | Ground Signal |
| 35 | NC | | 136 | NC | |
| 36 | NC | | 135 | NC | |
| 37 | GND | Ground Signal | 134 | GND | Ground Signal |

| | | | | | |
|---|---|---|---|---|---|
| 38 | NC | | 133 | NC | |
| 39 | NC | | 132 | NC | |
| 40 | GND | Ground Signal | 131 | GND | Ground Signal |
| 41 | ENABLE# | Enable Signal | 130 | I2C_SDA | I2C_SDA |
| 42 | VCC12 | +12V Power | 129 | I2C_SCL | I2C_SCL |
| 43 | GND | Ground Signal | 128 | GND | Ground Signal |
| 44 | NC | | 127 | NC | |
| 45 | NC | | 126 | NC | |
| 46 | GND | Ground Signal | 125 | GND | Ground Signal |
| 47 | NC | | 124 | TDM_FS | TDM_FS_ALT |
| 48 | NC | | 123 | TDM_CLK | TDM_CLK_ALT |
| 49 | GND | Ground Signal | 122 | GND | Ground Signal |
| 50 | NC | | 121 | TDM7 | TSIP1_TX3/RX1 |
| 51 | NC | | 120 | TDM6 | TSIP1_TX1/RX3 |
| 52 | GND | Ground Signal | 119 | GND | Ground Signal |
| 53 | NC | | 118 | TDM5 | TSIP1_TX2/RX0 |
| 54 | NC | | 117 | TDM4 | TSIP1_TX0/RX2 |
| 55 | GND | Ground Signal | 116 | GND | Ground Signal |
| 56 | SCL_IPMB | | 115 | TDM3 | TSIP0_TX3/RX1 |
| 57 | VCC12 | +12V Power | 114 | TDM2 | TSIP0_TX1/RX3 |
| 58 | GND | Ground Signal | 113 | GND | Ground Signal |
| 59 | NC | | 112 | TDM1 | TSIP0_TX2/RX0 |
| 60 | NC | | 111 | TDM0 | TSIP0_TX0/RX2 |
| 61 | GND | Ground Signal | 110 | GND | Ground Signal |
| 62 | NC | | 109 | NC | |
| 63 | NC | | 108 | NC | |
| 64 | GND | Ground Signal | 107 | GND | Ground Signal |
| 65 | NC | | 106 | NC | |
| 66 | NC | | 105 | NC | |
| 67 | GND | Ground Signal | 104 | GND | Ground Signal |
| 68 | NC | | 103 | NC | |
| 69 | NC | | 102 | NC | |
| 70 | GND | Ground Signal | 101 | GND | Ground Signal |
| 71 | SDA_IPMB | | 100 | NC | |
| 72 | VCC12 | +12V Power | 99 | NC | |
| 73 | GND | Ground Signal | 98 | GND | Ground Signal |
| 74 | TDM_CLK_P | TSIP Clock A | 97 | RIOTX_P1 | SRIO Port 1-TX |
| 75 | TDM_CLK_N | | 96 | RIOTX_N1 | SRIO Port 1-TX |
| 76 | GND | Ground Signal | 95 | GND | Ground Signal |
| 77 | TDM_FS_P | TSIP Clock B | 94 | RIORX_P1 | SRIO Port 1-RX |
| 78 | TDM_FS_N | | 93 | RIORX_N1 | SRIO Port 1-RX |
| 79 | GND | Ground Signal | 92 | GND | Ground Signal |
| 80 | NC | | 91 | RIOTX_P0 | SRIO Port 0-TX |
| 81 | NC | | 90 | RIOTX_N0 | SRIO Port 0-TX |
| 82 | GND | Ground Signal | 89 | GND | Ground Signal |
| 83 | PS0# | Presence 0 | 88 | RIORX_P0 | SRIO Port 0-RX |
| 84 | VCC12 | +12V Power | 87 | RIORX_N0 | SRIO Port 0-RX |
| 85 | GND | Ground Signal | 86 | GND | Ground Signal |

### 4.2.3 J3, Ethernet Connector

J3 is vertically stacked dual gigabit Ethernet connector with integrated magnetics. It is driven from the 88E1121 Marvell PHY device. The pin out for this connector is shown in the table below.

**Table 11: Ethernet Connector pin out**

| Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|
| 1 | Port 0 – MD0+ | 13 | Port 1 – MD0+ |
| 2 | Port 0 – MD0- | 14 | Port 1 – MD0- |
| 3 | Port 0 – MD1+ | 15 | Port 1 – MD1+ |
| 4 | Port 0 – MD1- | 16 | Port 1 – MD1- |
| 5 | Port 0 – MD2+ | 17 | Port 1 – MD2+ |
| 6 | Port 0 – MD2- | 18 | Port 1 – MD2- |
| 7 | Port 0 – MD3+ | 19 | Port 1 – MD3+ |
| 8 | Port 0 – MD3- | 20 | Port 1 – MD3- |
| 9 | VCC1.8 | 21 | VCC1.8 |
| 10 | Ground | 22 | Ground |
| 11 | Port 0 – LED+ | 23 | Port 1 – LED+ |
| 12 | Port 0 – LED- | 24 | Port 1 – LED- |

### 4.2.4 J4, UART 3-Pin Connector

J5 is 3-pin male connector for RS232 serial interface. A 3-Pin female to 9-Pin DTE female cable will be needed to connect this to a PC. The pin out for the connector is shown in the figure below.

**Table 12: UART Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | Ground |
| 2 | Transmit |
| 3 | Receive |

### 4.2.5 J5, MSP430 JTAG Connector

J5 is a 14 pin JTAG connector for MSP430 only. The pin out for the connector is shown in the figure below.

**Table 13: MSP430 JTAG Connector pin out**

| Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|
| 1 | TDO | 8 | TEST |
| 2 | NC | 9 | NC |
| 3 | TDI | 10 | RESET# |
| 4 | VCC | 11 | NC |
| 5 | TMS | 12 | NC |
| 6 | No Pin (**Key**) | 13 | NC |
| 7 | TCK | 14 | TDO |

### 4.2.6 J6, Power Input Jack Connector

J6 is a 3 pin, 2.5mm power jack with the center tip as positive polarity. Do NOT use this connector, if powering the board from the AMC carrier back-plane.

### 4.2.7 J7, Mini-USB Connector

In TMDSEVM6472, J7 is available to connect CCS with C6472 DSP using on-board XDS100 type emulation circuitry as well as to access UART-over-USB. In TMDSEVM6472LE, J7 is available for UART-over-USB only.

The pin out for the connector is shown in the table below.

**Table 14: Mini-B USB Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | VBUS |
| 2 | D- |
| 3 | D+ |
| 4 | ID |
| 5 | Ground |

### 4.2.8 J8, DSP JTAG Connector

J8 is a standard TI 60 pin JTAG connector for XDS560v2 Emulator. The onboard switch multiplexes this interface with the onboard emulation interface. When an external emulator is plugged into J8, the external emulator can connect with the DSP. The I/O voltage level on these pins is 3.3V. So any 3.3V compatible emulator can be used to interface to the C6472 device. Note, that when an external emulator is plugged into this connector (J8), the onboard emulation circuitry will be disabled. The pin out for the connector is shown in the figure below.

**Table 15: DSP JTAG Connector pin out**

| Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|
| B1 | ID0 | D1 | NC |
| A1 | Ground | C1 | ID2 |
| B2 | TMS | D2 | Ground |
| A2 | Ground | C2 | EMU18 |
| B3 | EMU17 | D3 | Ground |
| A3 | Ground | C3 | TRST |
| B4 | TDI | D4 | Ground |
| A4 | Ground | C4 | EMU16 |
| B5 | EMU14 | D5 | Ground |
| A5 | Ground | C5 | EMU15 |
| B6 | EMU12 | D6 | Ground |
| A6 | Ground | C6 | EMU13 |
| B7 | TDO | D7 | Ground |
| A7 | Ground | C7 | EMU11 |
| B8 | TVD | D8 | Type1 (Ground) |
| A8 | Type0 (NC) | C8 | TCLKRTN |
| B9 | EMU9 | D9 | Ground |
| A9 | Ground | C9 | EMU10 |
| B10 | EMU7 | D10 | Ground |
| A10 | Ground | C10 | EMU8 |
| B11 | EMU5 | D11 | Ground |
| A11 | Ground | C11 | EMU6 |
| B12 | TCLK | D12 | Ground |
| A12 | Ground | C12 | EMU4 |
| B13 | EMU2 | D13 | Ground |
| A13 | Ground | C13 | EMU3 |
| B14 | EMU0 | D14 | Ground |
| A14 | Ground | C14 | EMU1 |
| B15 | ID1 | D15 | Ground |
| A15 | TRGRSTz | C15 | ID3 |

### 4.2.9 J9, FPGA JTAG Connector

J9 is a 10 pin JTAG connector for FPGA only. The pin out for the connector is shown in the figure below.

**Table 16: FPGA JTAG Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | TCK |
| 2 | GND |
| 3 | TDO |
| 4 | NC |
| 5 | TMS |
| 6 | VJTAG |
| 7 | VPUMP |
| 8 | TRST# |
| 9 | TDI |
| 10 | GND |

### 4.2.10 J10, UART Path Select Connector

UART port can be accessed either through USB connector (J7) or through 3-pin serial port header (J5). The selection can be made through UART path select connector J10 as follows:

- UART over USB Connector (Default): Shunt installed over J10.3-J10.1 and J10.4 -J10.2
- UART over 3-Pin Header J4 - Shunt installed over J10.3-J10.5 and J10.4 -J10.6

The pin out for the connector is shown in the figure below.

**Table 17: UART Path Select Connector pin out**

| Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|
| 1 | FT2232 Transmit | 2 | FT2232 Receive |
| 3 | UART Transmit | 4 | UART Receive |
| 5 | MAX3221 Transmit | 6 | MAX3221 Receive |

### 4.2.11 J1, Mini-AB USB Connector – In TMDSEVM6472LE only

Mini-AB USB connector (J1) mounted on Mezzanine Card, is available to connect EVM to CCS for XDS560v2 type emulation. The pin out for the connector is shown in the table below.

**Table 18: Mini-AB USB Connector pin out**

| Pin # | Signal Name |
|---|---|
| 1 | VBUS |
| 2 | D- |
| 3 | D+ |
| 4 | ID |
| 5 | Ground |

## 4.3 Switches

The TMS320C6472 EVM Board has three DIP and two push button switches, namely SW1 to SW5. SW1 to SW3 are DIP switches and SW4 and SW5 are push button switches. The function of each of the switches is listed in the table below.

**Table 19: C6472 EVM Board Switches**

| Switch | Function |
|---|---|
| SW1 | DSP Configuration |
| SW2 | DSP Boot mode |
| SW3 | User switch |
| SW4 | Warm Reset |
| SW5 | Cold Reset |

### 4.3.1 SW1, DSP Configurations

SW1 is an 8 position DIP switch that is used for DSP configuration. A diagram of SW1 switch (with factory default settings) is shown below.

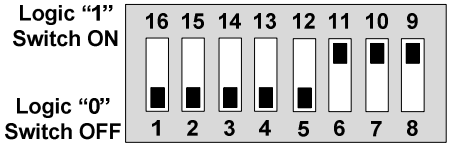


**Figure 4.3: SW1 default settings**

The following table describes the positions and corresponding function on SW1.

**Table 20: SW1, DSP Configuration Switch**

| SW1 Position | Description | Default Value | Function |
|---|---|---|---|
| 5 - 1 | CFGG[4:0] | 00000 | DSP Configuration selection Pins |
| 6 | DDREN | 1(ON) | OFF - DDR2 disable<br>ON - DDR2 enable |
| 7 | RIOEN | 1(ON) | OFF - SRIO disable<br>ON - SRIO enable |
| 8 | LENDIAN | 1(ON) | OFF - Big Endian mode<br>ON - Little Endian mode |

### 4.3.2 SW2, DSP Boot Mode

SW2 is a 5 position DIP switch that is used for DSP boot mode selection and system clock out enable option. A diagram of the SW2 switch (with factory default settings) is shown below.

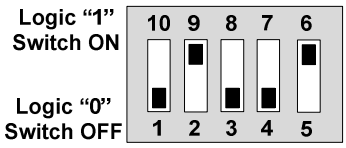


**Figure 4.4: SW2 default settings**

The following table describes the positions and corresponding function on SW2.

**Table 21: SW2, DSP Boot Mode Selection Switch**

| SW2 Position | Description | Default Value | Function |
|---|---|---|---|
| 4 - 1 | Boot Mode[3:0] | 0010 | Boot mode selection pins for DSP. Master I2C boot mode for I2C address 50h<br>Refer to TMS320C6472 datasheet for details of other boot modes supported. |
| 5 | CLKOUTEN | 1(ON) | OFF – SYSCLKOUT disable<br>ON – SYSCLKOUT enable |

**Note**: Please change Boot Mode [3:0] to "0011" for NAND boot mode of this EVM. "0011" is primarily a Master I2C boot mode for I2C address 51h for DSP, which works as NAND boot mode in this EVM.

### 4.3.3 SW3, User Switch

SW3 is a 2 position user accessible switch. A diagram of the SW3 switch (with factory default settings) is shown below. FPGA monitors status of the user switches and stores its value into internal FPGA registers. The DSP can read user switches' value by accessing FPGA's internal registers.

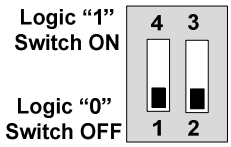


**Figure 4.5: SW3 default settings**

### 4.3.4 SW4, Warm Reset

Push button Switch SW4 asserts DSP's RESET# input when pressed. This will reset the DSP and boot parameters will be reloaded.

### 4.3.5 SW5, Cold Reset

Push button Switch SW5 asserts DSP's POR# and global board reset when pressed. This is equivalent to a power cycle of the board and will have following effects:

- Resets DSP
- Resets FPGA
- Resets Ethernet PHY
- Resets I2C-UART bridge
- Reloads boot parameters.

Re-launch and/or re-connect of CCS application may be required after pressing warm or cold reset buttons.

**Note:** User may refer to TMS320C6472 datasheet to check difference between assertion of DSP RESET# and DSP POR# signals.

## 4.4 Test Points

TMS320C6472 EVM Board has 29 test points. The position of each test point is shown in the figure 4.6 and its description is listed in Table 22.

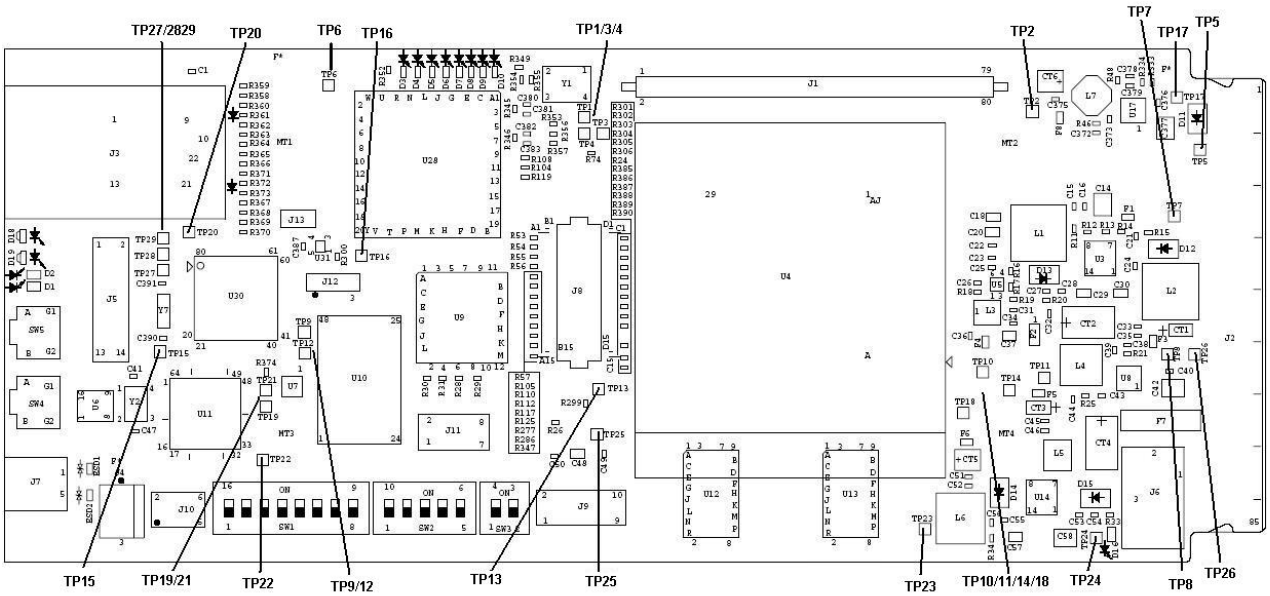


**Figure 4.6: Board Test Points [5]**

**Note: [5] - Some of these TPs may not be visible in TMDSEVM6472LE**

**Table 22: C6472 EVM Board Test Points**

| Test Point | Signal | Test Point | Signal |
|---|---|---|---|
| TP1, TP5, TP20, TP23, TP25, TP26 | Ground | TP13 | System Clock Out |
| TP2 | +2.5V Supply | TP14 | +1.2V Supply |
| TP3 | RGCLK0 | TP15 | FT2232H, PWREN# |
| TP4 | RGCLK1 | TP16 | Enable# |
| TP6 | Test Point, Ethernet PHY | TP17 | Management Power (+3.3V) |
| TP7 | +3.3V Supply | TP18 | +1.8V |
| TP8 | +5V Supply | TP21 | FT2232H, GPIOH0 |
| TP9 | System (Cold) Reset | TP22 | FT2232H, GPIOH1 |
| TP10 | +1.5 Supply | TP24 | +12V Input Supply |
| TP11 | CVDD Supply (+1.2V) | TP27 | MSP430 SMCLK |
| TP12 | DSP (Warm ) Reset | TP28 | MSP430 ACLK |

## 4.5 System LEDs

The C6472 EVM board has 11 LEDs. Their positions on the board are indicated in figure 4.7. The description of each LED is listed in table 23.

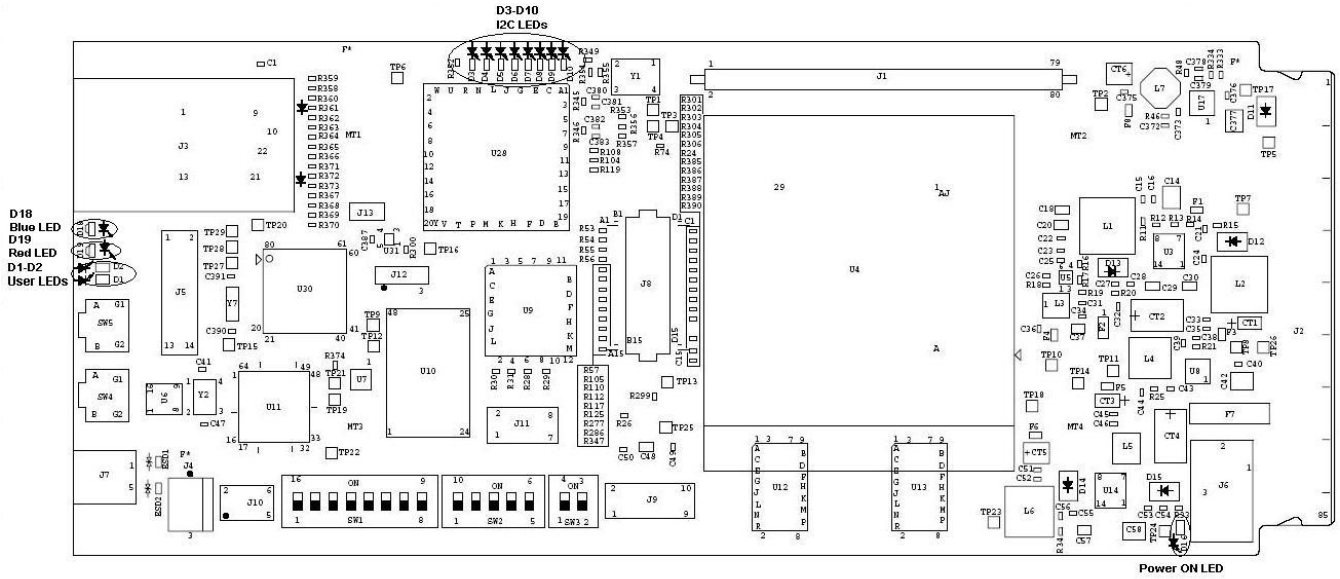


**Figure 4.7: The C6472 EVM Board LEDs**

**Table 23: The C6472 EVM EVM Board LEDs**

| LED# | Color | Description |
|---|---|---|
| D1, D2 | Orange | User LEDs |
| D3 – D10 | Green | I2C LEDs |
| D16 | Green | Board Powered ON Indicator |
| D18 | Blue | Hot Swap status in AMC chassis |
| D19 | Red | Failure and Out of service status in AMC chassis |

Additional LEDs on TMDSEVM6472LE board are highlighted in figure 4.8 and their description is listed in table 24.

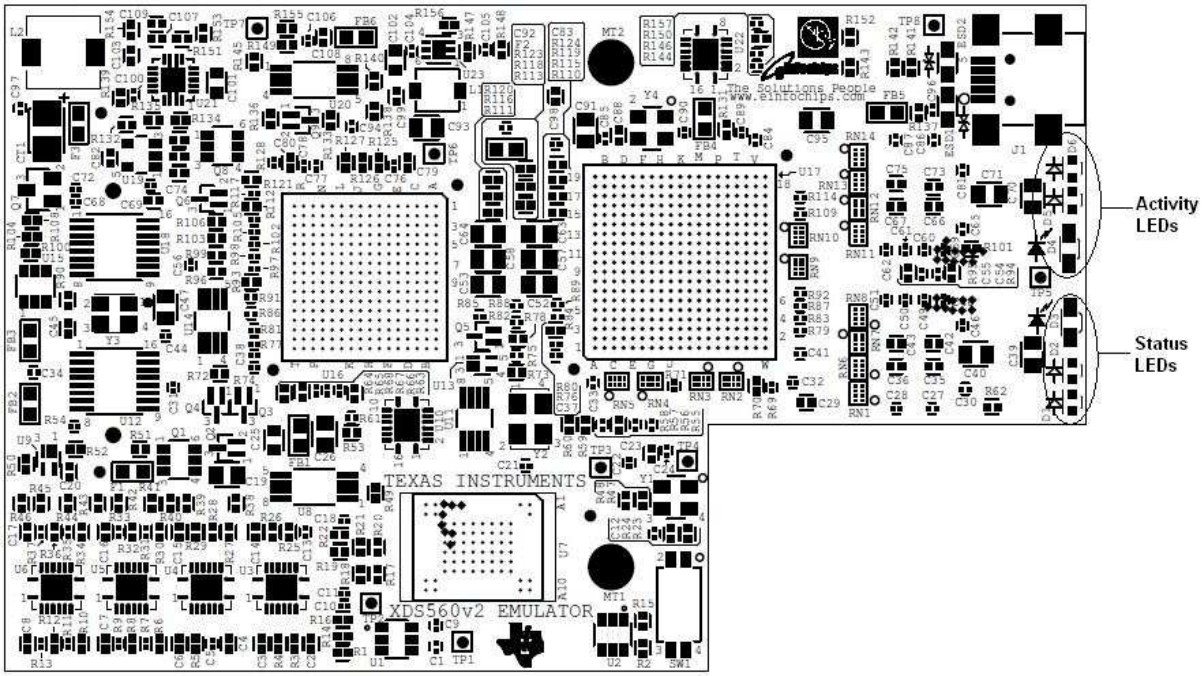


**Figure 4.8: TMDSEVM6472LE Board Additional LEDs**

**Table 24: TMDSEVM6472LE Board Additional LEDs**

| LED# | Color | Description |
|---|---|---|
| D1 (Activity LED 1) | Red | ON - DTC Ready<br>OFF - DTC Not Ready |
| D2 (Activity LED 2) | Yellow | ON - FPGA Programmed<br>OFF - FPGA Not Programmed |
| D3 (Activity LED 3) | Green | Reserved |
| D4 (Status LED 3) | Green | ON =CCS Connected<br>OFF= CCS Disconnected |
| D5 (Status LED 2) | Yellow | DTC to Host Activity |
| D6 (Status LED 1) | Orange | Target to DTC Trace Activity |

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