TMDSEVM6457L / TMDSEVM6457LE Technical Reference Manual Version 2.0

Literature Number: SPRUGX0
Revised March 2011

EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMER

Not for Diagnostic Use: For Feasibility Evaluation Only in Laboratory/Development Environments

The EVM may not be used for diagnostic purposes.

This EVM is intended solely for evaluation and development purposes. It is not intended for use and may not be used as all or part of an end equipment product.

This EVM should be used solely by qualified engineers and technicians who are familiar with the risks associated with handling electrical and mechanical components, systems and subsystems.

Your Obligations and Responsibilities

Please consult the EVM documentation, including but not limited to any user guides, set up guides or getting started guides and other warnings prior to using the EVM. Any use of the EVM outside of the specified operating range may cause danger to the users and/or produce unintended results, inaccurate operation, and permanent damage to the EVM and associated electronics. You acknowledge and agree that:

You are responsible for compliance with all applicable Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, UL, CSA, VDE, CE, RoHS and WEEE,) that relate to your use (and that of your employees, contractors or designees) of the EVM for evaluation, testing and other purposes.

You are responsible for the safety of you and your employees and contractors when using or handling the EVM. Further, you are responsible for ensuring that any contacts or interfaces between the EVM and any human body are designed to be safe and to avoid the risk of electrical shock.

You will defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, “Claims”) arising out of or in connection with any use of the EVM that is not in accordance with the terms of this agreement. This obligation shall apply whether Claims arise under the law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Warning

The EVM board may get very hot during use. Specifically, the DSP, its heat sink and power supply circuits all heat up during operation. This will not harm the EVM. Use care when touching the unit when operating or allow it to cool after use before handling. If unit is operated in an environment that limits free air flow, a fan may be needed.

Preface

About this Document
This document is a Technical Reference Manual for TMS320C6457 EVM designed and developed by eInfochips Limited for Texas Instruments, Inc.

Notational Conventions
This document uses the following conventions:

Program listings, program examples, and interactive displays are shown in a mono-spaced font. Examples use **bold** for emphasis, and interactive displays use bold to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Square brackets ([and]) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets. Unless the square brackets are in a bold typeface, do not enter the brackets themselves.

Underlined, italicized non-bold text in a command is used to mark place holder text that should be replaced by the appropriate value for the user's configuration.

Trademarks

The Texas Instruments logo and Texas Instruments are registered trademarks of Texas Instruments. Trademarks of Texas Instruments include: TI, XDS, Code Composer, Code Composer Studio, Probe Point, Code Explorer, DSP/BIOS, RTDX, Online DSP Lab, TMS320, TMS320C54x, TMS320C55x, TMS320C62x, TMS320C64x, TMS320C67x, TMS320C5000, and TMS320C6000.

MicroTCA and AMC (or AdvancedMC) are trademarks of PICMG.

All other brand, product names, and service names are trademarks or registered trademarks of their respective companies or organizations.

Document Revision History

Release	Chapter	Description of Change
1.0	All	First Draft
2.0	All	Updated for TMDSEVM6457LE

Acronyms

Acronym	Description
AMC or AdvancedMC	Advanced Mezzanine Card
CCS	Code Composer Studio
DDR2	Double Data Rate 2 Interface
DIP	Dual-In-Line Package
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
EEPROM	Electrically Erasable Programmable Read Only Memory
EMAC	Ethernet Media Access Controller
EMIF	External Memory Interface
EVM	Evaluation Module
FPGA	Field Programmable Gate Array
HPI	Host Port Interface
HPI DC	Host Port Interface Daughter Card
I2C	Inter Integrated Circuit
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LED	Light Emitting Diode
McBSP	Multi Channel Buffered Serial Port
MCH	MicroTCA Carrier Hub
MTCA or MicroTCA	Micro Telecommunication Computing Architecture
MMC	Module Management Controller
PICMG®	PCI Industrial Computer Manufacturers Group
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer-Deserializer
SGMII	Serial Gigabit Media Independent Interface
SRIO	Serial RapidIO
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XDS560v2	Texas Instruments' System Trace Emulator

Table of Contents

List of Figures

List of Tables

1. Overview

This chapter provides an overview of the C6457 lite EVM along with the key features and block diagram.

1.1 Key Features

The C6457 lite EVM is a high performance, cost-efficient, standalone development platform that enables users to evaluate and develop applications for the Texas Instruments' TMS320C6457 Digital Signal Processor (DSP). The Evaluation Module (EVM) also serves as a hardware reference design platform for TMS320C6457 DSP. The EVM's form-factor is equivalent to a single-wide PICMG® AMC.0 R2.0 AdvancedMC module.

TMDSEVM6457LE comes with an integrated, high speed, system trace capable XDS560v2 Mezzanine Emulator

Schematics, code examples and application notes are available, to ease the hardware development process and to reduce the time to market.

The key features of the C6457 Lite EVM are:

- Texas Instruments' fixed point DSP - TMS320C6457
- 256 Mbytes of DDR2 Memory
- 128 Mbytes of NAND Flash
- One Gigabit Ethernet port supporting 10/100/1000 Mbps data-rate
- 170 pin B+ style AMC Interface
- I2C EEPROM for booting
- 2 User LEDs and 2 User Switches
- 8 I2C controlled LEDs
- RS232 Serial interface on 3-Pin header or UART over mini-USB connector
- Host Port Interface, McBSP, Timer on 80-pin test header
- 32 bit EMIF interface header option (Footprint Support)
- On Board FPGA (Actel's ProASIC 3) for DSP boot-strapping and NAND Flash interface
- On-Board XDS100 type Emulation using USB 2.0 interface[1]
- TI 60-Pin JTAG header to support External Emulator[1]
- High Speed Integrated XDS560v2 Mezzanine Emulator[2]
- Module Management Controller (MMC) for Intelligent Platform Management Interface (IPMI)
- Powered by DC power-brick adaptor (12V/2.5A) or AMC Carrier back-plane
- AMC like form factor

Note: [1] - Available in TMDSEVM6457L only.
[2] - Available in TMDSEVM6457LE only.

1.2 Functional Overview

The C6457 lite EVM contains single TMS320C6457 fixed point Digital Signal Processor. TMS320C6457 device is based on the third-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture, making these DSPs an excellent choice for applications including video and telecom infrastructure, imaging/medical, and wireless infrastructure (WI). The C64x+ devices are upward code-compatible from previous devices that are part of the C6000™ DSP platform.

The functional block diagram of TMDSEVM6457L is shown in figure 1.1

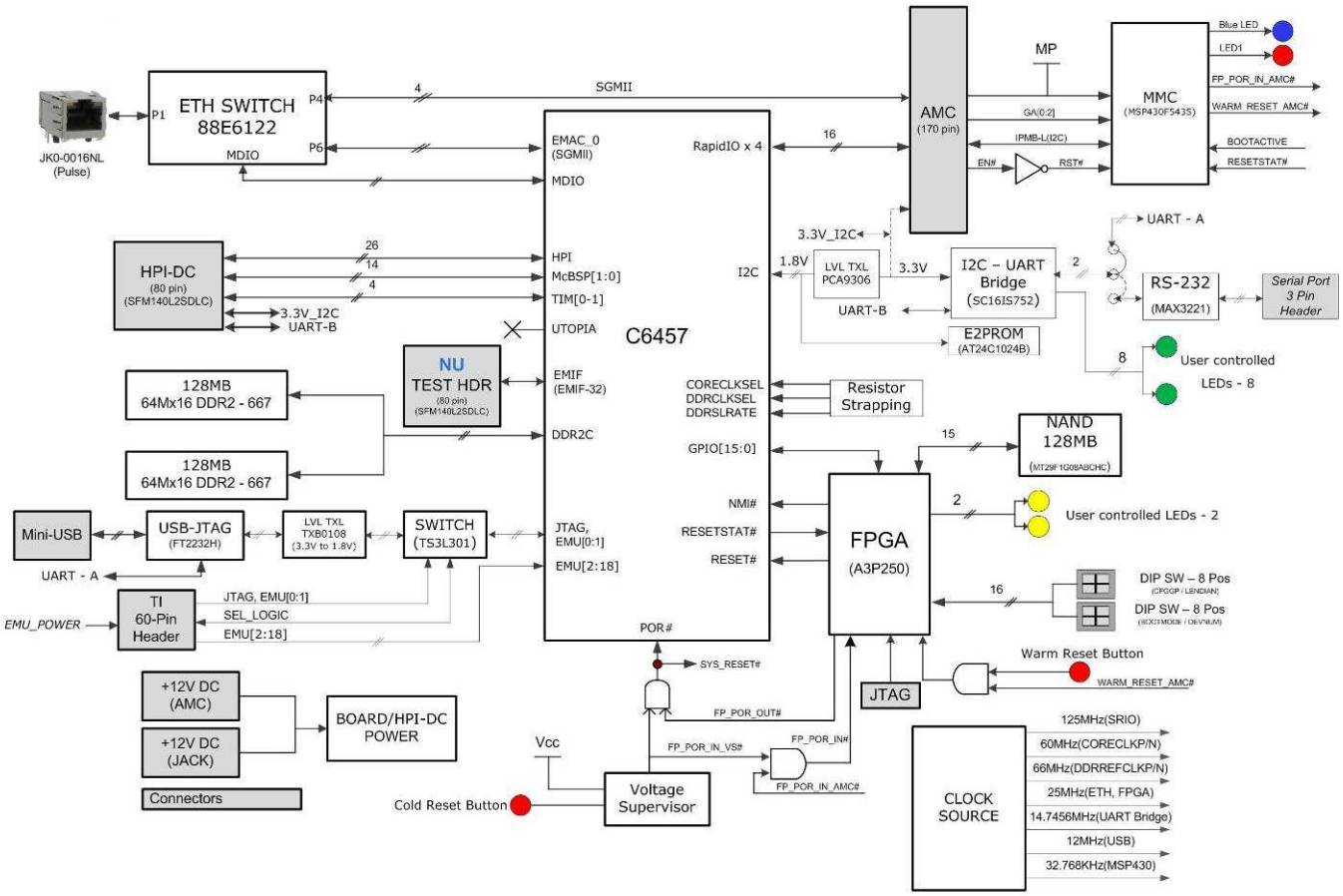

Figure 1.1: Block Diagram of TMDSEVM6457L

The functional block diagram of TMDSEVM6457LE is shown in figure 1.2

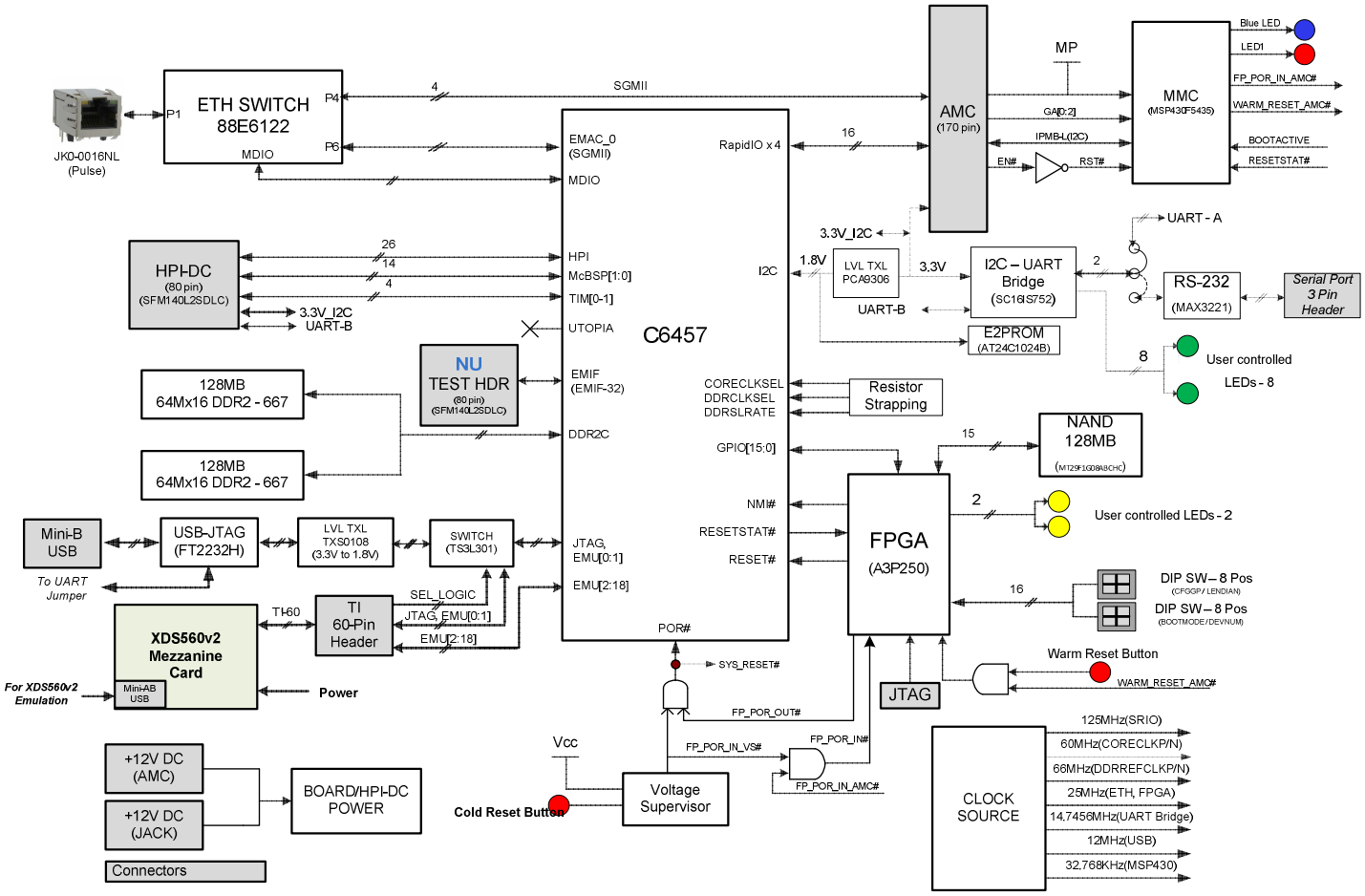

Figure 1.2: Block Diagram of TMDSEVM6457LE

1.3 Basic Operation

The C6457 lite EVM platform is designed to work with TI's Code Composer Studio version 4 (CCSv4) development environment and is shipped with the latest version with all necessary emulation drivers. CCSv4 interfaces with the board via on-board emulation circuitry using the USB cable supplied along with this EVM or through external emulator. For TMDSEVM6427LE, CCSv4 interfaces with the board only via XDS560v2 System Trace emulator using the USB cable supplied.

To start operating the board, follow instructions in the Quick Setup Guide. Follow the instruction in BIOS MCSDK Getting Started Guide to install all the necessary development tools, drivers and documentation.

After the installation is completed, follow below steps to run Code Composer Studio.

1. Power ON the board using power brick adaptor (12V/2.5A) supplied along with this EVM or Insert this EVM board into MicroTCA chassis or AMC carrier back-plane.
2. Connect USB cable from host PC to EVM board for TMDSEVM6457L or to XDS560v2 Mezzanine emulator for TMDSEVM6457LE.
3. Launch Code Composer Studio from host PC by double clicking on its icon at PC desktop.

Detailed information about the EVM including examples and reference material is available in the DVD available with this EVM kit.

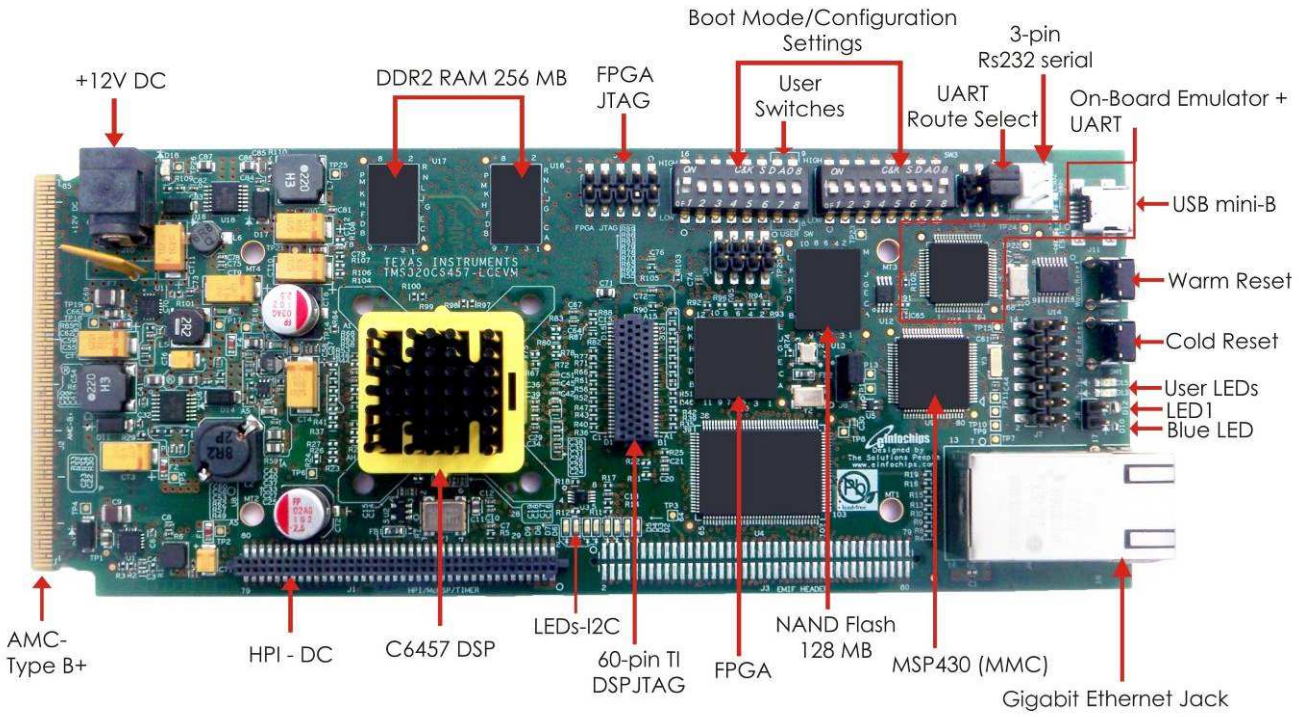

Figure 1.3: TMDSEVM6457L

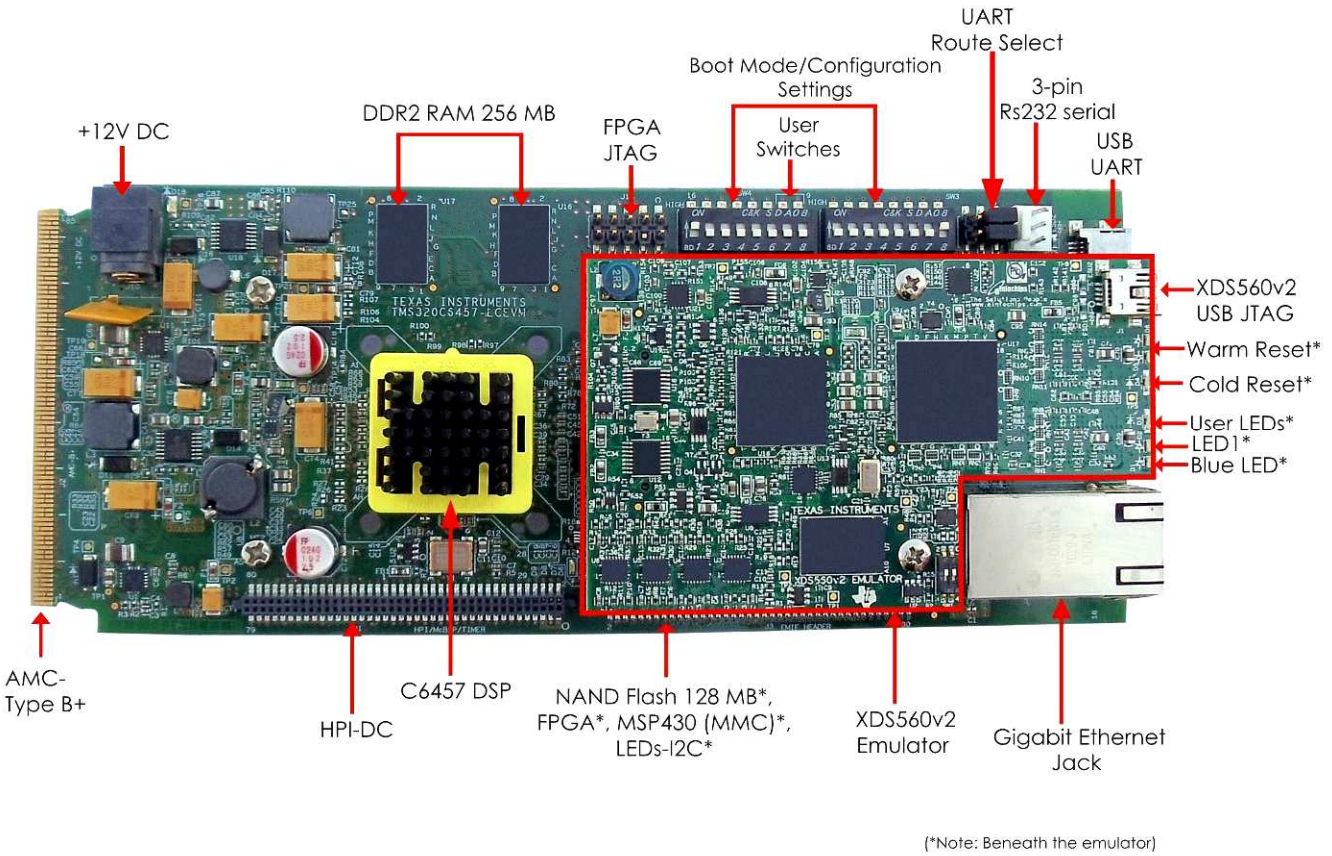

Figure 1.4: TMDSEVM6457LE

1.4 Boot Mode and Boot Configuration Switch Setting

The C6457 lite EVM has 16 sliding DIP switches (Board Ref. SW3 and SW4) to determine boot mode, boot configuration, device number, endian mode, HPI width and EMIF clock selection (internal / external) options at every reset of the DSP.

1.5 Power Supply

TMDSEVM6457 can be powered from a single +12V / 2.5A DC (30W) external power supply connected to the DC power jack (J10). Internally, +12V input is converted into desired voltage levels such as, +5V, +3.3V, +2.5V, +1.8V, +1.5V and +1.1V using local DC-DC converters.

- +1.1V is used for DSP Core (CVDD) and SRIO/SGMII IO supply for DSP
- +1.5V is used for FPGA core
- +1.8V is used for DSP GPIOs, DDR2 / FPGA IO, NAND flash interface
- +2.5V is used for Ethernet Switch
- +3.3V is used for DSP HPI/EMIF IOs
- The DC power jack connector is a 2.5mm barrel-type plug with center-tip as positive polarity

The C6457 lite EVM can also draw power from the AMC edge connector (J2). If the board is inserted into a PICMG® MicroTCA.0 R1.0 compliant system chassis or AMC Carrier back-plane, an external +12V supply from DC jack (J10) is not required.

2. Introduction to the C6457 lite EVM Board

This chapter provides an introduction and details of interfaces for the C6457 lite EVM board. It contains:

2.1 Memory Map

The memory map of the TMS320C6457 device is as shown in Table 1. The external memory configuration register address ranges in the C6457 device begin at the hex address location 0x7000 0000 for EMIFA and hex address location 0x7800 0000 for DDR2 Memory Controller.

Table 1: TMS320C6457 Memory Map

Hex Address Range	Memory Block Description
0x00000000 – 0x007FFFFF	Reserved
0x00800000 – 0x009FFFFF	L2 RAM
0x00A00000 – 0x00DFFFFF	Reserved
0x00E00000 – 0x00E07FFF	L1P SRAM
0x00E08000 - 0x00EFFFFF	Reserved
0x00F00000 - 0x00F07FFF	L1D SRAM
0x01800000 - 0x01BFFFFF	C64x+ Megamodule Registers
0x01C00000 - 0x77FFFFFF	Control Registers, Reserved
0x78000000 - 0xDFFFFFFF	DDR2 EMIF Config, Reserved
0xE0000000 - 0xFFFFFFFF	CE0 DDR2 SDRAM

2.2 EVM Boot Mode and Boot Configuration Switch Settings

The C6457 lite EVM has two configuration switches SW3 and SW4. Whenever the user presses a Cold or Warm Reset button or power-cycles the board, an on-board FPGA latches the state of configuration inputs from SW3 and SW4 and presents them to the DSP during the reset period.

SW3 determines general DSP configuration, little or big endian mode, HPI width selection and EMIFA input clock source. SW4 determines DSP boot mode and device number for DSP. Please refer to section 4.3 of this document for default switch setting and details of each switch. For more information on DSP supported Boot mode, refer to TMS320C6457 datasheet and TMS320C6457 Boot loader User's Guide (TMS320C645x/C647x DSP User's Guide)

2.3 Clock Configuration

Table 2 shows clock configuration information of the EVM.

Table 2: Clock Configurations

Clock	Frequency	Description
CORECLKN/P	60.000MHz	Clock Input for PLL1(Differential)
DDRREFCLKN/P	66.000MHz	DDR Reference Clock Input to DDR PLL (differential)

2.4 Board Revision ID

Board PCB (Printed Circuit Board) and PCA (Printed Circuit Assembly) revision are located below RJ-45 Jack in bottom silk, as shown in Figure 2.1. Table 3 describes the PCA/PCB revisions.

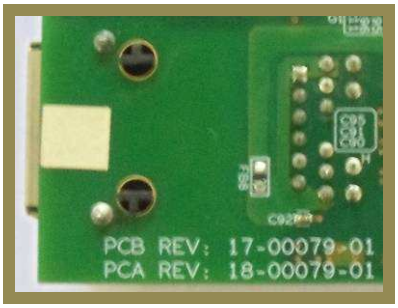

Figure 2.1: EVM Board Revision

Table 3: PCA/PCB revision description

PCA REV	PCB REV	Description
18-00079-01	17-00079-01	Pilot boards (Initial engineering samples)
18-00079-02	17-00079-02	Production boards

Note: Last two digits represent major PCB / PCA revision number.

2.5 JTAG - Emulation Overview

2.5.1 JTAG – TMDSEVM6457L

The EVM supports two different types of DSP Emulation - “USB mini-B” and “60-pin TI JTAG-DSP”.

USB emulation is supported through an on-board, optimized XDS100-class embedded emulation circuit. On-board (embedded) USB emulation is accessible through the USB mini-B connector (J11); hence any external emulator is not necessary to connect EVM with Code Composer Studio. User can connect CCS with target DSP in EVM with USB cable supplied along with this board.

TI 60-pin JTAG header (J5) is provided on-board to allow user to connect to external emulator for high speed real-time emulation. External/mezzanine emulators as XDS560v2 emulators and standard XDS510 or XDS560 emulators with 60 to 20-pin or 60 to 14-pin adapter boards from TI and 3rd-party vendors are supported. Please refer to the documentation supplied with your emulator for connection assistance.

Both emulator configurations are enabled by default and there is dynamic switching between them. On-board embedded JTAG emulator is default connection to DSP, however when external emulator is connected to EVM, board circuitry automatically switches to give access to external emulator. When both are connected at the same time, external emulator is given priority and on-board emulator is disconnected from DSP.

The interface between DSP, on-board and external emulator is shown in figure below:

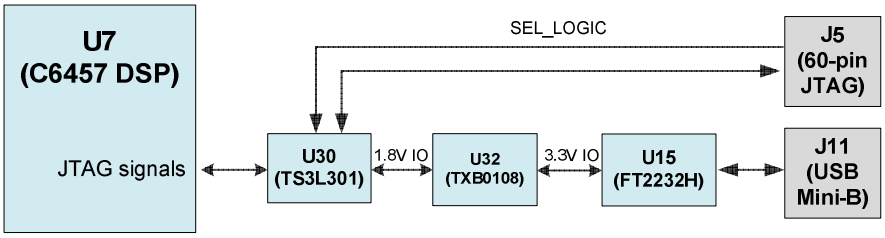

Figure 2.2: TMDSEVM6457L JTAG emulation

2.5.2 JTAG – TMDSEVM6457LE

In TMDSEVM6457LE, high speed real time emulation can be performed without needing an external emulator as it has an integrated, system trace capable XDS560v2 Mezzanine Emulator mounted on its TI 60-pin JTAG header (J3). User can connect the EVM to CCS by connecting the USB port of XDS560 Mezzanine Emulator to PC using USB cable supplied with an EVM.

As high speed XDS560v2 Emulator is already mounted on TI 60-pin JTAG header of the EVM, the low speed XDS100 emulation is no longer required and not available to user.

It is important to note that for XDS560v2 emulation, the USB cable needs to be connected to the mini-AB connector (J1) on XDS560v2 Mezzanine Emulator and not to mini-B connector (J11) on the main board. For TMDSEVM6457LE, the mini-B connector (J11) on the main board can be used to access UART-over-USB; please refer to section 2.11 of this document for more details.

The interface between DSP and XDS560v2 Mezzanine Emulator is shown in figure 2.3:

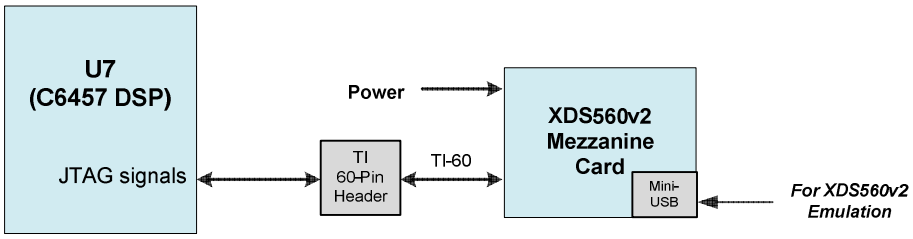

Figure 2.3: TMDSEVM6457LE JTAG emulation

2.5.2.1 XDS560v2 Mezzanine Emulator Booting

When TMDSEVM6457LE is powered ON, the XDS560v2 Mezzanine Emulator starts booting. It takes approximately half minute to boot-up. The successful booting of XDS560v2 Mezzanine Emulator is indicated by following LEDs sequence:

- Green LED (D3) turns ON
- Yellow LED (D2) and Red LED (D1) turns ON
- Green LED (D3) blinks and turns OFF

After the completion of booting XDS560v2 mezzanine emulator is ready to interface with CCS. Once CCS is connected to the target DSP Green LED D4 turns ON.

The boot failure is indicated by simultaneous blinking of Red LED (D1), Yellow LED (D2) and Green LED (D3). In this case CCS can't be connected to XDS560v2 mezzanine emulator. The boot failure can happen when mezzanine emulator is attempted to mount over a non-compatible base EVM.

2.6 Clock Domains

The EVM incorporates variety of clocks to TMS320C6457 as well as other devices which are configured automatically during the power up configuration sequence. The figure below illustrates the clocking for the system in EVM module.

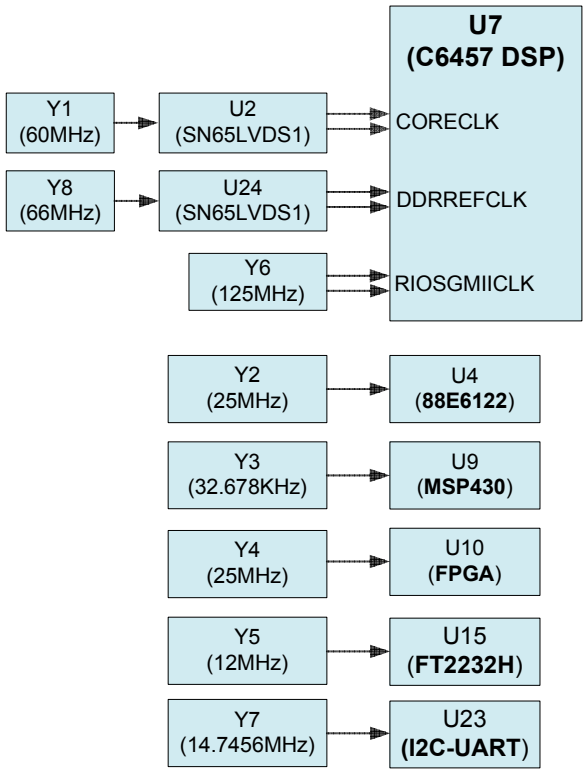

Figure 2.4: C6457 EVM Clock Domains

2.7 I2C Boot EEPROM

The I2C EEPROM address 0x50 contains Power on Self Test (POST) program and I2C address 0x51 contains second level boot-loader program. The second level boot-loader reads the Out-Of-Box Demo program from the NAND FLASH memory.

2.8 FPGA

The FPGA (Actel #A3P250-FGG144) interface provides reset control circuitry and latching of device configuration pins. The logic level of these pins is latched at reset to determine the device configuration. These switch-controlled inputs are driven to the DSP at reset time.

FPGA supports two modes; Normal mode and NAND pass through mode. These modes are mutually exclusive modes. In Normal mode, FPGA provides access to FPGA registers through DSP's GPIO pins. FPGA supports 2 user LEDs and 2 User Switches through control registers.

In NAND pass through mode, DSP GPIOs are directly assigned to NAND pins. NAND access is only possible in NAND pass through mode. Details of these are provided in chapter 3 FPGA Functional Specification.

Below figure shows interface between C6457 DSP and FPGA.

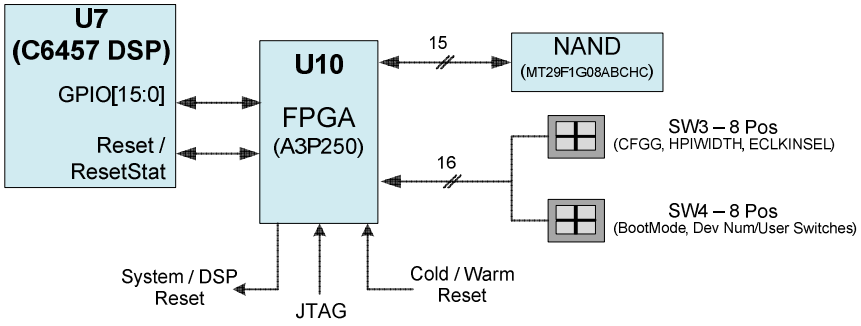

Figure 2.5: C6457 EVM FPGA Connections

2.9 Ethernet Switch

TMS320C6457 supports SGMII EMAC interface and it is connected to Port 6 of on board Giga bit Ethernet Switch 88E6122. The interface between DSP and Ethernet Switch (U4) is shown in figure below:

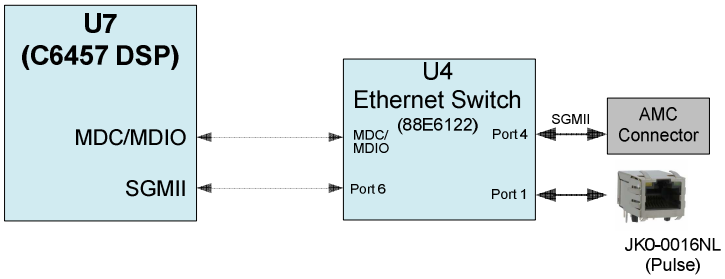

Figure 2.6: C6457 EVM Ethernet Switch Routing

The Ethernet switch's Port 1 is configured for copper interface and routed to Gigabit RJ-45 connector (J4). Port 4 of Ethernet switch is configured in SGMII mode routed to AMC edge connector (Port 0) for back-plane interface. At Power On, Ethernet switch will be configured by the configuration EEPROM (U19). The default configuration will ensure the connectivity of DSP SGMII port to RJ45 connector and Port 0 of AMC edge connector.

2.10 Serial RapidIO (SRIO) Interface

TMS320C6457 supports high speed SERDES based Serial RapidIO (SRIO) interface. There are total four 1x or one 4x Serial RapidIO ports available on C6457. All SRIO ports are routed to AMC edge connector on board as per the PICMG AMC.0 R2.0 specifications; SRIO ports 1-4 are routed to AMC ports 8-11 respectively. Below figure shows RapidIO connections between the DSP and AMC edge connector.

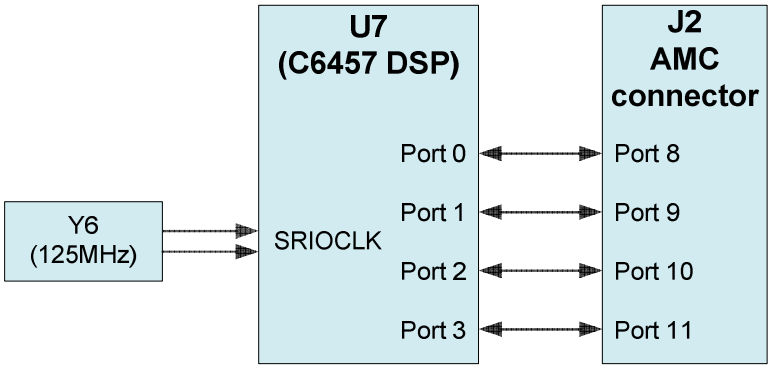

Figure 2.7: C6457 EVM SRIO Port Connections

2.11 UART Interface

A serial port is provided for UART communication using an I2C-UART bridge. This serial port can be accessed either through USB connector (J11) or through 3-pin (Tx, Rx and Gnd) serial port header (J12). The selection can be made through UART Route Select shunt-post J13 as follows:

- UART over mini-USB Connector - Shunts installed over J13.3-J13.1 and J13.4 -J13.2 **(Default)**
- UART over 3-Pin Header (J12) - Shunts installed over J13.3-J13.5 and J13.4 -J13.6

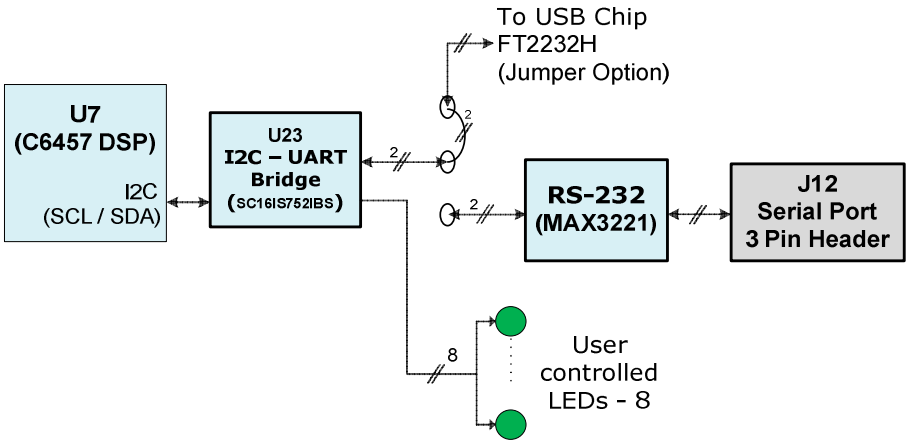

Figure 2.8: C6457 EVM UART Connections

2.12 Module Management Controller (MMC) for IPMI

The C6457 lite EVM supports limited set of Intelligent Platform Management Interface (IPMI) commands and Module Management Controller (MMC) based on Texas Instruments MSP430F5435 mixed signal processor.

The MMC will communicate with MicroTCA Carrier Hub (MCH) over IPMB (Intelligent Platform Management Bus) when inserted into AMC slot of a PICMG® MTCA.0 R1.0 compliant chassis. The primary purpose of the MMC is to provide necessary information to MCH, to enable the payload power to The C6457 lite EVM when it is inserted into the MicroTCA chassis.

The EVM also supports a Blue LED and LED1 on the front panel as specified in PICMG® AMC.0 R2.0 AdvancedMC base specification. Both of these LEDs will blink as part of initialization process when the MMC will receive management power.

Blue LED:

Blue LED will turn ON when MicroTCA chassis is powered ON and an EVM is inserted into it. The blue LED will turn OFF when payload power is enabled to the EVM by the MCH.

LED1:

Red colored LED1 will normally be OFF. It will turn ON to provide basic feedback about failures and out of service.

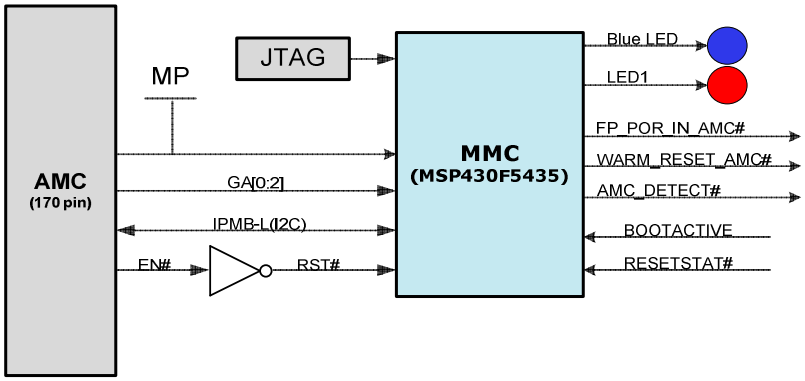

Figure 2.9: C6457 EVM MMC Connections for IPMI

2.13 HPI

TMS320C6457 has an HPI interface, which can be accessed by an external host controller. This HPI interface is available on HPI Daughter Card (DC) connector J1 of the EVM.

2.14 Additional Headers

The C6457 lite EVM contains 80 pin header (J1) which has HPI, McBSP [1:0], TIM [1:0], I2C and UART signal connections. It shall be noted that HPI, I2C and UART connections to this header (J1) are of 3.3V level whereas McBSP, Timers and GPIO signals are of 1.8V level.

The C6457 lite EVM also contains footprint provision for an additional 80 pin header (J3) for 32 bit EMIF interface.

3. FPGA Functional Specification

This chapter contains:

3.1 FPGA Modes

The FPGA can be configured in two modes. They are:

1. Normal mode
2. NAND pass through mode

After the completion of booting, DSP GPIO 14 is used to select between the Normal mode and the NAND Pass through mode.

If DSP GPIO 14 is 1'b0, normal mode is selected. FPGA registers can be accessed in normal mode of operation only.

If DSP GPIO 14 is 1'b1, Pass-Through mode is selected. In this mode DSP GPIO pins are directly mapped to the pins of the NAND Flash memory except Write-Protect Pin. The Write-Protect pin is not mapped due to unavailability of a GPIO pin in NAND pass through mode. The Write-Protect Pin of NAND Flash is mapped to the bit [4] of NAND_CWR_REGH FPGA register. The user application will require to disable write protect using the FPGA normal mode and then switch to NAND pass through mode to write to the NAND flash.

3.2 FPGA – DSP Communication Signals

The GPIO signals used for communication between FPGA and DSP when FPGA is in Normal mode are described in Table 4. The GP[12:13] are not used.

Table 4: GPIO pin mapping in Normal mode

GPIO#	Function	Direction	Description
GP[7:0]	Data	Bidirectional	This is 8-bit wide bidirectional bus, shared for address and data. Whether the signals currently carry address, read data, or write data is defined by the Command signals.
GP[9:8]	Command	Input	These bits define the bus operation for the current strobe period. 00 - NOP 01 - address cycle 10 - read cycle 11 - write cycle
GP10	Strobe	Input	This signal is used to synchronize the bus activity between the DSP and FPGA. The DSP is always master of the bus timing.
GP11	Ready	Output	A low value on this pins during a read or write cycle will cause the DSP to extend the cycle until the signal goes high. This signal is not monitored for address and NOP cycles
GP14	FPGA mode select	Input	This signal selects the mode of communication with the NAND Flash Memory. If it is 1'b1, then pass-through mode is enabled whereby the DSP GPIO pins are directly mapped to the pins of NAND Flash Memory. If it is 1'b0, then Normal Mode of operation is selected in which FPGA Configuration Registers will be accessed.
GP 15	I2C-UART interrupt	Output	This signal directly follows the Bridge Interrupt input to FPGA.

GPIO signals used for communication between FPGA and DSP when FPGA is used in NAND pass through mode are described in Table 5.

Table 5: FPGA Configuration Registers Set

GPIO#	Function	Direction	Description
GP[7:0]	Data	Bidirectional	This 8-bit data bus is mapped to the 8-bit data bus of NAND Flash Memory.
GP[9:8]	Command	Input	GP[8] pin is mapped to the Command Latch Enable (CLE) pin of NAND Flash Memory. GP[9] pin is mapped to the Address Latch Enable (ALE) pin of NAND Flash Memory.
GP10	Write enable	Input	This signal is mapped to the Write Enable (nWE) pin of the NAND Flash Memory.
GP11	Ready	Output	This signal is mapped to the Ready/Busy (RB) pin of the NAND Flash Memory.
GP12	Read enable	Input	This signal is mapped to the Read Enable (nRE) pin of the NAND Flash Memory.
GP13	Chip enable	Input	This signal is mapped to the Chip Enable (nCE) pin of the NAND Flash Memory.
GP14	FPGA mode select	Input	This signal selects the mode of communication with the NAND Flash Memory. If it is 1'b1, then pass-through mode is enabled whereby the DSP GPIO pins are directly mapped to the pins of NAND Flash Memory. If it is 1'b0, then Normal Mode of operation is selected in which FPGA Configuration Registers will be accessed.
GP 15	I2C-UART interrupt	Output	This signal directly follows the Bridge Interrupt input to FPGA.

3.3 FPGA Memory Map

Table 6 describes the memory map of FPGA when FPGA is configured in Normal mode of operation.

Table 6: FPGA Memory Map

GPIO[7:0]	Memory
0x00 – 0x22	Configuration Memory Space

3.4 FPGA Configuration Registers

The following table enlists the FPGA configuration register and its description:

Table 7: FPGA Configuration Registers Set

Name	Address	Read / Write	Default value in HEX	Data bits	Description
Reserved	0x00 - 0x05	-	-	7:0	Reserved for future use.
BITFILE_VER_REG	0x06	Read	0x01	7:0	Shows the BITFILE version
RTL_VER_REG	0x07	Read	0x01	7:0	Shows the RTL version
-	0x08	-	0x00	7:0	Reserved for future use.
CONTROL_REGH	0x09	Read / Write	0x70	3:0	Reserved for future use.
				4	Write Protect Bit 1 => Disable 0 => Enable This bit is mapped to the Write-Protect pin of NAND Flash Memory if the Pass-Through Mode is enabled.
				5	User LED 0 Data. The bit value that is written at this location is driven on the User LED 0, if the User LED is enabled via NAND_CWR_REGH[7].
				6	User LED 1 Data. The bit value that is written at this location is driven on the User LED 1, if the User LED is enabled via NAND_CWR_REGH[7].
				7	User LED's Enable/Disable 0 => FPGA drives 1'b1 on User LED's (Disable). 1 => Data present in the NAND_CWR_REGH [6:5] is driven on the User LED's (Enable).
Reserved	0x0A – 0x21	-	-	7:0	Reserved for future use. (RFU)
USER_SW_REG	0x22	Read	0x00	0	tievm_user_sw1_i
				1	tievm_user_sw2_i
				4:2	Reserved for future use
				7:5	tievm_board_ver_i[2:0]

3.5 FPGA-DSP Communication Protocol in FPGA Normal Mode

At system reset FPGA becomes master and DSP becomes slave. The FPGA will provide the boot parameters to DSP. Once booting is done the FPGA will become slave and DSP will become master, at this point the below mentioned protocol is implemented.

The 16 bit bus from DSP GPIO to FPGA is divided in

- 8-bit bi-directional bus which is shared between data and address.
- 4-bit for control and handshaking signals.
- 2-bits are not used.

DSP to FPGA has strobe based asynchronous communication.

After the DSP reset and boot sequence the GPIO pins will transition from their configuration role to their role in the GPIO Bus.

The DSP is the master of the GPIO BUS. The DSP will initiate bus cycles, define how long they last and when they will complete. The FPGA can extend a read or write cycle if needed.

The normal write sequence is for the DSP to issue an address cycle followed by a write cycle. The normal read sequence is for the DSP to issue an address cycles followed by a read cycle. If a read or write cycle is not preceded by an address cycle, the address of the last cycle is used. This allows repeated reads or writes to a given register.

To initiate an address cycle the DSP will:

1. Set the value of cmd
2. Set the direction of data_io as output from DSP
3. Set the address value on data_io
4. Set stb_o active
5. Wait a minimum of 50 ns
6. Set stb_o inactive
7. Wait a minimum of 50 ns before the next cycle starts

Procedure 3-1: Address cycle Initiation by DSP

To initiate a write cycle the DSP will:

1. Set the value of cmd
2. Set the direction of data_io as output from DSP
3. Set the write data value on data_io
4. Set stb_o active
5. Wait a minimum of 50 ns
6. If rdy_o is low wait until it is high
7. Set stb_o inactive
8. Wait a minimum of 50 ns before the next cycle starts

Procedure 3-2: Write cycle Initiation by DSP

To initiate a read cycle the DSP will:

Set the value of cmd
Set the direction of data_io as input to DSP
Set stb_o active
Wait a minimum of 50 ns
If rdy_o is low wait until it is high
read data_io and store as the read cycle result
Set stb_o inactive
Wait a minimum of 50 ns before the next cycle starts

Procedure 3-3: Read Cycle Initiation by DSP

The FPGA will only enable its data_io drive when cmd == READ and stb_o is active. The FPGA must ensure that its driver is off no later than 40 ns after stb_o goes inactive.

The bus may idle after any of the above cycles; an explicit NOP cycle is not needed

3.6 Sequence of Operation

Following section provides details of FPGA sequence of operation.

3.6.1 Boot Sequence – Power-On (Cold) Reset

1. On system reset (power-on reset), available through the global FPGA system reset pin, assert POR# and RESET# pin active low
2. Wait for the FPGA internal PLL to stabilize
3. Once the PLL is locked, user defined configuration pins and fixed configuration pins are latched by FPGA and pin status are provided to C6457 device configuration pins. For device configuration settings please refer to sections 4.3.3 DSP Configurations and 4.3.4 DSP Boot mode.
4. Wait for 50 µS. As the frequency of operation of the FPGA is 40MHz, the internal counters would count 2000 clock cycles
5. De-assert RESET#. Keep POR# asserted.
6. Wait for 200 mS. As the frequency of operation of the FPGA is 40MHz, the internal counters would count 8000000 clock cycles. De-assert POR#.
7. Wait for RESETSTAT# signal from DSP to go from low to high. GPIO lines to GIC modules would be put in tri-state condition
8. If boot modes are for EMAC boot (0'b0110, 0'b0111, 0'b1000) on boot mode DIP input switch, wait for 4 seconds. Assert RESET# and wait for 50 µS. De-assert RESET#.
9. Indicate GIC module that the boot mode is over

Procedure 3-1: Power on Reset

3.6.2 Boot Sequence – Warm Reset

1. On warm reset, available through the push button switches on-board, assert RESET# pin active low
10. Once the PLL is locked, user defined configuration pins and fixed configuration pins are latched by FPGA and pin status are provided to C6457 device configuration pins. For device configuration settings please refer to sections 4.3.3 DSP Configurations and 4.3.4 DSP Boot mode.
2. Wait for 50 µS. As the frequency of operation of the FPGA is 40MHz, the internal counters would count 2000 clock cycles
3. De-assert RESET#
4. Wait for RESETSTAT# signal from DSP to go from low to high. GPIO lines to GIC modules would be put in tri-state condition
5. Indicate GIC module that the boot mode is over

Procedure 3-1: Warm Reset

4. EVM Board Physical Specifications

This chapter describes the physical layout of the C6457 lite EVM board and its connectors, switches and test points. It contains:

4.1 Board Layout

The C6457 lite EVM board dimension is 7.11” x 2.89” (180.6mm x 73.5mm). It is a 12 layer board and powered through connector J10. Figure 3-1 and 3-2 shows assembly layout of the C6457 Lite EVM Board.

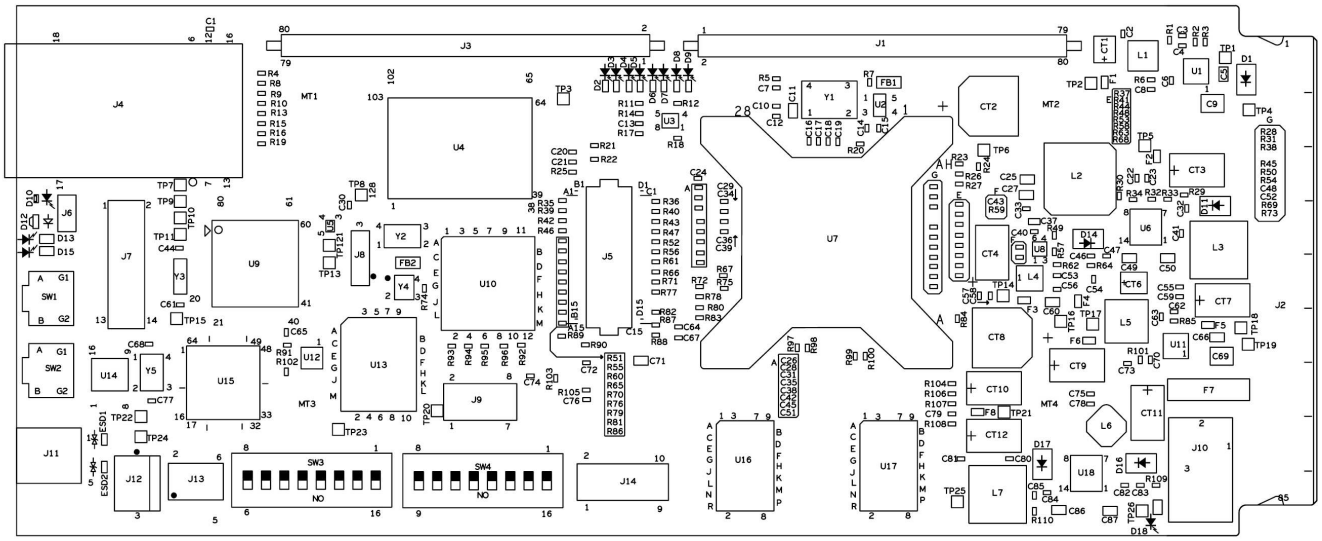

Figure 4.1: C6457 Lite EVM Board Assembly Layout – TOP view

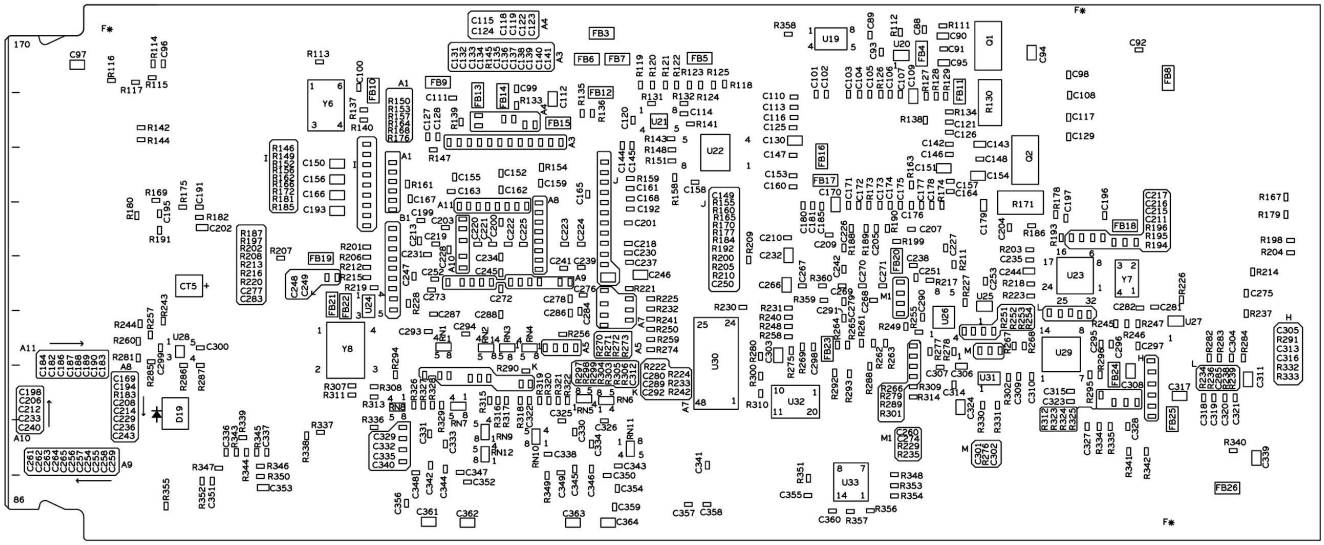

Figure 4.2: C6457 Lite EVM Board layout – Bottom view

4.2 Connector Index

The C6457 lite EVM Board has several connectors which provide access to various interfaces on the board.

Table 8: TMS320C6457 Lite EVM Board Connectors

Connector	Pins	Function
J1	80	HPI DC Connector
J2	170	AMC Edge Connector
J3	80	EMIF Test Header (Option)
J4	18	Giga bit Ethernet RJ-45 Connector
J5	60	TI 60-Pin DSP JTAG Connector [3]
J6	*2*	*AMC Enable -- For Factory Use Only*
J7	*14*	*MSP430 JTAG Connector -- For Factory Use Only*
J8	*3*	*MSP430 Power Selection -- For Factory Use Only*
J10	3	DC Power Input Jack Connector
J11	5	Mini-B USB Connector
J12	3	UART 3-Pin Connector
J13	6	UART Route Select Jumper
J14	10	FPGA JTAG Connector
J1	5	Mini-AB USB Connector [4]

Note: **[3] – Not Available in TMDSEVM6457LE.**
[4] – Present on XDS5602v2 Mezzanine Card. Available in TMDSEVM6457LE only.

4.2.1 J1, HPI DC Connector

Connector J1 provides the HPI, McBSP and Timer Interfaces of the DSP. The signals on this connector are shown in the table below. This connector is identical to the HPI connector implemented on previous AMC EVMs of TI, so that any previous test fixtures will connect without revision.

Table 9: HPI DC Connector

Pin	Signal	Description	Pin	Signal	Description
1	VCC5	+5V Power	2	VCC3.3	+3.3V Power
3	GND	Ground Signal	4	VCC3.3	+3.3V Power
5	VCC5	+5V Power	6	VCC1.8	+1.8V Power
7	GND	Ground Signal	8	GND	Ground Signal
9	HPI_D1	Data Signal – 1	10	VCC1.8	+1.8V Power
11	HPI_D3	Data Signal – 3	12	HPI_D0	Data Signal – 0
13	HPI_D5	Data Signal – 5	14	HPI_D2	Data Signal - 2
15	HPI_D7	Data Signal – 7	16	HPI_D4	Data Signal - 4
17	GND	Ground Signal	18	HPI_D6	Data Signal - 6
19	HPI_D9	Data Signal – 9	20	GND	Ground Signal
21	HPI_D11	Data Signal - 11	22	HPI_D8	Data Signal - 8
23	HPI_D13	Data Signal – 13	24	HPI_D10	Data Signal - 10
25	HPI_D15	Data Signal – 15	26	HPI_D12	Data Signal - 12
27	GND	Ground Signal	28	HPI_D14	Data Signal - 14
29	HPI_DS2#	Data Strobe – 2	30	GND	Ground Signal
31	GND	Ground Signal	32	HPI_HAS#	Address Strobe
33	HPI_DS1#	Data Strobe – 1	34	GND	Ground Signal
35	GND	Ground Signal	36	HPI_CNTL0	Control Select 0
37	HPI_CS	Chip Select	38	GND	Ground Signal
39	GND	Ground Signal	40	GP14_HPIWIDTH	GPIO
41	HPI_CNTL1	Control Select 1	42	GND	Ground Signal
43	GND	Ground Signal	44	HPI_INT	Interrupt
45	HPI_RDY#	Ready indication	46	GND	Ground Signal
47	GND	Ground Signal	48	MCBSP0_FSR	MCBSP0 RX Frame Sync
49	HPI_RW#	Read/Write select	50	MCBSP0_FSX	MCBSP0 TX Frame Sync
51	McBSP0_CLKS	McBSP0 Module Clock	52	MCBSP0_DR	MCBSP0 RX Data
53	McBSP0_CLKR	McBSP0 RX Clock	54	MCBSP0_DX	MCBSP0 TX Data
55	McBSP0_CLKX	McBSP0 TX Clock	56	GND	Ground Signal
57	I2C_3V3_SCL	I2C Clock	58	MCBSP1_CLKS	McBSP1 Module Clock
59	I2C_3V3_SDA	I2C Data	60	MCBSP1_CLKR	McBSP1 RX Clock
61	GND	Ground Signal	62	MCBSP1_CLKX	McBSP1 TX Clock
63	MCBSP1_FSR	McBSP0 RX Frame Sync	64	UARTB_TX	UART TX data
65	MCBSP1_FSX	McBSP0 TX Frame Sync	66	UARTB_RX	UART RX data
67	MCBSP1_DR	McBSP0 RX data	68	TIM_0_IN	Timer 0 Input
69	MCBSP1_DX	McBSP0 TX data	70	GND	Ground Signal
71	GND	Ground Signal	72	TIM_0_OUT	Timer 0 Output
73	TIM_1_IN	Timer 1 Input	74	GND	Ground Signal
75	GND	Ground Signal	76	TIM_1_OUT	Timer 1 Output
77	HPI_HWIL	Half Word Select	78	GND	Ground Signal
79	GND	Ground Signal	80	GP15_ECLKINSEL	GPIO

Note: HPI, I2C and UART signals (highlighted in blue) are 3.3V level. McBSP, Timer and GPIO signals (highlighted in green) are 1.8V level.

4.2.2 J2, AMC Edge Connector

The J2 card edge connector plugs into an AMC compatible carrier board and provides a high speed Serial RapidIO, SGMII and IPMB-I2C interfaces to the carrier board. This connector is the 170 pin B+ style. The signals on this connector are shown in the table below:

Table 10: AMC Edge Connector

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground Signal	170	GND	Ground Signal
2	VCC12	+12V Power	169	NC	
3	PS1#	Presence 1	168	NC	
4	MP	Management Power	167	NC	
5	GA0	Geographic Address 0	166	NC	
6	NC		165	NC	
7	GND	Ground Signal	164	GND	Ground Signal
8	NC		163	NC	
9	VCC12	+12V Power	162	NC	
10	GND	Ground Signal	161	GND	Ground Signal
11	P4_SGMII_TXP		160	NC	
12	P4_SGMII_TXN		159	NC	
13	GND	Ground Signal	158	GND	Ground Signal
14	P4_SGMII_RXP		157	NC	
15	P4_SGMII_RXN		156	NC	
16	GND	Ground Signal	155	GND	Ground Signal
17	GA1	Geographic Address 1	154	NC	
18	VCC12	+12V Power	153	NC	
19	GND	Ground Signal	152	GND	Ground Signal
20	NC		151	NC	
21	NC		150	NC	
22	GND	Ground Signal	149	GND	Ground Signal
23	NC		148	NC	
24	NC		147	NC	
25	GND	Ground Signal	146	GND	Ground Signal
26	GA2	Geographic Address 2	145	NC	
27	VCC12	+12V Power	144	NC	
28	GND	Ground Signal	143	GND	Ground Signal
29	NC		142	NC	
30	NC		141	NC	
31	GND	Ground Signal	140	GND	Ground Signal
32	NC		139	NC	
33	NC		138	NC	
34	GND	Ground Signal	137	GND	Ground Signal
35	NC		136	NC	
36	NC		135	NC	
37	GND	Ground Signal	134	GND	Ground Signal
38	NC		133	NC	
39	NC		132	NC	
40	GND	Ground Signal	131	GND	Ground Signal
41	ENABLE#	Enable Signal	130	I2C_SDA	I2C_SDA
42	VCC12	+12V Power	129	I2C_SCL	I2C_SCL
43	GND	Ground Signal	128	GND	Ground Signal

44	NC		127	NC	
45	NC		126	NC	
46	GND	Ground Signal	125	GND	Ground Signal
47	NC		124	NC	
48	NC		123	NC	
49	GND	Ground Signal	122	GND	Ground Signal
50	NC		121	NC	
51	NC		120	NC	
52	GND	Ground Signal	119	GND	Ground Signal
53	NC		118	NC	
54	NC		117	NC	
55	GND	Ground Signal	116	GND	Ground Signal
56	SCL_IPMB		115	NC	
57	VCC12	+12V Power	114	NC	
58	GND	Ground Signal	113	GND	Ground Signal
59	NC		112	NC	
60	NC		111	NC	
61	GND	Ground Signal	110	GND	Ground Signal
62	NC		109	RIOTX_P3	SRIO Port 3-TX
63	NC		108	RIOTX_N3	SRIO Port 3-TX
64	GND	Ground Signal	107	GND	Ground Signal
65	NC		106	RIORX_P3	SRIO Port 3-RX
66	NC		105	RIORX_N3	SRIO Port 3-RX
67	GND	Ground Signal	104	GND	Ground Signal
68	NC		103	RIOTX_P2	SRIO Port 2-TX
69	NC		102	RIOTX_N2	SRIO Port 2-TX
70	GND	Ground Signal	101	GND	Ground Signal
71	SDA_IPMB		100	RIORX_P2	SRIO Port 2-RX
72	VCC12	+12V Power	99	RIORX_N2	SRIO Port 2-RX
73	GND	Ground Signal	98	GND	Ground Signal
74	NC		97	RIOTX_P1	SRIO Port 1-TX
75	NC		96	RIOTX_N1	SRIO Port 1-TX
76	GND	Ground Signal	95	GND	Ground Signal
77	NC		94	RIORX_P1	SRIO Port 1-RX
78	NC		93	RIORX_N1	SRIO Port 1-RX
79	GND	Ground Signal	92	GND	Ground Signal
80	NC		91	RIOTX_P0	SRIO Port 0-TX
81	NC		90	RIOTX_N0	SRIO Port 0-TX
82	GND	Ground Signal	89	GND	Ground Signal
83	PS0#	Presence 0	88	RIORX_P0	SRIO Port 0-RX
84	VCC12	+12V Power	87	RIORX_N0	SRIO Port 0-RX
85	GND	Ground Signal	86	GND	Ground Signal

4.2.3 J3, EMIF Test Header (Footprint Only)

J3 is a test header footprint for 32 bit EMIFA interface of the DSP. The user can mount Samtec Part #SFM-140-L2-S-D-LC or equivalent connector into this footprint. The signal connections to the test header are as shown in the table below:

Table 11: EMIFA Test Header pin out

Pin	Signal	Description	Pin	Signal	Description
1	VCC3.3	+3.3V Power	2	VCC3.3	+3.3V Power
3	GND	Ground Signal	4	GND	Ground Signal
5	EMIF_D00	Data 0	6	EMIF_D08	Data 8
7	EMIF_D01	Data 1	8	EMIF_D09	Data 9
9	EMIF_D02	Data 2	10	EMIF_D10	Data 10
11	EMIF_D03	Data 3	12	EMIF_D11	Data 11
13	EMIF_D04	Data 4	14	EMIF_D12	Data 12
15	EMIF_D05	Data 5	16	EMIF_D13	Data 13
17	EMIF_D06	Data 6	18	EMIF_D14	Data 14
19	EMIF_D07	Data 7	20	EMIF_D15	Data 15
21	GND	Ground Signal	22	GND	Ground Signal
23	EMIF_D16	Data 16	24	EMIF_D24	Data 24
25	EMIF_D17	Data 17	26	EMIF_D25	Data 25
27	EMIF_D18	Data 18	28	EMIF_D26	Data 26
29	EMIF_D19	Data 19	30	EMIF_D27	Data 27
31	EMIF_D20	Data 20	32	EMIF_D28	Data 28
33	EMIF_D21	Data 21	34	EMIF_D29	Data 29
35	EMIF_D22	Data 22	36	EMIF_D30	Data 30
37	EMIF_D23	Data 23	38	EMIF_D31	Data 31
39	GND	Ground Signal	40	GND	Ground Signal
41	EMIF_BA0	Bank Address 0	42	EMIF_BA1	Bank Address 1
43	EMIF_A00	Address 0	44	EMIF_A10	Address 10
45	EMIF_A01	Address 1	46	EMIF_A11	Address 11
47	EMIF_A02	Address 2	48	EMIF_A12	Address 12
49	EMIF_A03	Address 3	50	EMIF_A13	Address 13
51	EMIF_A04	Address 4	52	EMIF_A14	Address 14
53	EMIF_A05	Address 5	54	EMIF_A15	Address 15
55	EMIF_A06	Address 6	56	EMIF_A16	Address 16
57	EMIF_A07	Address 7	58	EMIF_A17	Address 17
59	EMIF_A08	Address 8	60	EMIF_A18	Address 18
61	EMIF_A09	Address 9	62	EMIF_A19	Address 19
63	GND	Ground Signal	64	GND	Ground Signal
65	EMIF_CLKIN	External Input clock	66	EMIF_CE2#	Space Enable 2
67	EMIF_CLKOUT	Output clock	68	EMIF_CE3#	Space Enable 3
69	GND	Ground Signal	70	EMIF_AOE#	Output enable
71	EMIF_BE00#	Byte Enable 0	72	EMIF_SADS#	Address Strobe
73	EMIF_BE01#	Byte Enable 1	74	EMIF_R/W#	Read / Write
75	EMIF_BE02#	Byte Enable 2	76	EMIF_ARDY	Read Input
77	EMIF_BE03#	Byte Enable 3	78	EMIF_AWE#	Write Enable
79	GND	Ground Signal	80	GND	Ground Signal

4.2.4 J4, Ethernet Connector

J4 is a Gigabit RJ45 Ethernet connector with integrated magnetics. It is driven by Marvell Gigabit Ethernet switch 88E6122. The connections are shown in a table below:

Table 12: Ethernet Connector pin out

Pin #	Signal Name
1	Center Tap 2
2	MD2-
3	MD2+
4	MD1-
5	MD1+
6	Center Tap 1
7	Center Tap 3
8	MD3+
9	MD3-
10	MD0-
11	MD0+
12	Center Tap 0
13	LED1-
14	LED1+
15	LED2-
16	LED2+
17	Shield 1
18	Shield 2

4.2.5 J5, TI 60 Pin DSP JTAG Connector

J5 is a high speed system trace capable TI 60 pin JTAG connector for XDS560v2 type of DSP emulation. The onboard switch multiplexes this interface with the on-board XDS100 type emulator. Whenever an external emulator is plugged into J5, the external emulator connects with the DSP. The I/O voltage level on these pins is 1.8V. So any 1.8V level compatible emulator can be used to interface with the C6457 DSP. It should be noted that when an external emulator is plugged into this connector (J5), onboard XDS100 type emulation circuitry will be disconnected from the DSP. The pin out for the connector is shown in table below:

Table 13: DSP JTAG Connector pin out

Pin #	Signal Name	Pin #	Signal Name
B1	ID0	D1	NC
A1	Ground	C1	ID2
B2	TMS	D2	Ground
A2	Ground	C2	EMU18
B3	EMU17	D3	Ground
A3	Ground	C3	TRST
B4	TDI	D4	Ground
A4	Ground	C4	EMU16
B5	EMU14	D5	Ground
A5	Ground	C5	EMU15
B6	EMU12	D6	Ground
A6	Ground	C6	EMU13
B7	TDO	D7	Ground
A7	Ground	C7	EMU11
B8	TVD	D8	Type1 (Ground)
A8	Type0 (NC)	C8	TCLKRTN
B9	EMU9	D9	Ground
A9	Ground	C9	EMU10
B10	EMU7	D10	Ground
A10	Ground	C10	EMU8
B11	EMU5	D11	Ground
A11	Ground	C11	EMU6
B12	TCLK	D12	Ground
A12	Ground	C12	EMU4
B13	EMU2	D13	Ground
A13	Ground	C13	EMU3
B14	EMU0	D14	Ground
A14	Ground	C14	EMU1
B15	ID1	D15	Ground
A15	TRGRSTz	C15	ID3

4.2.6 J6, MSP430 Reset, 2-Pin header (For Factory Use Only)

J6 is 2-pin male header to Reset MSP430. By shorting both the pins, MSP430 will go into reset.

The pin out for the connector is shown in the table below:

Table 14: MSP430 Reset Connector pin out

Pin #	Signal Name
1	Enable
2	Ground

4.2.7 J7, MSP430 JTAG Connector (For Factory Use Only)

J7 is a 14 pin JTAG connector for IPMI software loading into MSP430. The C6457 lite EVM are supplied with IPMI software already loaded into MSP430. The pin out for the connector is shown in the table below:

Table 15: MSP430 JTAG Connector pin out

Pin #	Signal Name	Pin #	Signal Name
1	TDO	8	TEST
2	VCCTOOL (NC)	9	Ground
3	TDI	10	NC
4	VCC	11	RESET#
5	TMS	12	NC
6	No Pin (**Key**)	13	NC
7	TCK	14	NC

4.2.8 J8, MSP430 Power Selection, 3-Pin Connector (For Factory Use Only)

J8 is 3-pin male connector for MSP430 Power Selection. By shorting Pin 2 with Pin 1, MSP430 will be powered from AMC Carrier back-plane (Default) and by shorting Pin 2 with Pin3; MSP430 can be made to power from On-Board 3.3V regulator.

The pin out for the connector is shown in the table below:

Table 16: UART Connector pin out

Pin #	Signal Name
1	AMC 3.3V Power
2	MSP430 Power
3	On-Board 3.3V Power

4.2.9 J10, DC Power Input Jack Connector

J10 is a DC Power-in Jack Connector for the stand-alone application of the C6457 lite EVM. It is a 2.5mm power jack with positive center tip polarity. Do not use this connector if EVM is inserted into MicroTCA chassis or AMC carrier back-plane.

4.2.10 J11, Mini-B USB Connector

In TMDSEVM6457L, J11 is available to connect CCS with C6457 DSP using on-board XDS100 type emulation circuitry as well as to access UART-over-USB. In TMDSEVM6457LE, J11 is available for UART-over-USB only.

The pin out for the connector is shown in the table below.

Table 17: Mini-B USB Connector pin out

Pin #	Signal Name
1	VBUS
2	D-
3	D+
4	ID (NC)
5	Ground

4.2.11 J12, UART 3-Pin Connector

J12 is 3-pin male connector for RS232 serial interface. A 3-Pin female to 9-Pin DTE female, cable is supplied with C6457 lite EVM to connect with the PC. The pin out for the connector is shown in the table below:

Table 18: UART Connector pin out

Pin #	Signal Name
1	Ground
2	Transmit
3	Receive

4.2.12 J13, UART Route Select Connector

UART port can be accessed either through Mini-USB connector (J11) or through 3-pin RS232 Serial port header (J12). The selection can be made through UART route select connector J13 as follows:

- UART over USB Connector (Default): Shunts installed over J13.3-J13.1 and J13.4 -J13.2
- UART over 3-Pin Header J4 - Shunts installed over J13.3-J13.5 and J13.4 -J13.6

The pin out for the connector is shown in the table below:

Table 19: UART Path Select Connector pin out

Pin #	Signal Name	Pin #	Signal Name
1	FT2232H(USB Chip) Transmit	2	FT2232H(USB Chip) Receive
3	UART Transmit	4	UART Receive
5	MAX3221 Transmit	6	MAX3221 Receive

4.2.13 J14, FPGA JTAG Connector

J14 is a 10 pin JTAG connector for FPGA debugging and programming only. The pin out for the connector is shown in the table below:

Table 20: FPGA JTAG Connector pin out

Pin #	Signal Name
1	TCK
2	GND
3	TDO
4	NC
5	TMS
6	VJTAG
7	VPUMP
8	TRST#
9	TDI
10	GND

4.2.14 J1, Mini-AB USB Connector – In TMDSEVM6457LE only

Mini-AB USB connector (J1) mounted on Mezzanine Card, is available to connect EVM to CCS for XDS560v2 type emulation. The pin out for the connector is shown in the table below.

Table 21: Mini-AB USB Connector pin out

Pin #	Signal Name
1	VBUS
2	D-
3	D+
4	ID
5	Ground

4.3 Switches

The C6457 lite EVM has two push button switches and two sliding actuator DIP switches. The SW1 and SW2 are push button switches while SW3 and SW4 are DIP switches. The function of each of the switches is listed in the table below:

Table 22: C6457 Lite EVM Board Switches

Switch	Function
SW1	Cold Reset
SW2	Warm Reset
SW3	DSP Configuration
SW4	DSP Boot mode, User Switch

4.3.1 SW1, Cold Reset

Push button Switch SW1 asserts DSP's POR# input and global board reset when pressed. This is equivalent to a power cycle of the board and will have following effects:

- Reset DSP
- Reset FPGA
- Reset Ethernet Switch
- Reset I2C-UART bridge
- Reload boot parameters.

4.3.2 SW2, Warm Reset

Push button Switch SW2 asserts DSP's RESET# input when pressed. This will reset the DSP and boot parameters will be reloaded.

Re-launch and/or re-connect of CCS application may be required after pressing warm or cold reset buttons.

Note: User may refer to TMS320C6457 datasheet to check the difference between assertion of DSP RESET# and DSP POR# signals.

4.3.3 SW3, DSP Configuration

SW3 is an 8 position DIP switch, which is used for DSP configuration. A diagram of SW3 switch (with factory default settings) is shown below:

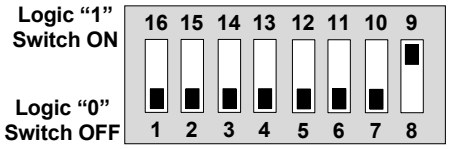

Figure 4.3: SW3 default settings

The following table describes the positions and corresponding function on SW1.

Table 23: SW3, DSP Configuration Switch

SW3 Position	Description	Default Value	Function
5 - 1	CFGG[4:0]	00000	DSP Configuration selection Pins
6	HPIWIDTH	0(OFF)	OFF – 16 bit wide bus ON – 32 bit wide bus
7	ECLKINSEL	0(OFF)	OFF – ECLKIN (External Clock) ON – SYSCLK7 (Internal clock)
8	LENDIAN	1(ON)	OFF - Big Endian mode ON - Little Endian mode

4.3.4 SW4, DSP Boot mode

SW4 is an 8 position DIP switch, which is used for DSP boot mode selection, device number and as a 2 position User Switch after DSP Boot. A diagram of the SW4 switch (with factory default settings) is shown below:

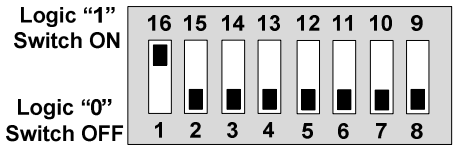

Figure 4.4: SW4 default settings

The following table describes the positions and corresponding function on SW4.

Table 24: SW4, DSP Boot Mode Selection Switch

SW4 Position	Description	Default Value	Function
4 - 1	Boot Mode[3:0]	0001	Boot mode selection pins for DSP. Master I2C boot mode for I2C address 50h Refer to TMS320C6457 datasheet for details of other boot modes supported.
8 – 5 *	Device Number [3:0]	0000	Device number selection for multiple DSPs and position 7 and 8 as User Switch-1 and User Switch-2 respectively after DSP boot.

Note: Please change Boot Mode[3:0] to "0010" for NAND boot mode of this EVM. "0010" is primarily a Master I2C boot mode for I2C address 51h for DSP, which works as NAND boot mode in this EVM.

* - SW4 position 7 and 8 is also configured as User Switch-1 and User Switch-2 respectively (after DSP boot). FPGA monitors status of the user switches and stores its value into internal FPGA registers. The DSP can read user switches' value by accessing FPGA's internal registers.

4.4 Test Points

TMS320C6457 Board has 26 test points. The position of each test point is shown in the figure below:

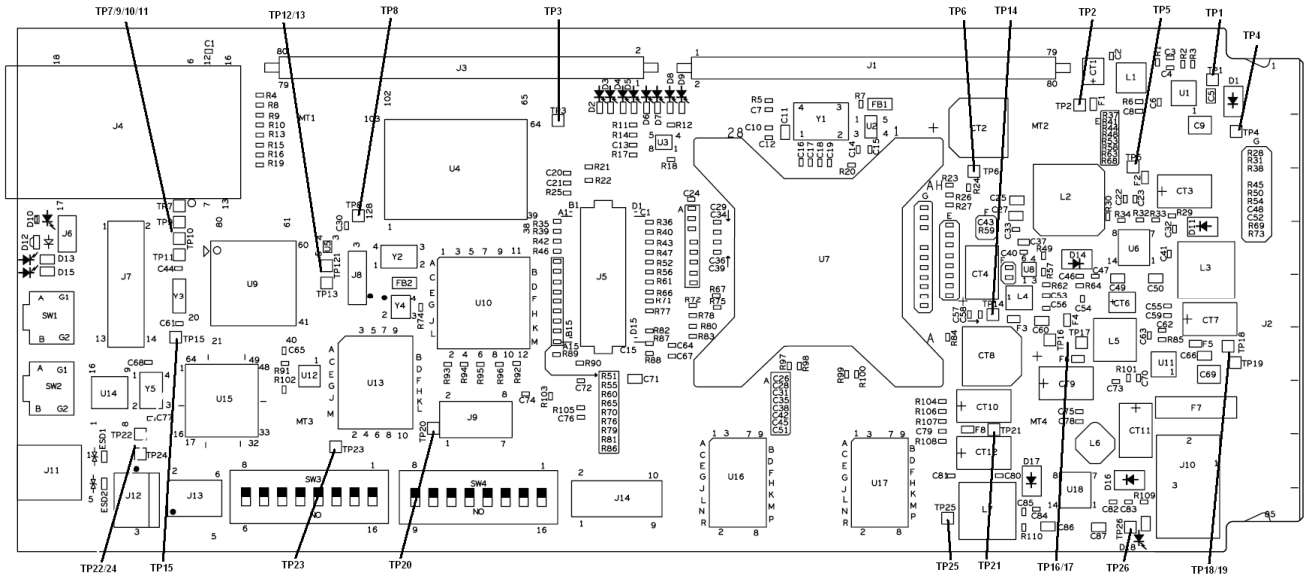

Figure 4.5: Board Test Points [5]

Note: [5] - Some of these TPs may not be visible in TMDSEVM6457LE

Table 25: TMS320C6457 Board Test Points

Test Point	Signal	Test Point	Signal
TP1	Management Power (+3.3V)	TP14	+1.5 Supply
TP2	+2.5V Supply	TP15	FT2232H, PWREN#
TP3,TP4,TP7, TP19,TP20,TP25	Ground	TP16	CVDD Supply (+1.1V)
TP5	+1.8V Supply	TP17	+1.1V Supply
TP6	System Clock Out	TP18	+5V Supply
TP8	DSP (Warm) Reset	TP21	+3.3V Supply
TP9	MSP430 MCLK	TP22	FT2232H, SUSPEND#
TP10	MSP430 ACLK	TP23	FT2232H, GPIOH0
TP11	MSP430 SMCLK	TP24	FT2232H, GPIOH1
TP12	Enable#	TP26	+12V Input Supply
TP13	System (Cold) Reset		

4.5 System LEDs

The C6457 lite EVM board has 13 LEDs. Their positions on the board are indicated in figure 4.6 and their descriptions are listed in table 26.

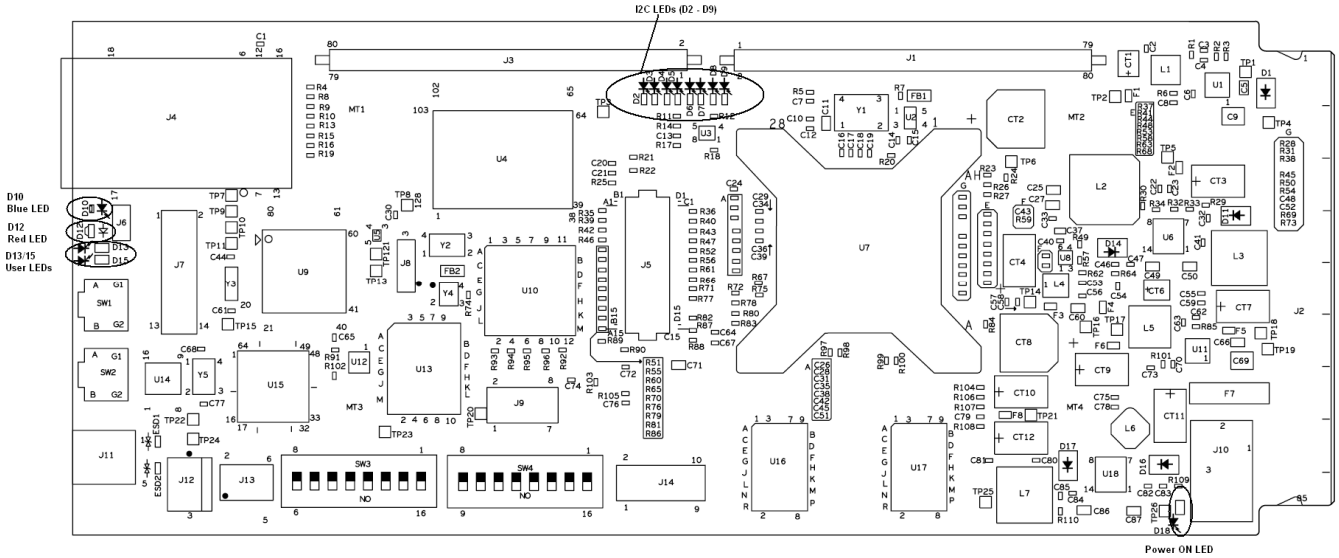

Figure 4.6: TMS320C6457 Board LEDs

Table 26: TMS320C6457 Board LEDs

LED#	Color	Description
D2 – D9	Green	I2C LEDs
D10	Blue	Hot Swap status in AMC chassis
D12	Red	Failure and Out of service status in AMC chassis
D13, D15	Orange	User LEDs
D18	Green	Board Powered ON Indicator

Additional LEDs on TMDSEVM6457LE board are highlighted in figure 4.7 and their description is listed in table 28.

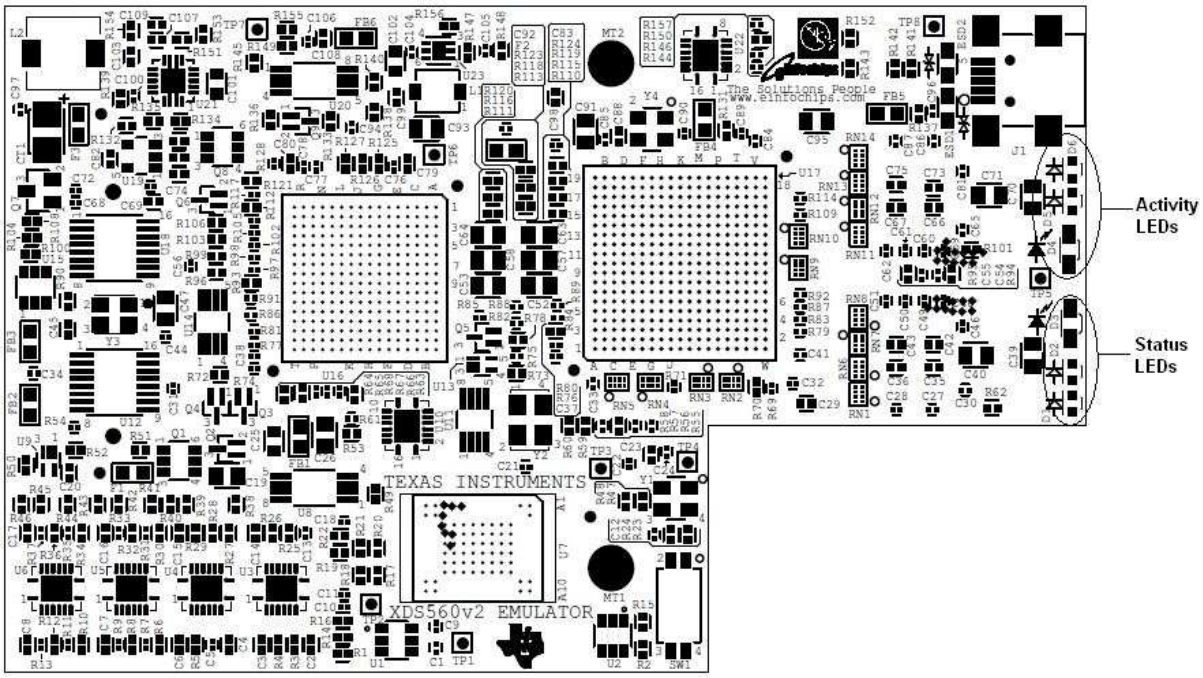

Figure 4.7: TMDSEVM6457LE Board Additional LEDs

Table 27: TMDSEVM6457LE Board Additional LEDs

LED#	Color	Description
D1 (Activity LED 1)	Red	ON - DTC Ready OFF - DTC Not Ready
D2 (Activity LED 2)	Yellow	ON - FPGA Programmed OFF - FPGA Not Programmed
D3 (Activity LED 3)	Green	Reserved
D4 (Status LED 3)	Green	ON =CCS Connected OFF= CCS Disconnected
D5 (Status LED 2)	Yellow	DTC to Host Activity
D6 (Status LED 1)	Orange	Target to DTC Trace Activity

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements. Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Product Applications

Amplifiers	http://amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265