K2L SCHEMATICS

MAJOR REVISION HISTORY :

PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	1.0	Pre-Proto Build	24-Dec-2013
2.0	2.06	Beta Build	02-Sep-2014
3.0	3.03	Production Build	24-Nov-2014

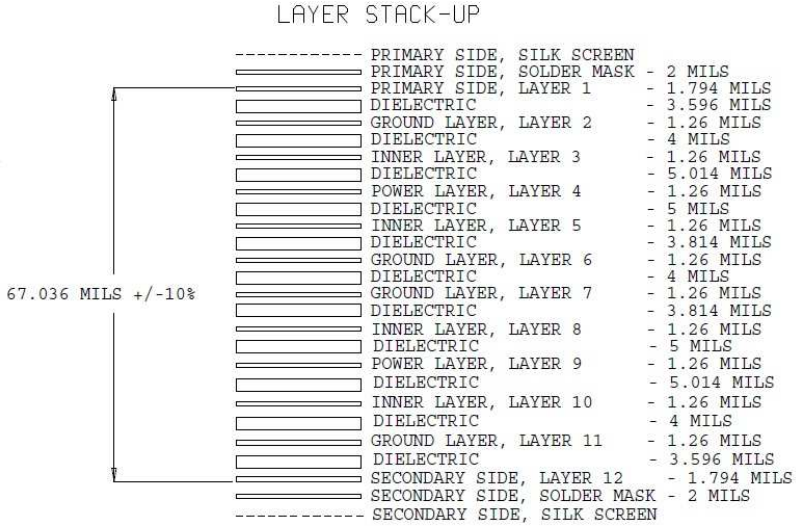
I2C ADDRESS TABLE :

REF DES	DESCRIPTION	7 BIT ADDRESS
EEPROM1	IC EEPROM 1MBIT 1MHZ 8SO	0x50
U40	IC SPD EEPROM 2KBIT 400KHZ 8TSSOP	0x53

PCB MECHANICAL DETAILS :

1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. PCB MATERIAL: TBD
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

PCB LAYER STACK-UP DETAILS :



NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.

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Title: COVER PAGE		Texas Instruments / eInfochips The Solutions People
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SCHEMATIC PAGE CONTENT

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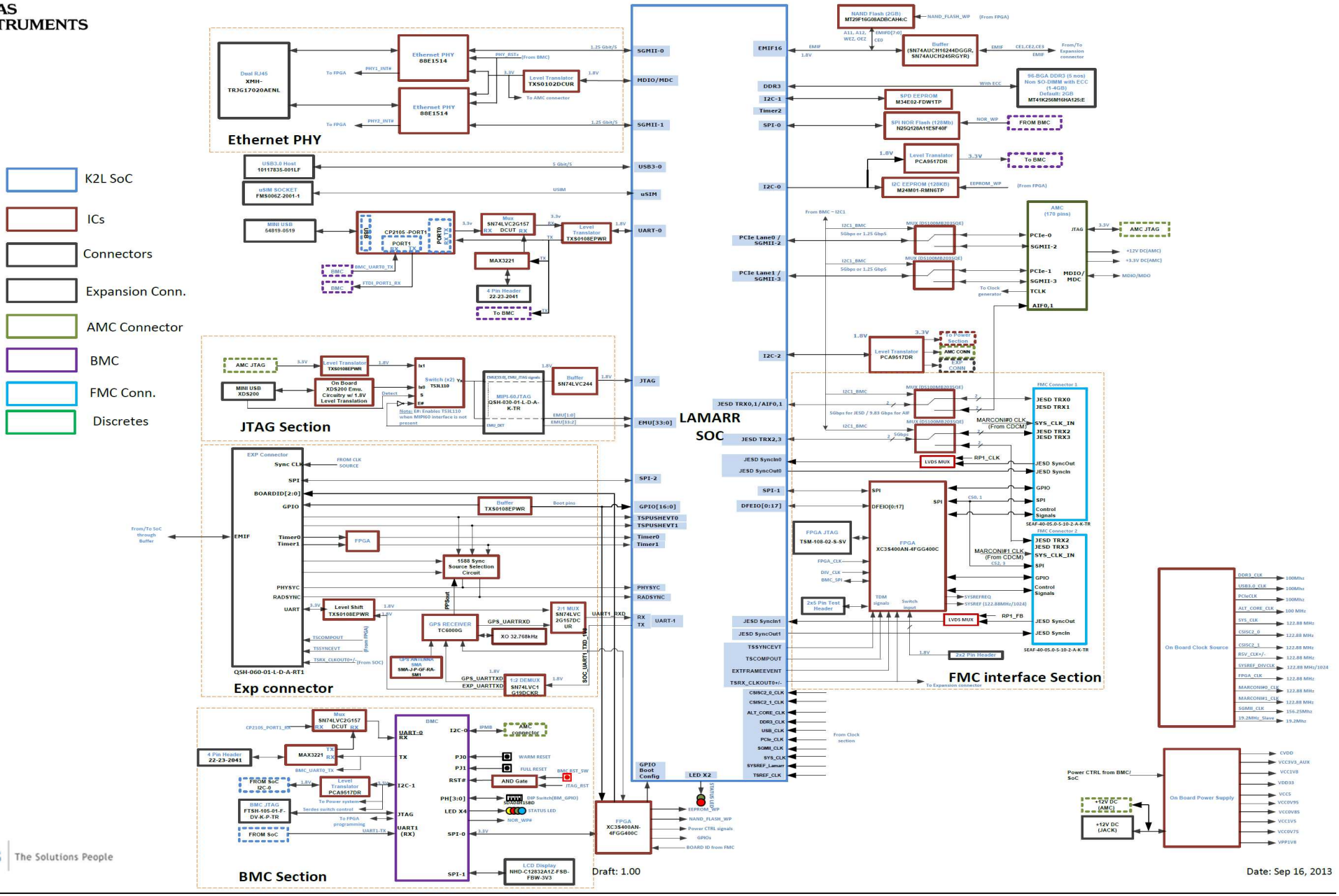
K2L EVM BLOCK DIAGRAM

TI Information-Selective Disclosure



Project: K2L EVM		Designed for TI by eInfochips
Title: BLOCK DIAGRAM		
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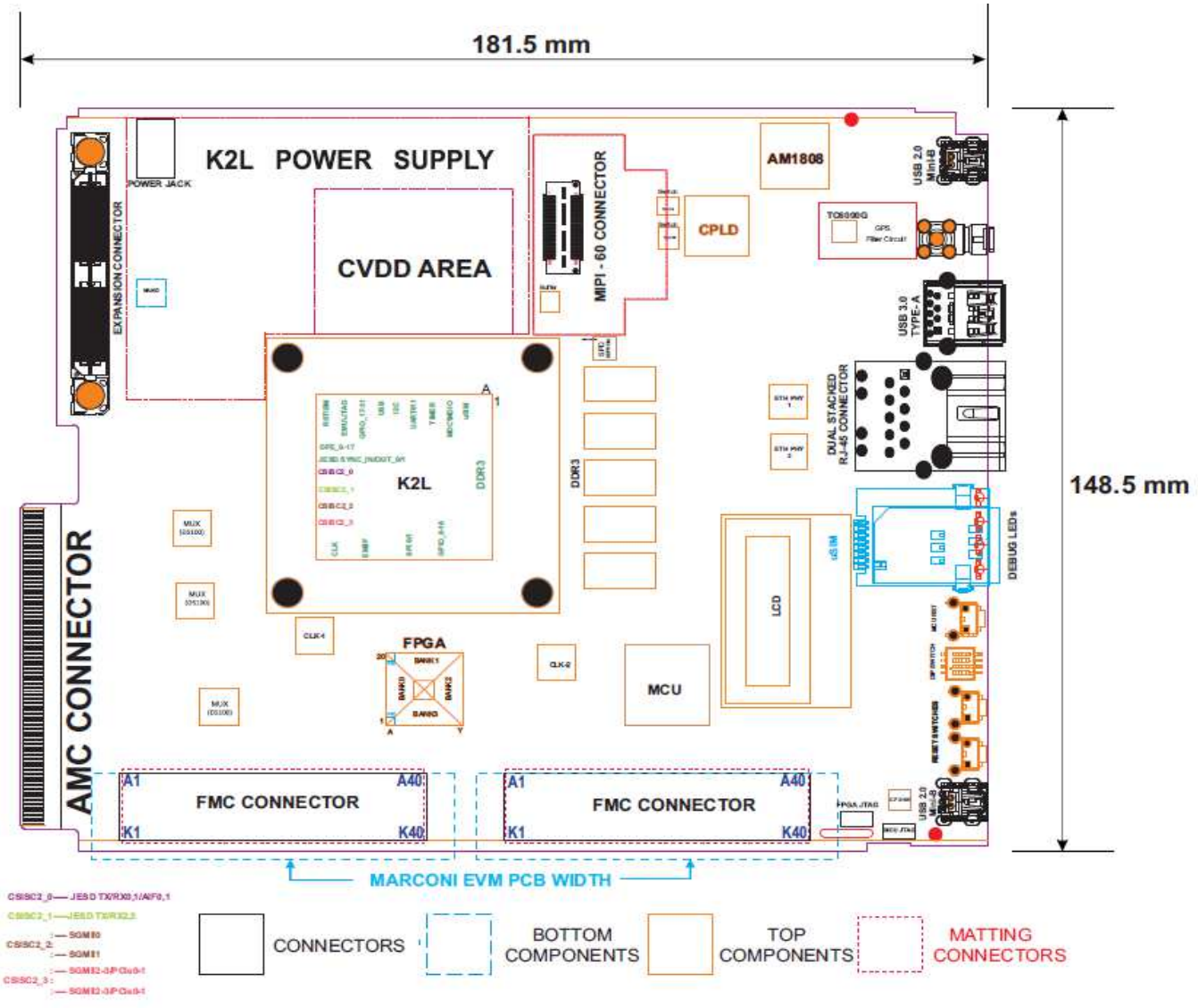
PLACEMENT



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POWER CONSUMPTION

Approx Power Consumption for TI_EVM -Lamarr

Components Part No.	Description	Quantity Per Board	Current Consumed by corresponding device on power supply (mA)													Total Power (mW)
			0.75	0.85 Analog	0.85 USB	0.95 Fixed DSP+ARM	1 AVS(DSP+ARM)	1.2	1.5	1.8 Digital	1.8 Analog	3	3.3	5	12	
Marconi Connector	2 Nos of Marconi EVM	2													1500	18000
Lammar (K2L) Part	TI- Multicore DSP with ARM Core	1		700	800	2900	18800		800	400	600		25			25912.5
MT41K256M16HA125:E	IC, DDR3, 4Gb (256Mx16)	5	1000						3000							5250
LM3S2D93	Microcontroller	1											135			445.5
88E1512	Gigabit ethernet phy	2											426			1405.8
MT29F16G16ADBCA	Nand Flash	1								40						72
N25Q128A11ESF40F	SPI NOR	1								20						36
LCD	LCD display	1										45				135
CDCM6208	Reference Clock generator	2											636			2098.8
MCP23S17T-E/SS	IC I/O EXPANDER SPI 16B 28SSOP	5								16			4			42
XDS200 circuitry (referred from K@E)	XDS200 circuitry	1												136		680
TXS4555RGTR	SIM translaor	1								5			50			174
CP2105	IC USB to DUAL UART	1											45			148.5
XC3S400AN-4FGG400C	IC SPARTAN 3AN FGG400 FPGA	1						90		275			409			1952.7
TC6000G	GPS Receiver	1								83						149.4
USB3.0 connector	USB 3.0	1												900		4500
DS100MB203SQE/NOPB	JESD and PCIe switch	4											828			2732.4
FAN		1													100	1200
UCD9090		1											60			198
Others	Other Ics	1								600			300			2070
Total Current on individual power supply (mA)			1000	700	800	2900	18800	90	3800	1439	600	45	2918	1036	1600	
6.5% margin added over design (mA)			1065	745.5	852	3088.5	20022	95.85	4047	1532.535	639	47.925	3107.67	1103.34	1704	
Power Consumption in (mW)			798.75	633.675	724.2	2934.075	20022	115.02	6070.5	2758.563	1150.2	143.775	10255.311	5516.7	20448	

TPS544C24 -- 12V to 1V regulation	1962.94
LM26430-1(SW1) -- 12V to 0.95V regulation	287.65
TLV1117-33CDCY -- 12V to 3.3V BMC (LDO) regulation	148.50
TPS54620 -- 12V to 1.5V regulation	751.76
LM26430-1(SW3) -- 12V to 0.85V Analog SoC regulation	62.13
TPS54620-- 12V to 1.8V Analog regulation	112.76
TPS51200 -- 1.5 to 0.75V DDR regulation	1065.00
LM26430-1(SW4) -- 12V to 0.85V USB SoC regulation	71.00
LM26430-1(SW2) -- 12V to 1.8V Digital regulation	240.79
TPS54620 -- 12V to 3.3V Others regulation	1101.76
TPS54620 -- 12V to 5V regulation	540.85
APL431LBAI-TRG -- 3.3V to 3V regulation	47.93
LDO -- 3.3V OTH to 1.2V FPGA (LDO) - regulation	95.85
LDO -- 3.3V OTH to 1.8V FPGA (LDO) - regulation	302.50
Total Current @ 12V	6.98A
Total Power :	83.81W
Total Current @5V	1103.34
Total Current @3.3V	3155.60
Total Current @1.5V	5112.00

Note :

1) Above power consumption considers major block of design and provides indicative figure only.
2) Power rail assignment to different regulator is tentative based on power consumption, this can be changed based on sequence requirement.
3) Total power consumption is system is higher than AMC power(80W), we assume that marconi EVM will be connected only when board is running on external power supply.

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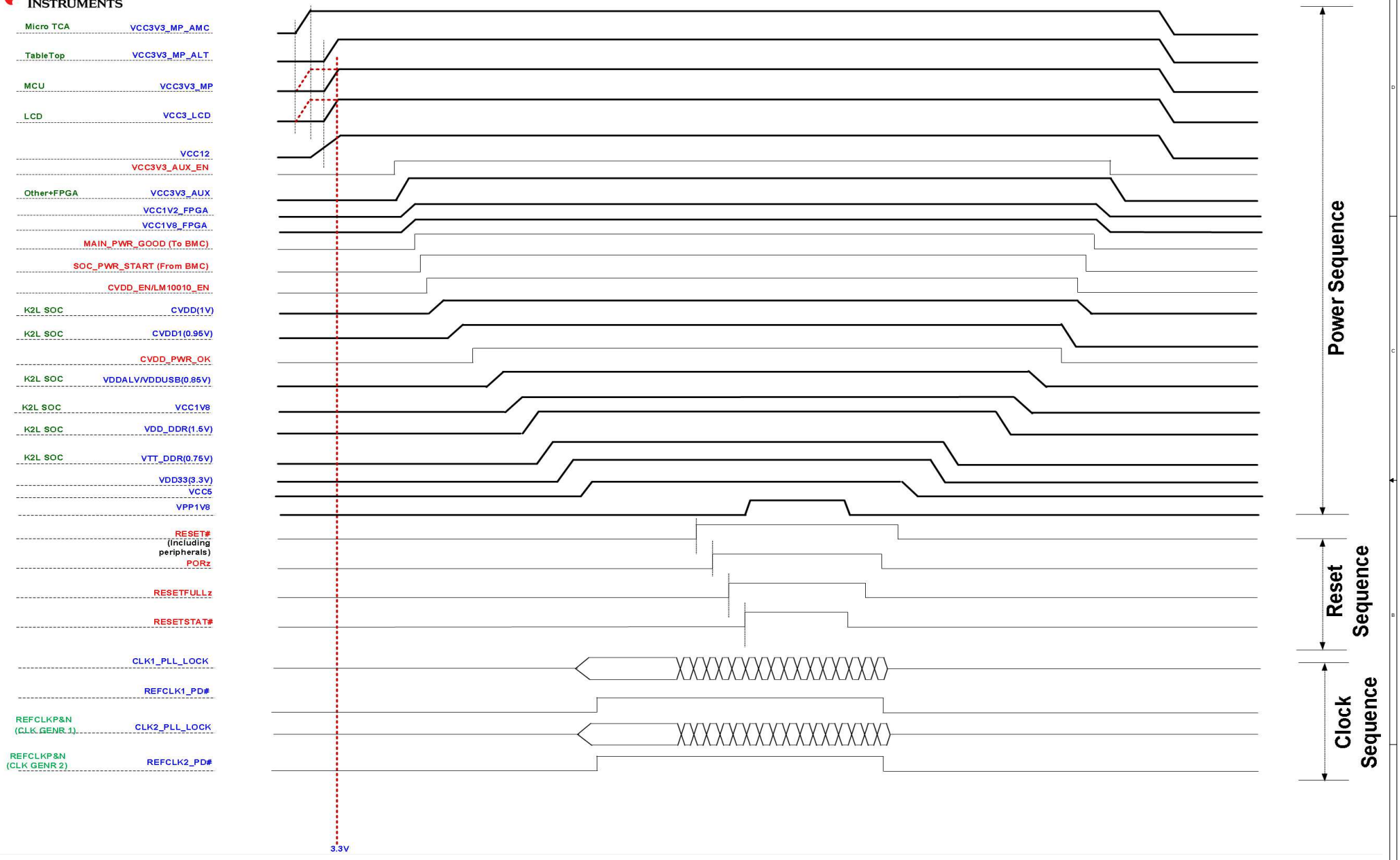
POWER SEQUENCE



Project: K2L EVM		Designed for TI by eInfochips
Title: POWER SEQUENCE		
Size: C	Document Number: 16_00176_03	Rev: 3.03
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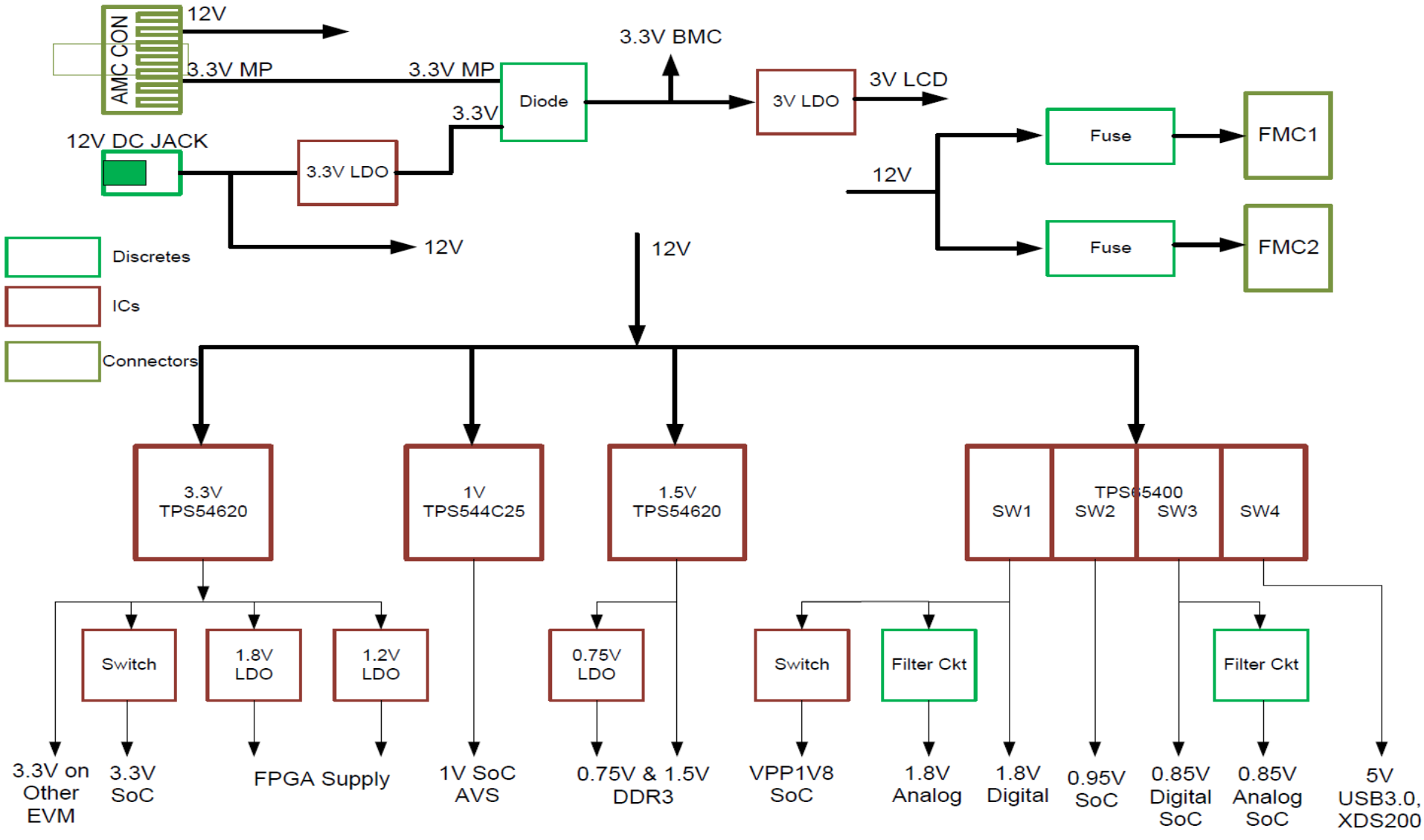
POWER DISTRIBUTION

Power Supply Block Diagram



Project: K2L EVM		Designed for TI by eInfochips
Title: POWER DISTRIBUTION		
Size: C	Document Number: 16_00176_03	Rev: 3.03
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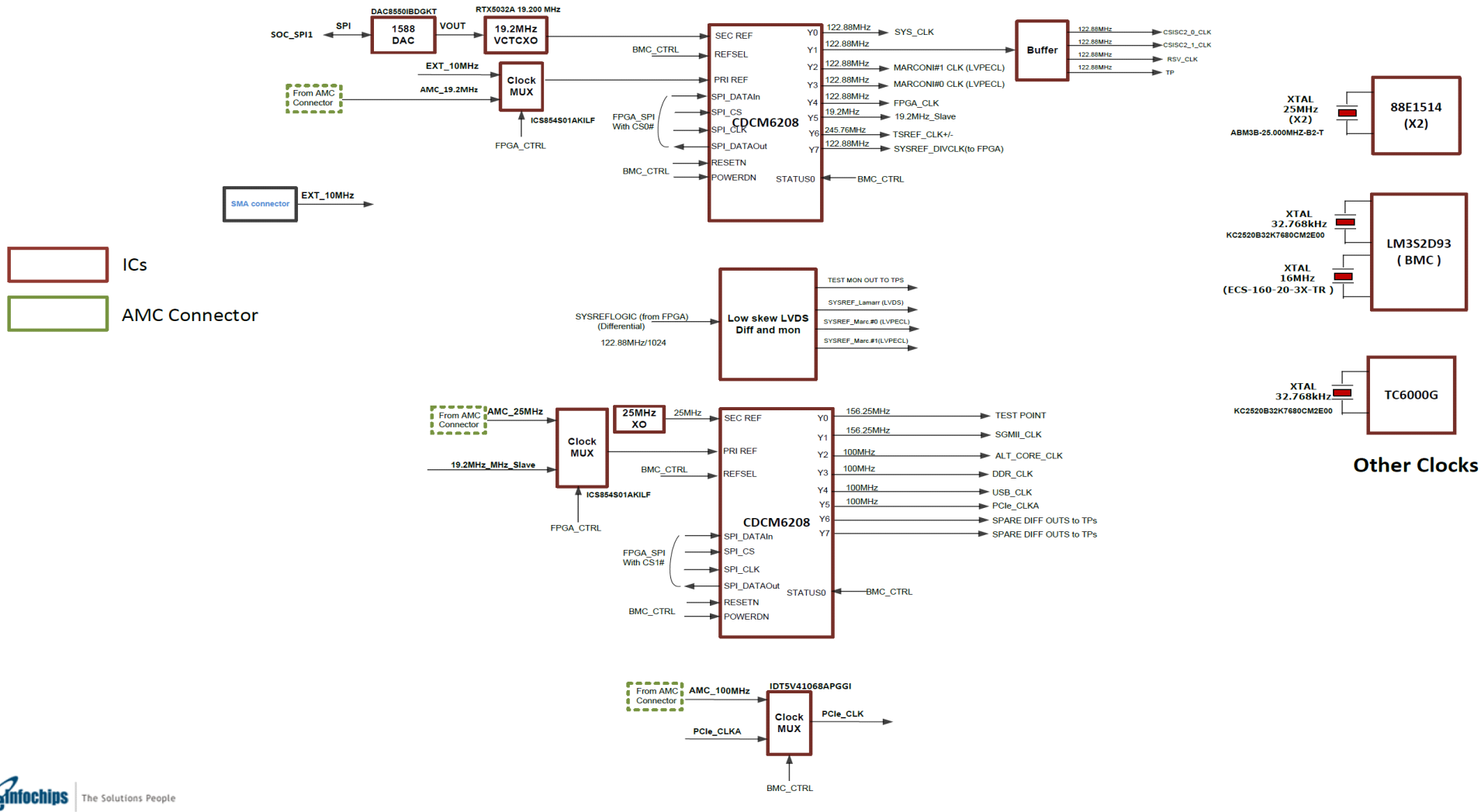
CLOCK DISTRIBUTION

K2L EVM CLOCK DIAGRAM



Project: K2L EVM		Designed for TI by eInfochips
Title: CLOCK DISTRIBUTION		
Size: C	Document Number: 16_00176_03	Rev: 3.03
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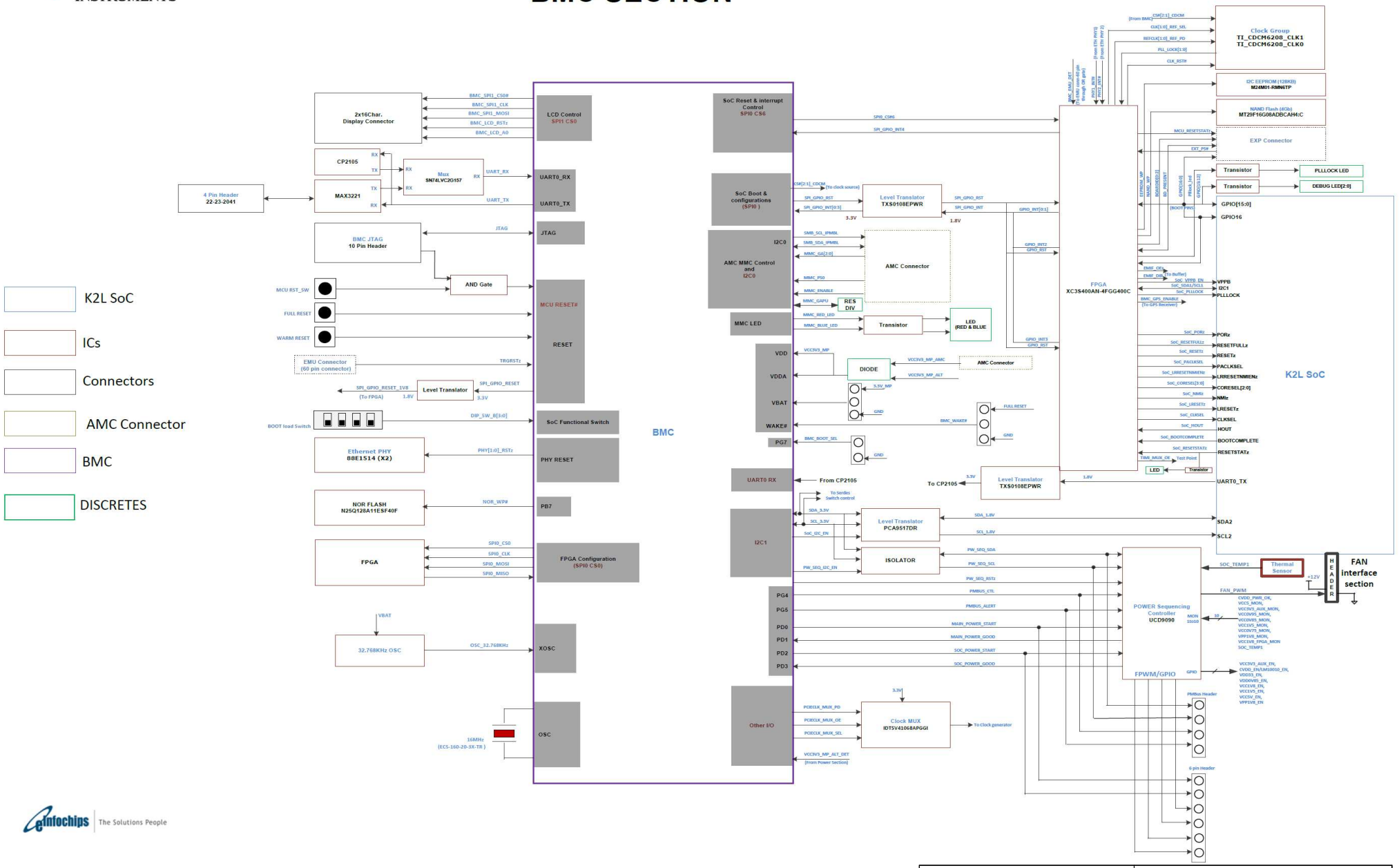
BMC BLOCK DIAGRAM

BMC SECTION



Project: K2E EVM		Designed for TI by eInfochips
Title: BMC BLOCK DIAGRAM		
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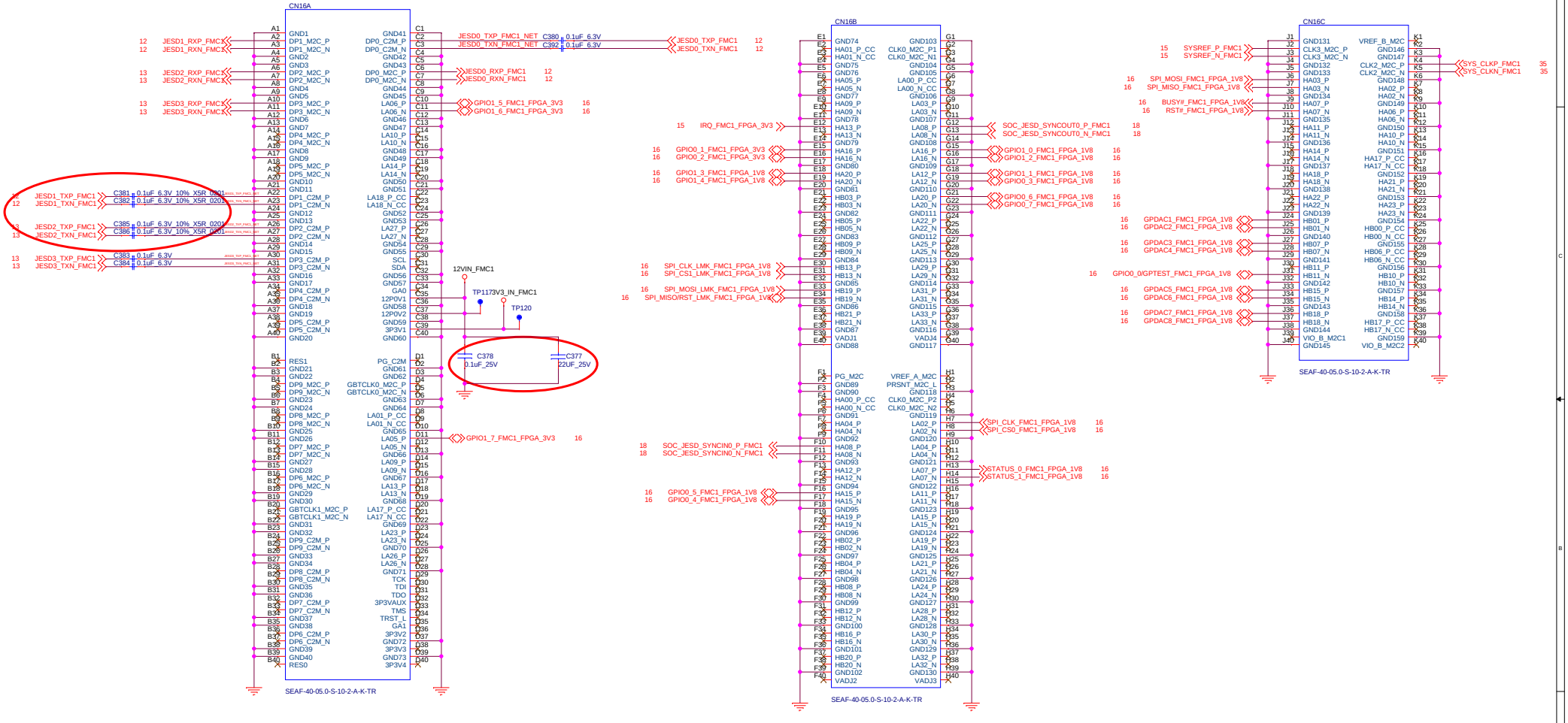
FMC Interface to JESD/RF devices - 1



Project: K2L EVM		Designed for TI by eInfochips
Title: FMC Interface to JESD/RF devices-1		
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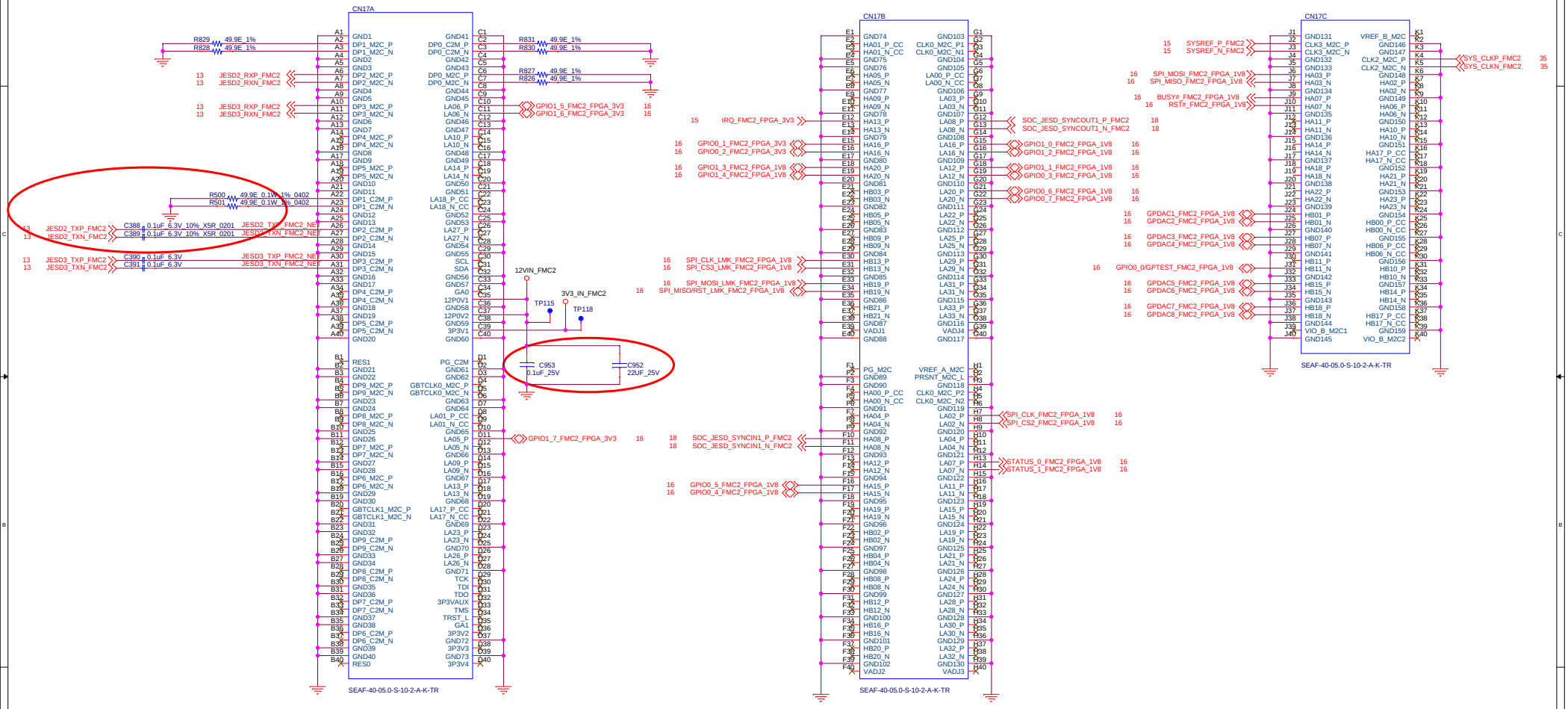
FMC Interface to JESD/RF devices - 2



Project: K2L EVM		Designed for TI by eInfochips
Title: FMC Interface to JESD/RF devices - 2		
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JESD Serdes switch - 1

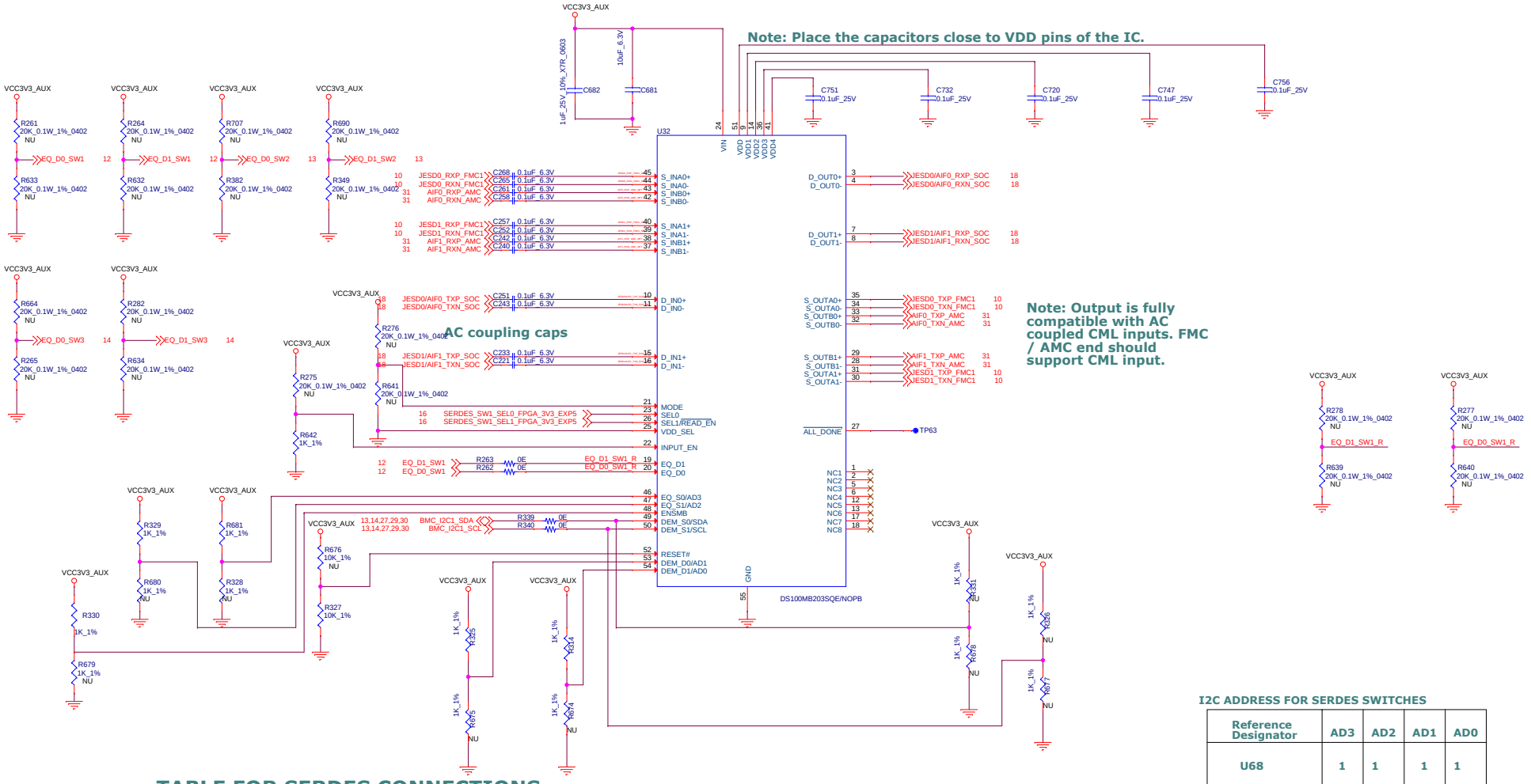

TABLE FOR SERDES CONNECTIONS

Lamarr Ballname	Lamarr Direction	Lamarr Ball	Lamarr SOC Net name to switch	Sw/SOC	Switch Inputs	Switch Outputs	FMC1 Name	FMC1 Pin	FMC2 Name	FMC2 Pin	Marconi Name	AMC Name	AMC Pin
CSISC2_0_RXN0	Diff In	AJ19	JESD0/AIF0_RXN_SOC	Sw Out	JESD0_RXN_FMC1 or AIF0_RXN_AMC	-	JESD0_RXN_FMC1	C7			TXN_S1	AIF0_RXN_AMC	141
CSISC2_0_RXP0	Diff In	AJ18	JESD0/AIF0_RXP_SOC	Sw Out	JESD0_RXP_FMC1 or AIF0_RXP_AMC	-	JESD0_RXP_FMC1	C6			TXP_S1	AIF0_RXP_AMC	142
CSISC2_0_RXN1	Diff In	AK20	JESD1/AIF1_RXN_SOC	Sw Out	JESD1_RXN_FMC1 or AIF1_RXN_AMC	-	JESD1_RXN_FMC1	A3			TXN_S2	AIF1_RXN_AMC	147
CSISC2_0_RXP1	Diff In	AK19	JESD1/AIF1_RXP_SOC	Sw Out	JESD1_RXP_FMC1 or AIF1_RXP_AMC	-	JESD1_RXP_FMC1	A2			TXP_S2	AIF1_RXP_AMC	148
CSISC2_0_TXN0	Diff Out	AH17	JESD0/AIF0_TXN_SOC	Sw In		JESD0_TXN_FMC1 or AIF0_TXN_AMC	JESD0_TXN_FMC1	C3	NU	C3	RXN_S1	AIF0_TXN_AMC	144
CSISC2_0_TXP0	Diff Out	AH18	JESD0/AIF0_TXP_SOC	Sw In		JESD0_TXP_FMC1 or AIF0_TXP_AMC	JESD0_TXP_FMC1	C2	NU	C2	RXP_S1	AIF0_TXP_AMC	145
CSISC2_0_TXN1	Diff Out	AG18	JESD1/AIF1_TXN_SOC	Sw In		JESD1_TXN_FMC1 or AIF1_TXN_AMC	JESD1_TXN_FMC1	A27	NU	A27	RXN_S2	AIF1_TXN_AMC	150
CSISC2_0_TXP1	Diff Out	AG19	JESD1/AIF1_TXP_SOC	Sw In		JESD1_TXP_FMC1 or AIF1_TXP_AMC	JESD1_TXP_FMC1	A26	NU	A26	RXP_S2	AIF1_TXP_AMC	151

I2C ADDRESS FOR SERDES SWITCHES

Reference Designator	AD3	AD2	AD1	AD0
U68	1	1	1	1
U69	1	0	1	1
U70	0	1	1	1

Project: K2L EVM	Designed for TI by eInfochips	
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JESD Serdes switch - 2

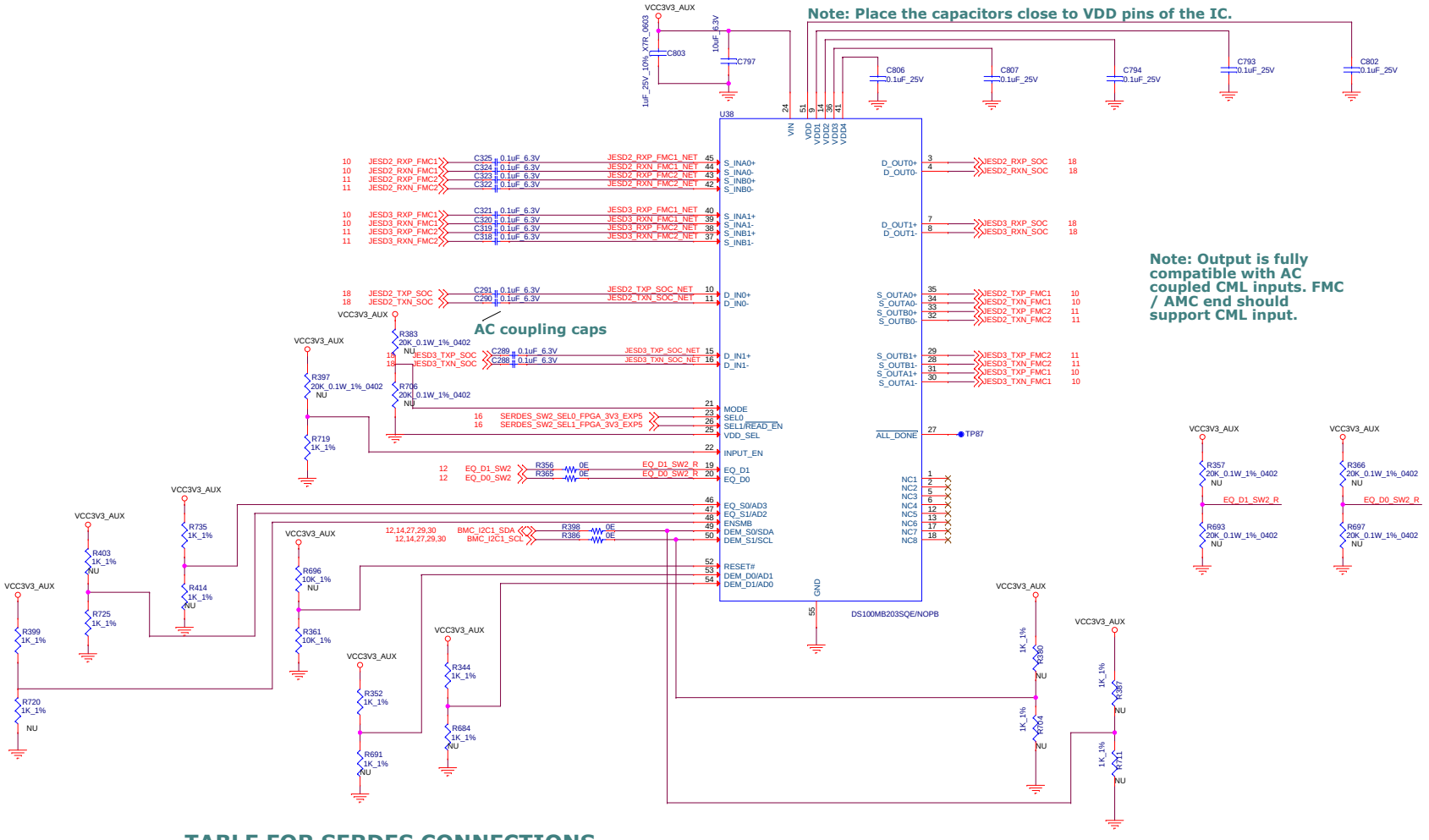

TABLE FOR SERDES CONNECTIONS

Lamarr Ballname	Lamarr Direction	Lamarr Ball	Lamarr SOC Net name to switch	Sw/SOC	Switch Inputs	Switch Outputs	FMC1 Name	FMC1 Pin	FMC2 Name	FMC2 Pin	Marconi Name
CSISC2_1_RXN0	Diff In	AJ16	JESD2_RXN_SOC	Sw Out	JESD2_RXN_FMC1 or JESD2_RXN_FMC2	-	JESD2_RXN_FMC1	A7	JESD2_RXN_FMC2	A7	TXN_S3
CSISC2_1_RXP0	Diff In	AJ15	JESD2_RXP_SOC	Sw Out	JESD2_RXP_FMC1 or JESD2_RXP_FMC2	-	JESD2_RXP_FMC1	A6	JESD2_RXP_FMC2	A6	TXP_S3
CSISC2_1_RXN1	Diff In	AK17	JESD3_RXN_SOC	Sw Out	JESD3_RXN_FMC1 or JESD3_RXN_FMC2	-	JESD3_RXN_FMC1	A11	JESD3_RXN_FMC2	A11	TXN_S4
CSISC2_1_RXP1	Diff In	AK16	JESD3_RXP_SOC	Sw Out	JESD3_RXP_FMC1 or JESD3_RXP_FMC2	-	JESD3_RXP_FMC1	A10	JESD3_RXP_FMC2	A10	TXP_S4
CSISC2_1_TXN0	Diff Out	AH14	JESD2_TXN_SOC	Sw In	-	JESD2_TXN_FMC1 or JESD2_TXN_FMC2	JESD2_TXN_FMC1	A23	JESD2_TXN_FMC2	A23	RXN_S3
CSISC2_1_TXP0	Diff Out	AH15	JESD2_TXP_SOC	Sw In	-	JESD2_TXP_FMC1or JESD2_TXP_FMC2	JESD2_TXP_FMC1	A22	JESD2_TXP_FMC2	A22	RXP_S3
CSISC2_1_TXN1	Diff Out	AG15	JESD3_TXN_SOC	Sw In	-	JESD3_TXN_FMC1 or JESD3_TXN_FMC2	JESD3_TXN_FMC1	A31	JESD3_TXN_FMC2	A31	RXN_S4
CSISC2_1_TXP1	Diff Out	AG16	JESD3_TXP_SOC	Sw In	-	JESD3_TXP_FMC1or JESD3_TXP_FMC2	JESD3_TXP_FMC1	A30	JESD3_TXP_FMC2	A30	RXP_S4

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SGMII/PCIe Serdes switch

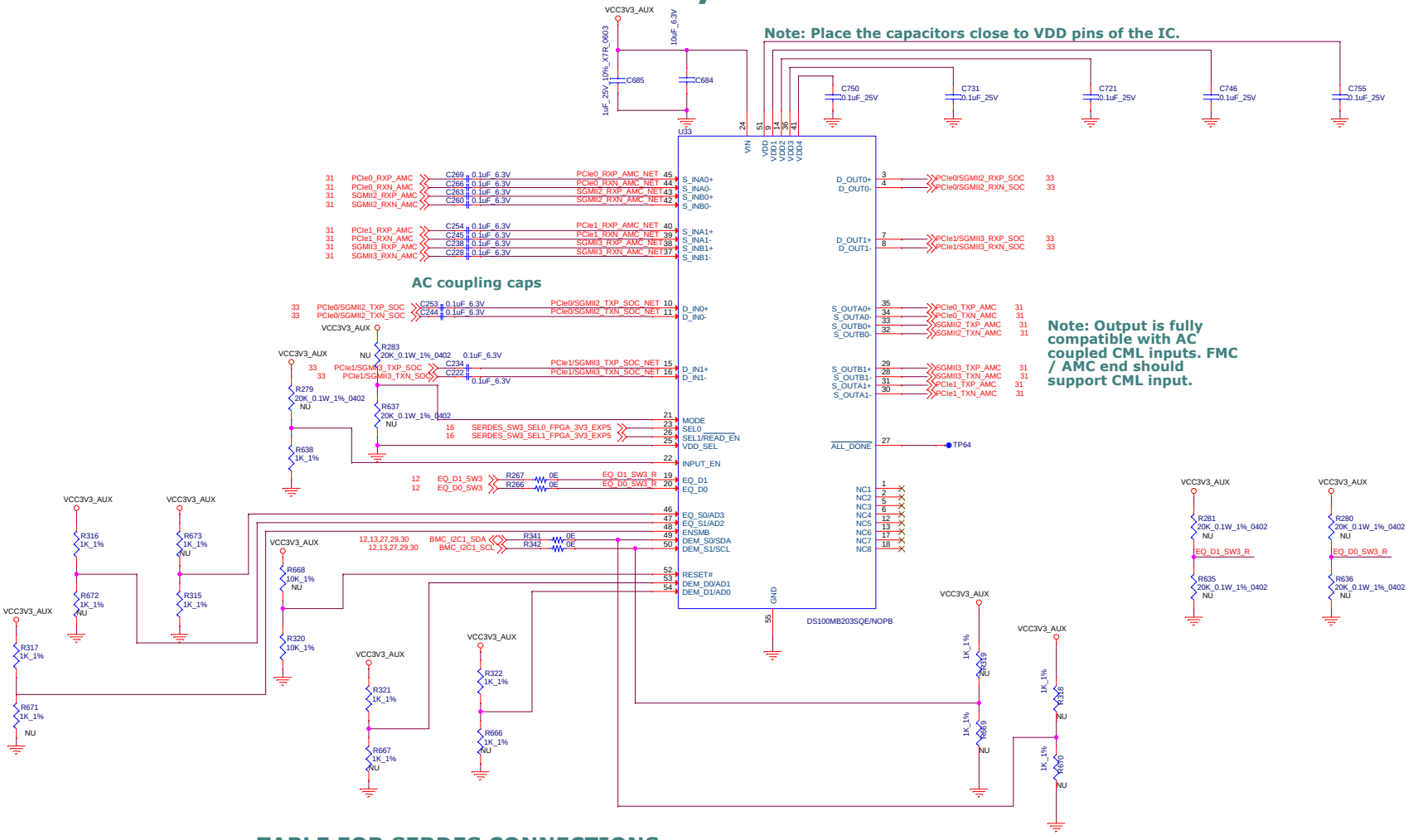

TABLE FOR SERDES CONNECTIONS

Lamarr Ballname	Lamarr Direction	Lamarr Ball	Lamarr SOC Net name to switch	Sw/SOC	Switch Inputs	Switch Outputs	AMC PCIe conn	AMC Pin	AMC SGMII conn	AMC Pin
CSISC2_3_RXN0	Diff In	AJ22	PCIe0/SGMII2_RXN_SOC	Sw Out	PCIe0_RXN_AMC or SGMII2_RXN_AMC	-	PCIe0_RXN_AMC	48	SGMII2_RXN_AMC	15
CSISC2_3_RXP0	Diff In	AJ21	PCIe0/SGMII2_RXP_SOC	Sw Out	PCIe0_RXP_AMC or SGMII2_RXP_AMC	-	PCIe0_RXP_AMC	47	SGMII2_RXP_AMC	14
CSISC2_3_RXN1	Diff In	AK23	PCIe1/SGMII3_RXN_SOC	Sw Out	PCIe1_RXN_AMC or SGMII3_RXN_AMC	-	PCIe1_RXN_AMC	63	SGMII3_RXN_AMC	24
CSISC2_3_RXP1	Diff In	AK22	PCIe1/SGMII3_RXP_SOC	Sw Out	PCIe1_RXP_AMC or SGMII3_RXP_AMC	-	PCIe1_RXP_AMC	62	SGMII3_RXP_AMC	23
CSISC2_1_TXN0	Diff Out	AH20	PCIe0/SGMII2_TXN_SOC	Sw In	-	PCIe0_TXN_AMC or SGMII2_TXN_AMC	PCIe0_TXN_AMC	45	SGMII2_TXN_AMC	12
CSISC2_1_TXP0	Diff Out	AH21	PCIe0/SGMII2_TXP_SOC	Sw In	-	PCIe0_TXP_AMC or SGMII2_TXP_AMC	PCIe0_TXP_AMC	44	SGMII2_TXP_AMC	11
CSISC2_1_TXN1	Diff Out	AG21	PCIe1/SGMII3_TXN_SOC	Sw In	-	PCIe1_TXN_AMC or SGMII1_TXN_AMC	PCIe1_TXN_AMC	60	SGMII3_TXN_AMC	21
CSISC2_1_TXP1	Diff Out	AG22	PCIe1/SGMII3_TXP_SOC	Sw In	-	PCIe1_TXP_AMC or SGMII3_TXP_AMC	PCIe1_TXP_AMC	59	SGMII3_TXP_AMC	20

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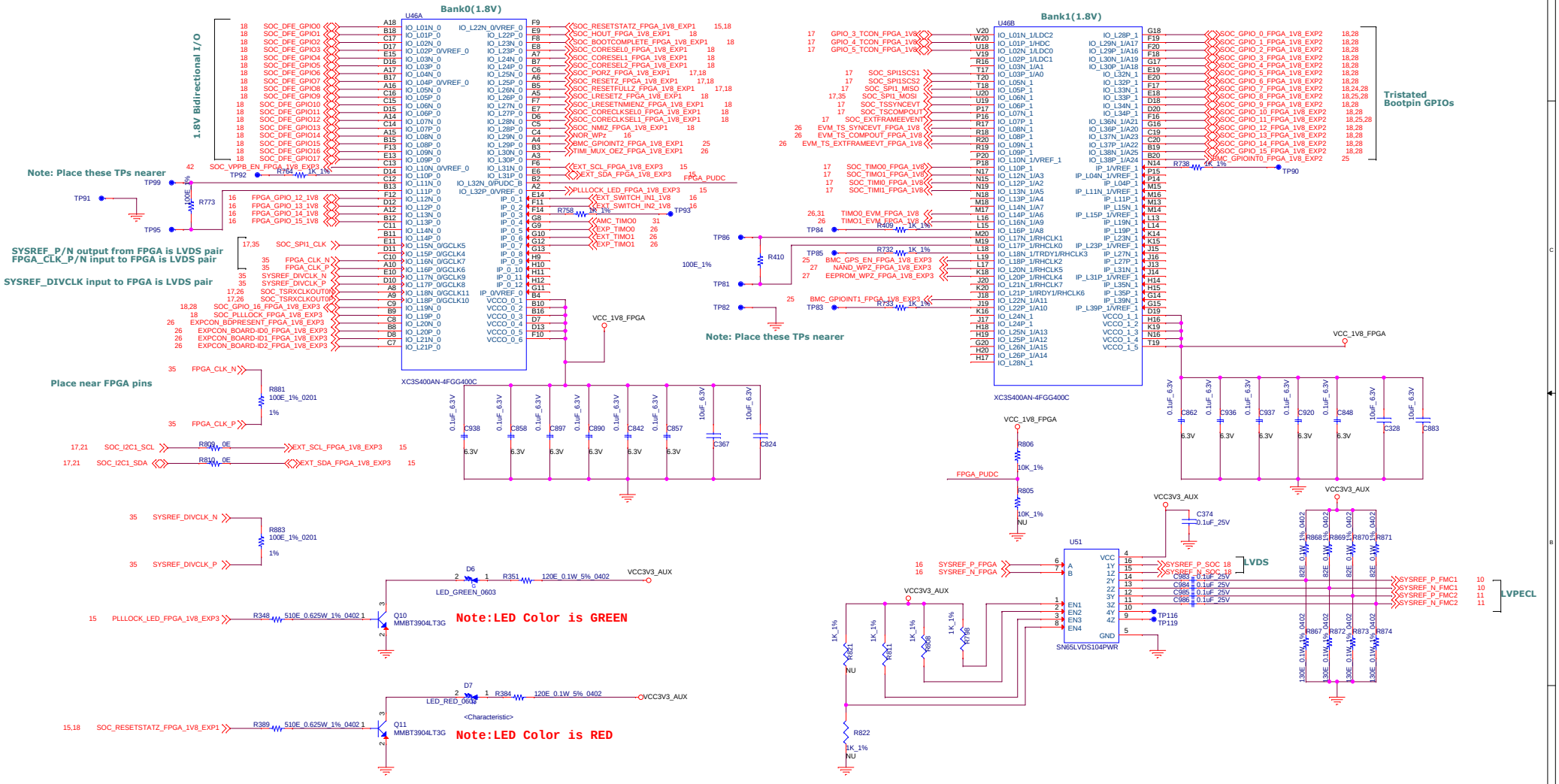
FPGA, SYSREF Buffering, LEDs



Project: K2L EVM		Designed for TI by eInfochips
Title: FPGA, SYSREF Buffering, LEDs		
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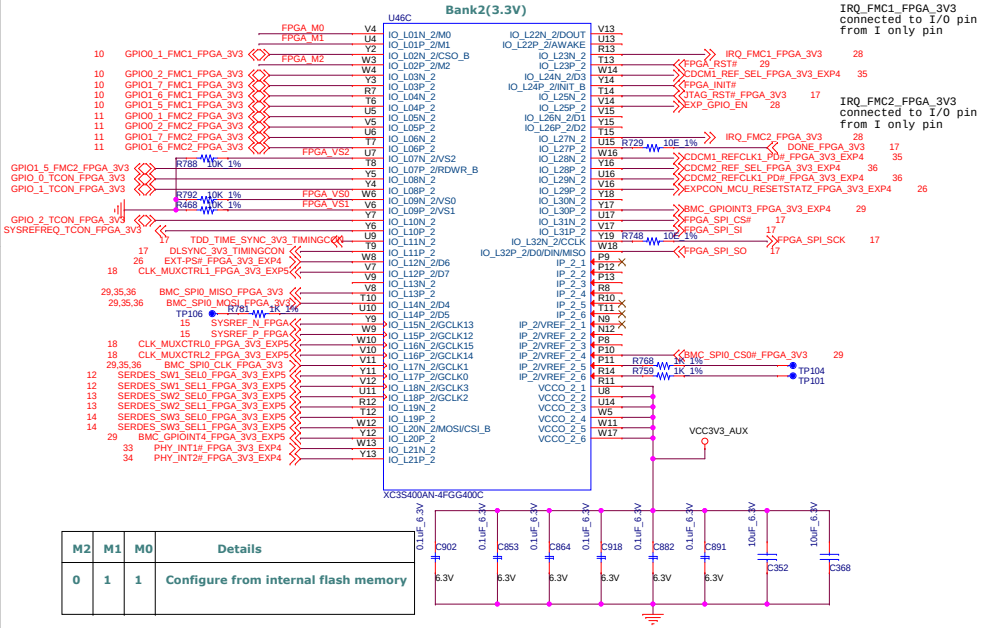
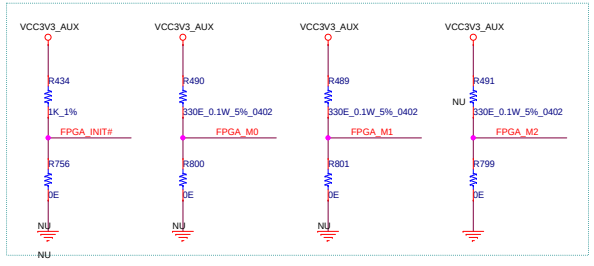
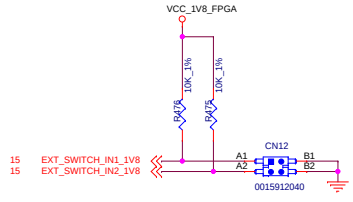
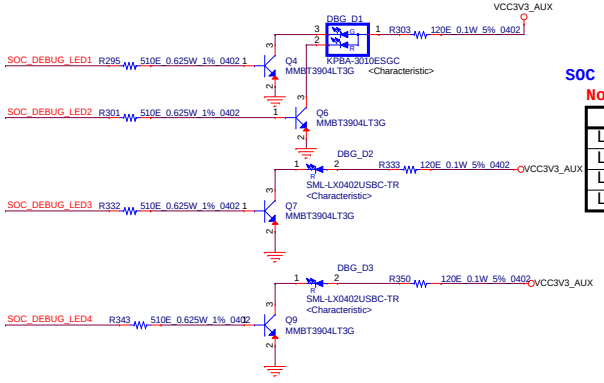
FPGA, FPGA 2pin conn, SPI Flash, LEDs



M2	M1	M0	Details
0	1	1	Configure from internal flash memory



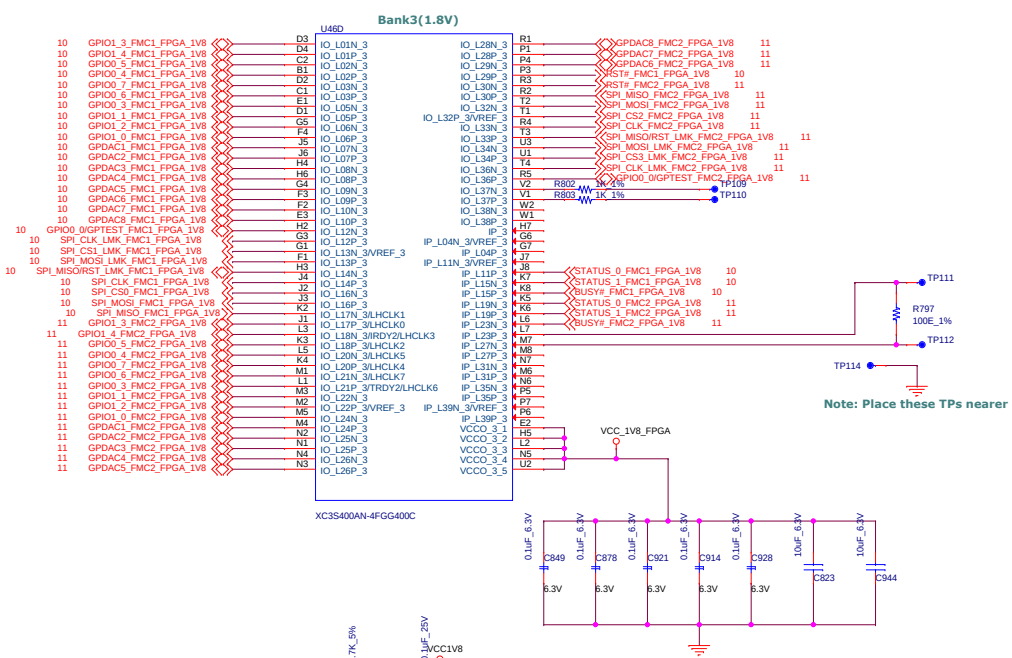


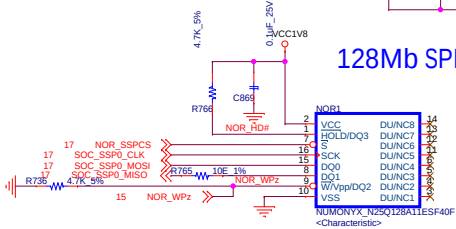


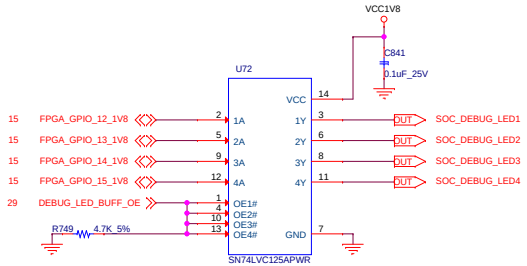
SOC Debug LEDs

Note:

	COLOR
LED1	RED
LED2	GREEN
LED3	BLUE
LED4	BLUE







Project: K2L EVM		Designed for TI by eInfochips
Title: FPGA, FPGA 2pin conn, SPI Flash, LEDs		
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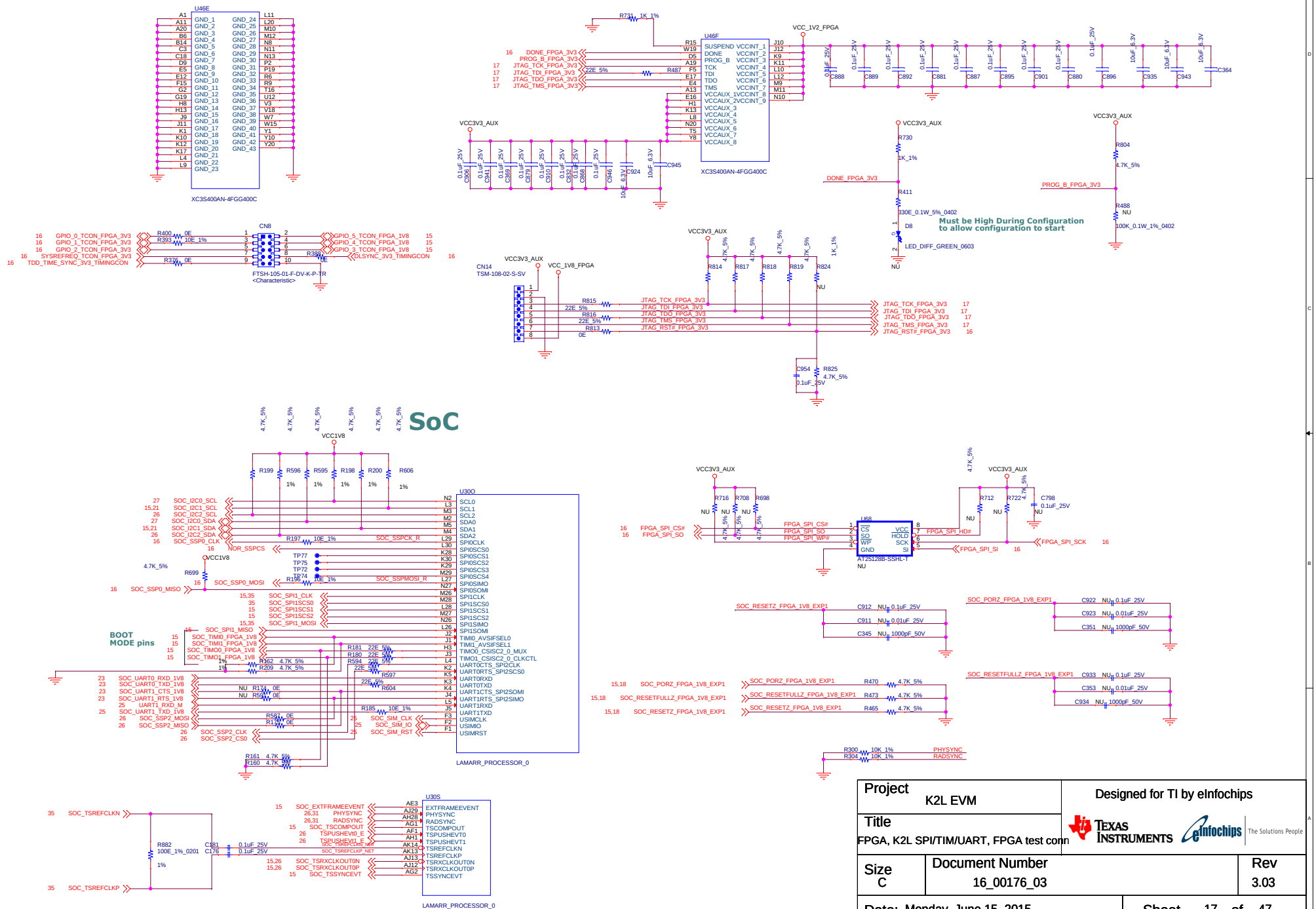
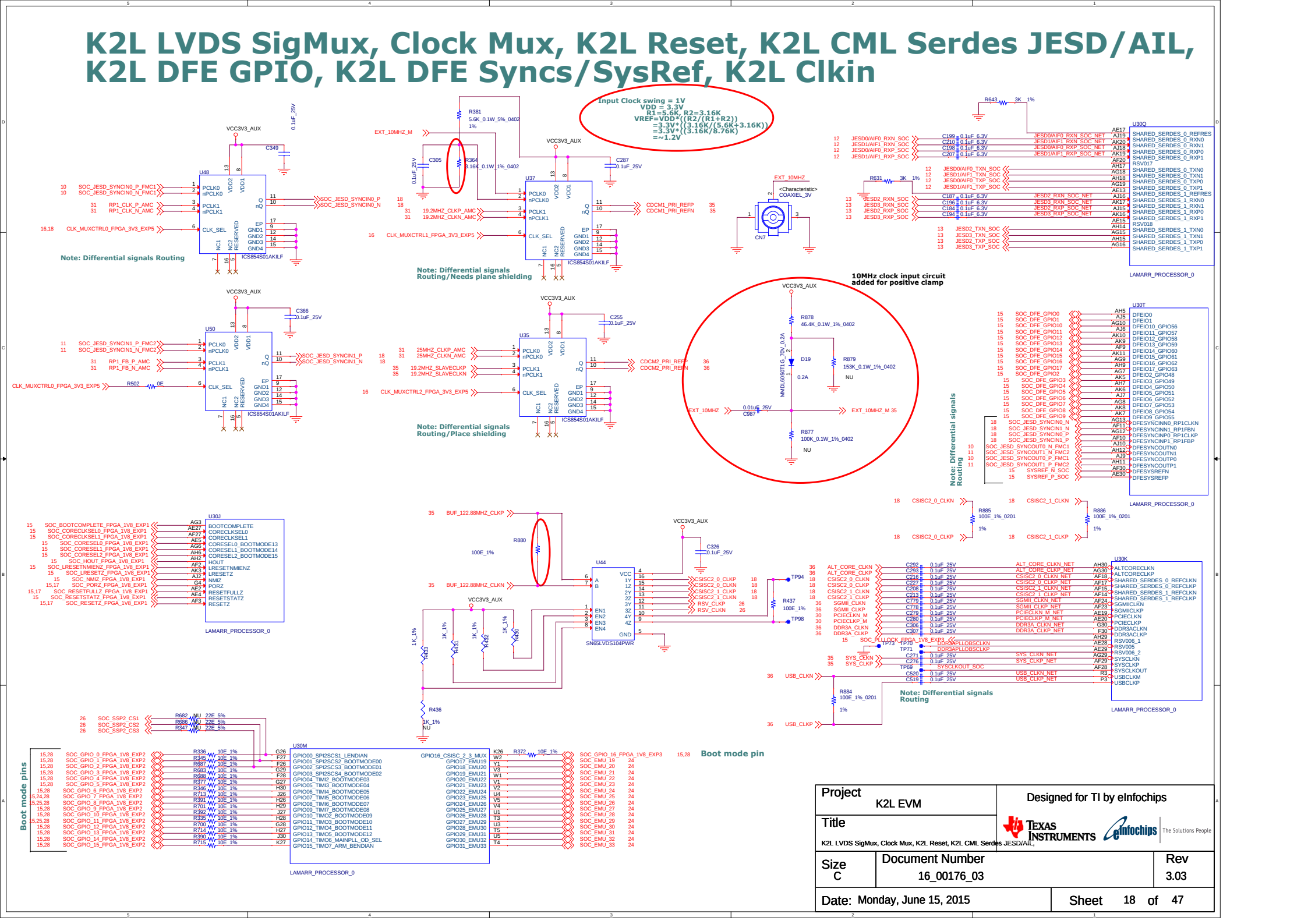
FPGA, FPGA JTAG, FPGA-Flash, FPGA Programmer, K2L SPI/TIM/UART, FPGA test conn



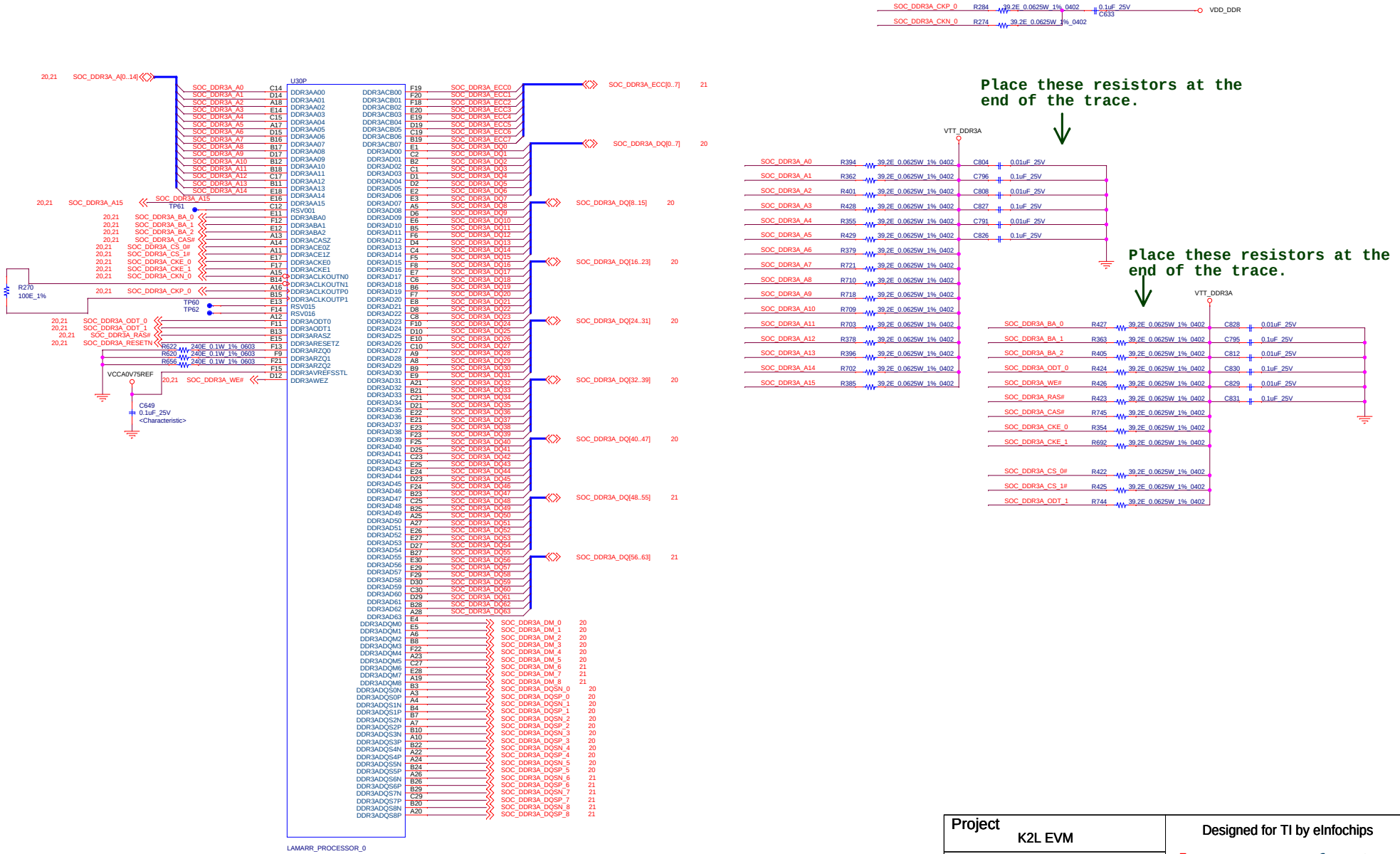
Project: K2L EVM		Designed for TI by eInfochips
Title: FPGA, K2L SPI/TIM/UART, FPGA test conn		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 17 of 47	

K2L LVDS SigMux, Clock Mux, K2L Reset, K2L CML Serdes JESD/AIL, K2L DFE GPIO, K2L DFE Syncs/SysRef, K2L Clkin



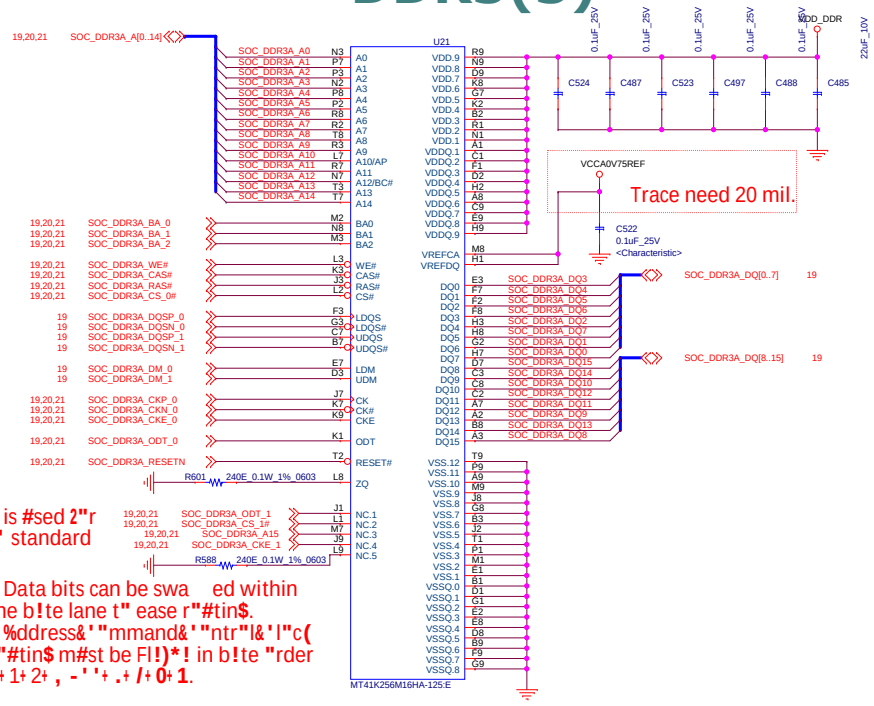
Project: K2L EVM	Designed for TI by eInfochips	
Title: K2L LVDS SigMux, Clock Mux, K2L Reset, K2L CML Serdes JESD/AIL,		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 18 of 47	

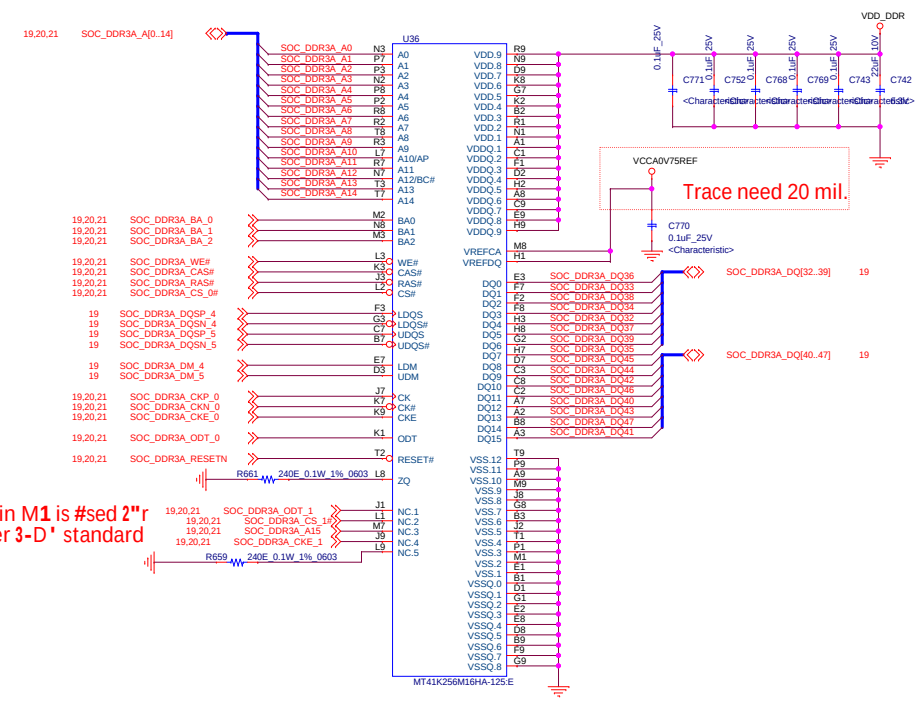
K2L DDR3

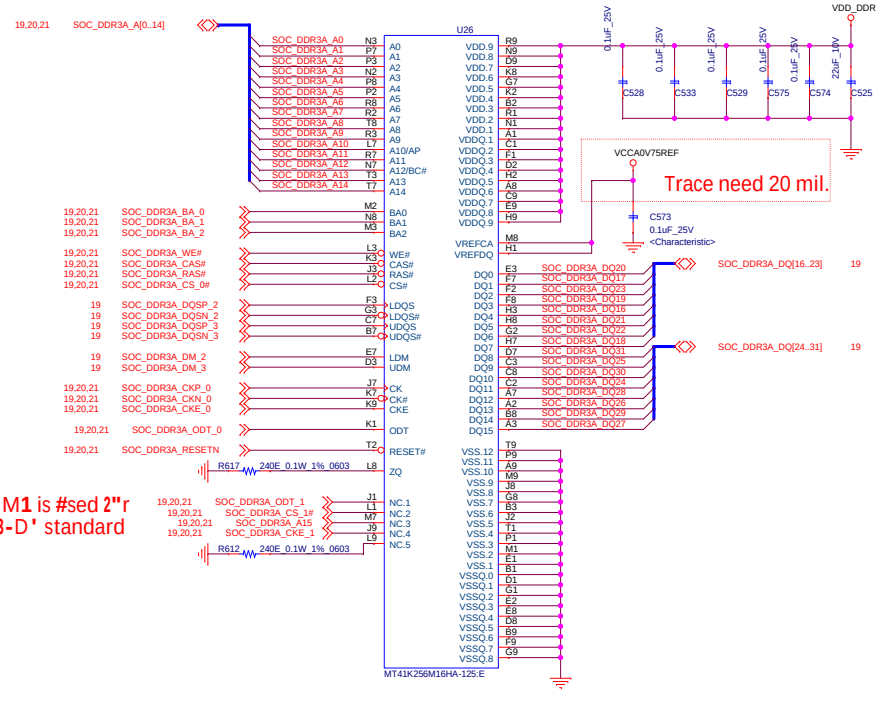


Project: K2L EVM	Designed for TI by eInfochips	
Title: K2L DDR3		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 19 of 47	

DDR3(3)

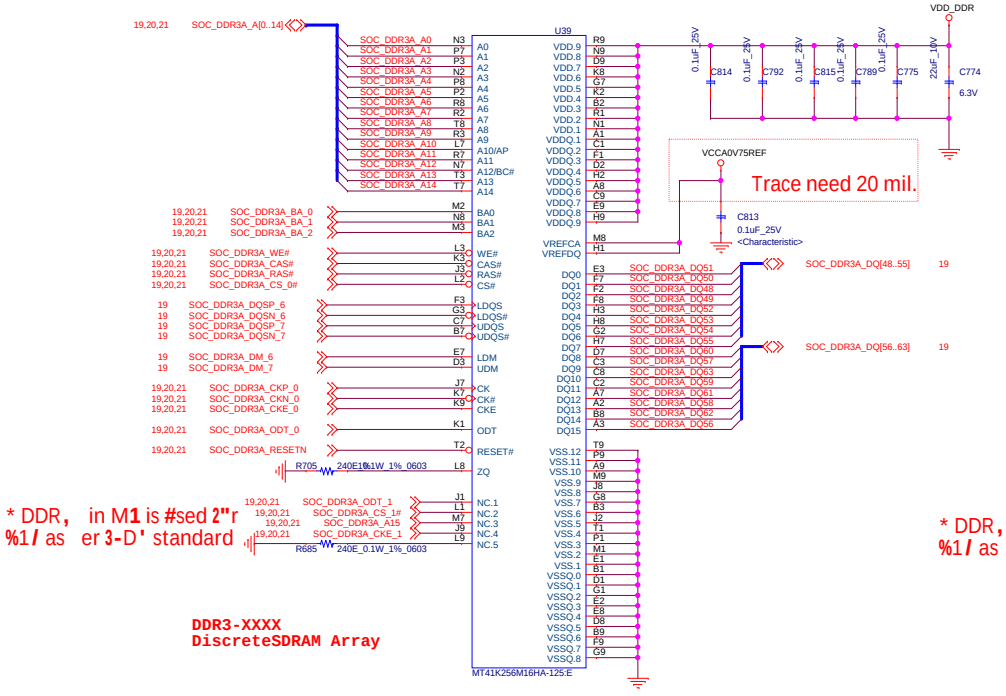




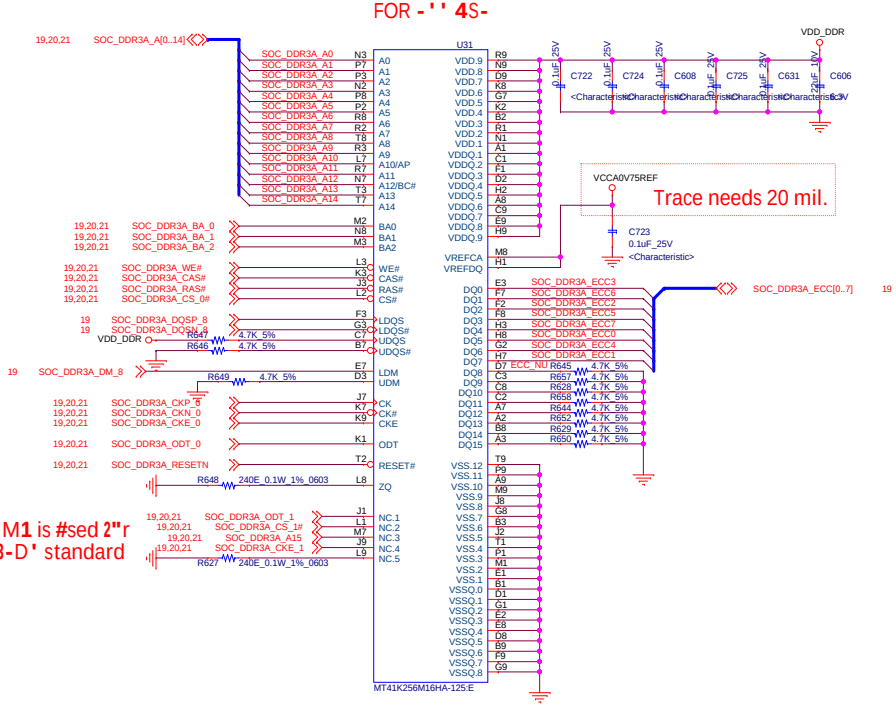


Project K2L EVM		Designed for TI by eInfochips
Title DDR3(3)		
Size C	Document Number 16_00176_03	Rev 3.03
Date: Monday, June 15, 2015		Sheet 20 of 47

DDR3(2), 3.3vaux -> .75v DDR3 Vt, DDR3 SPD EEPROM

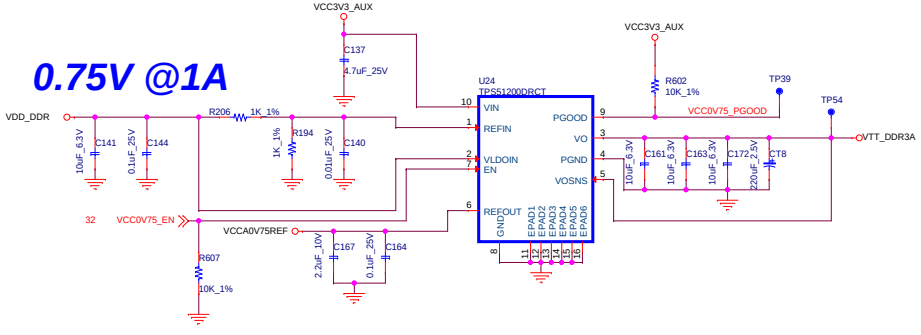


* DDR, in M1 is #sed 2"r
%1/ as er 3-D' standard

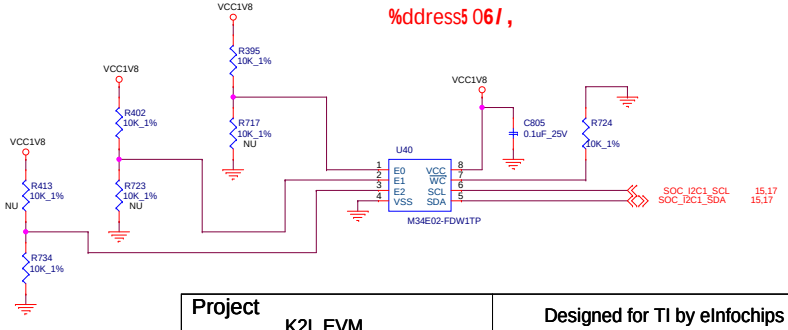


* DDR, in M1 is #sed 2"r
%1/ as er 3-D' standard

VCC0V75

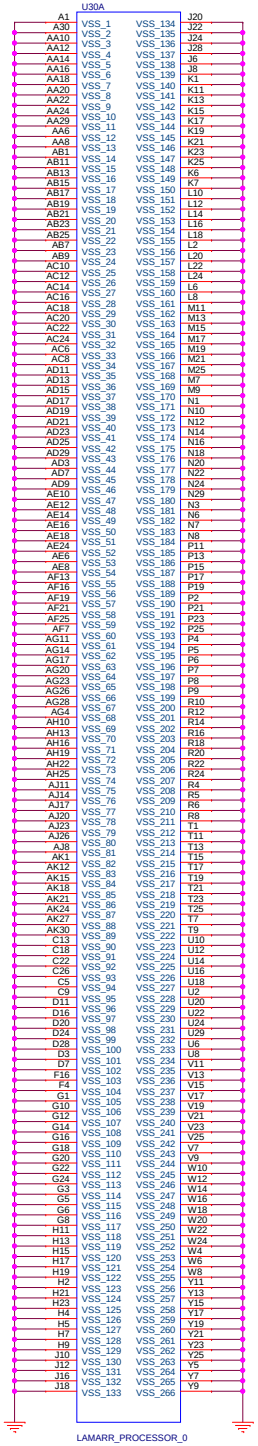


SPD EEPROM

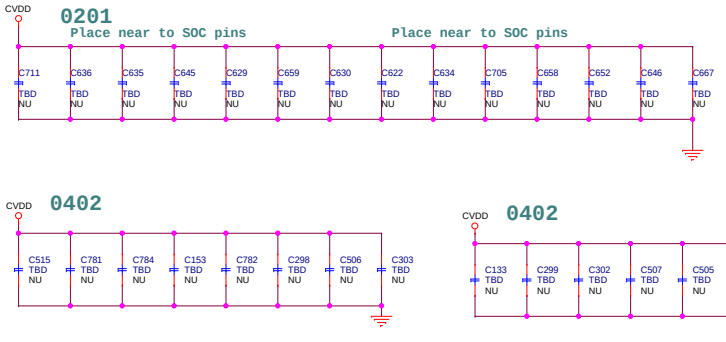


Project: K2L EVM		Designed for TI by eInfochips
Title: DDR3(2), 3.3vaux -> .75v DDR3 Vt, DDR3 SPD EEPROM		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 21 of 47	

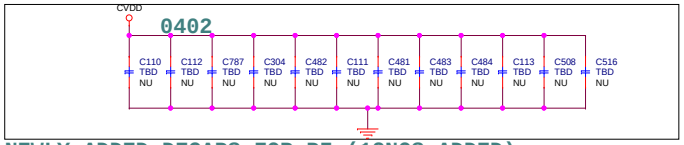
K2L GND AND POWER



THESE CAPS ARE ADDED FOR PROVISION ONLY. VALUES CAN BE CHANGED BASED ON PI ANALYSIS RESULT



THESE CAPS ARE ADDED TO SUPPORT PER PIN DECAP.
BASED ON PI ANALYSIS RESULT, IT WILL BE CHANGED (# OF CAPACITORS, VALUES, ETC)

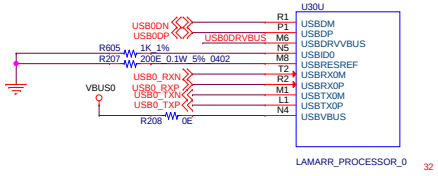


NEWLY ADDED DECAPS FOR PI (12NOS ADDED)

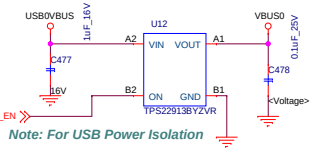
Project: K2L EVM		Designed for TI by eInfochips
Title: K2L GND AND POWER		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 22 of 47	

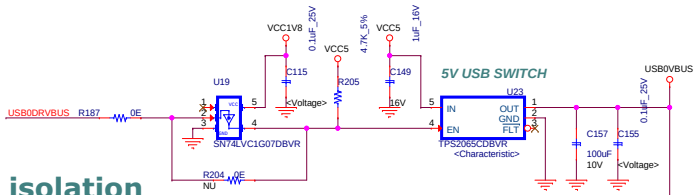
K2L USB3, TPS USB 5v isolation, USB Type A connector, magnetics, filter, SOC UART 1.8/3.3v, USB to dual UART

K2L USB3

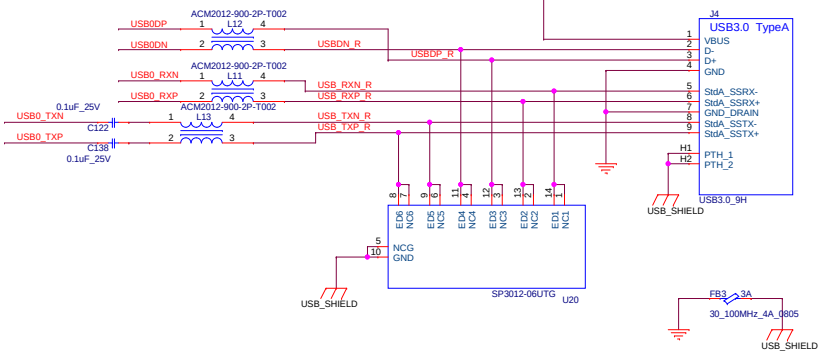


TPS USB 5v isolation

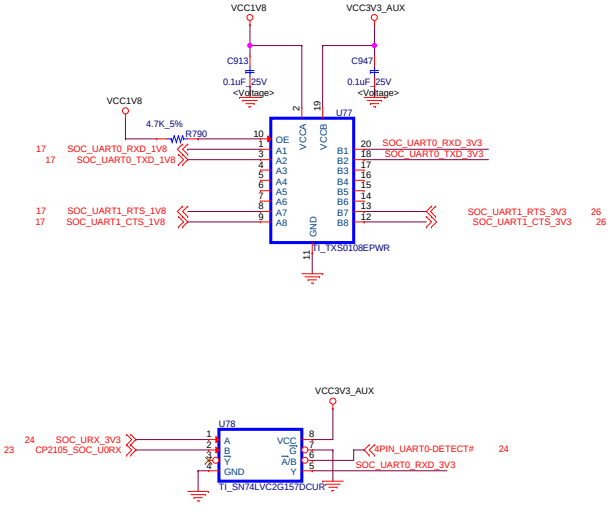




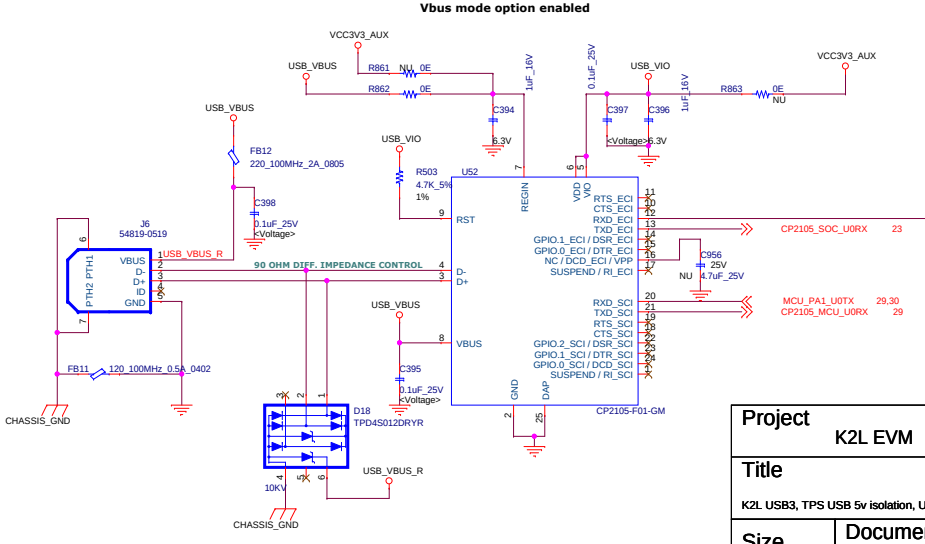
USB Type A connector



SOC UART 1.8/3.3v

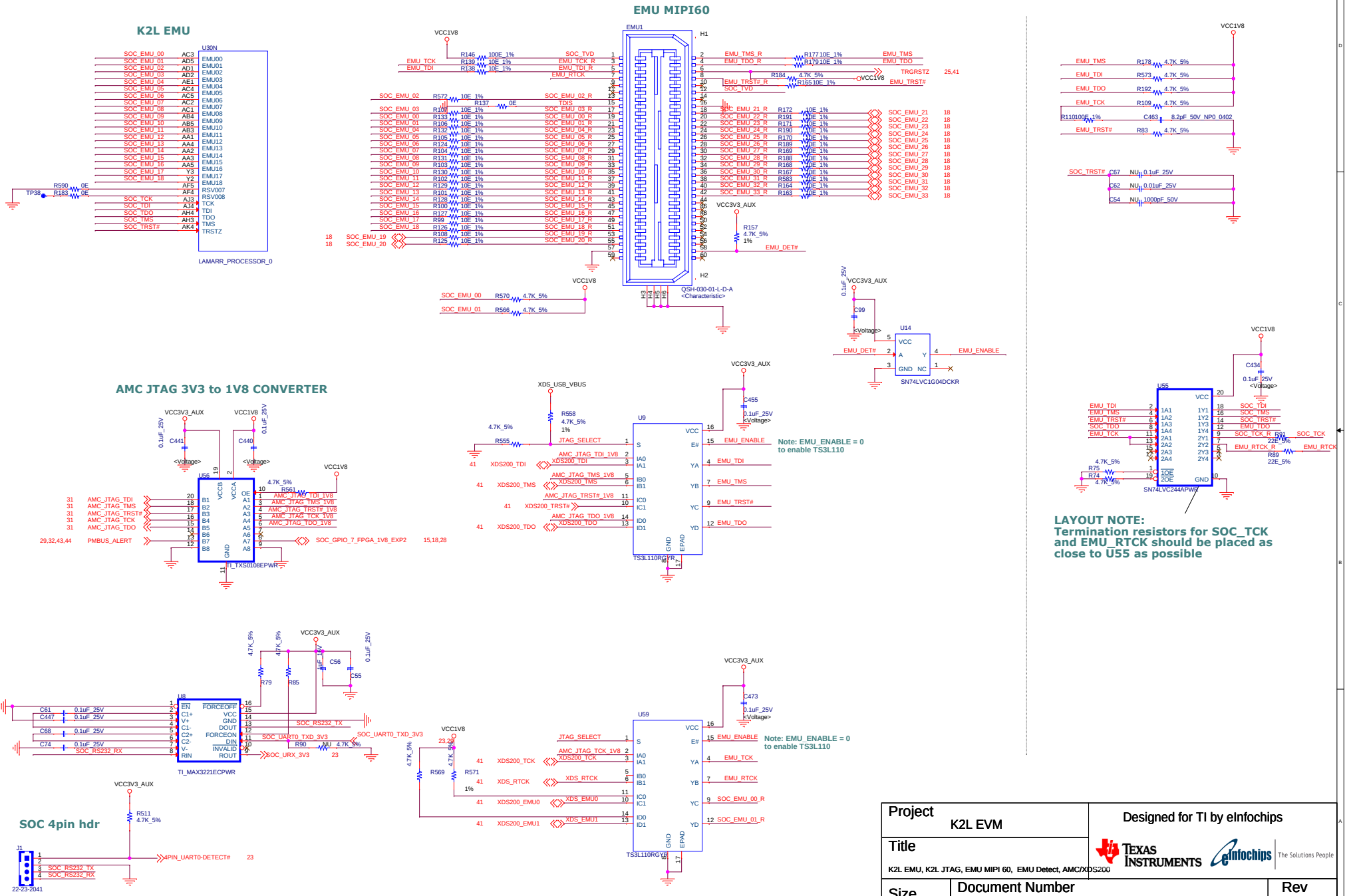


USB to dual UART



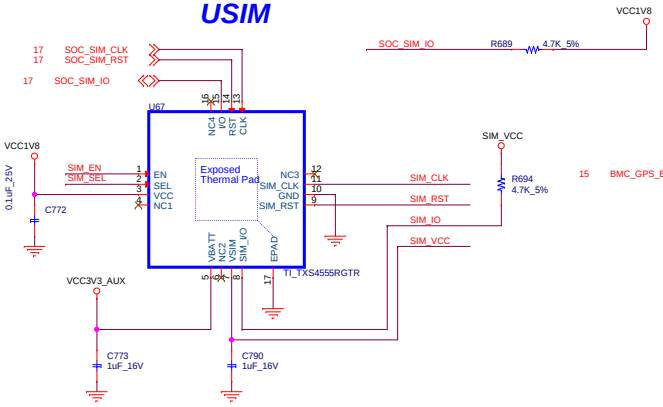
Project: K2L EVM		Designed for TI by eInfochips
Title: K2L USB3, TPS USB 5v isolation, USB Type A connector, magnetics, filter, SOC UART 1.8/3.3v, USB to dual UART		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 23 of 47	

K2L EMU, K2L JTAG, EMU MIPI 60, EMU Detect, AMC/XDS200 JTAG sw, AMC JTAG 3.3 to 1.8v, SOC miniUSB, SOC 4pin hdr

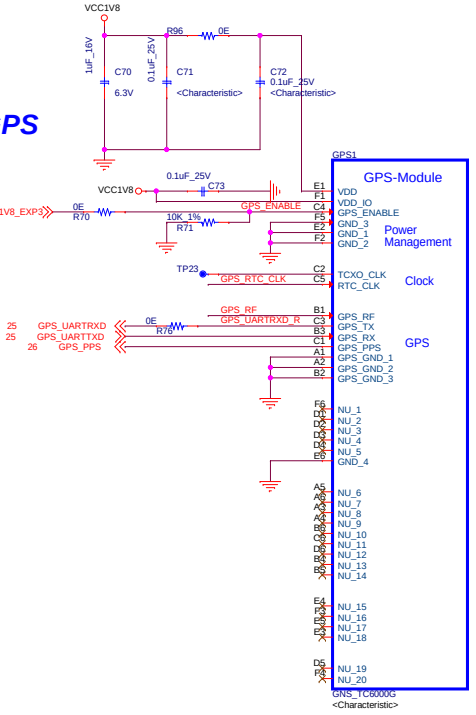


USIM, SOC UART 1.8v switching, 1.8v/3.3v GPIO INT, SOC UART, GPS

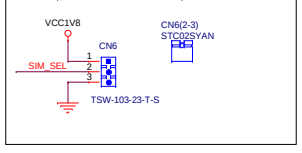
USIM

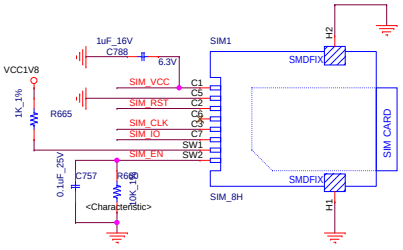


GPS

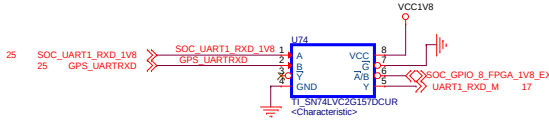


	High	Low (Default)
SIM_SEL	VCC_SIM Value = 2.95V	VCC_SIM Value = 1.8V

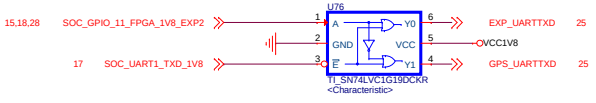




SOC UART 1.8v switching

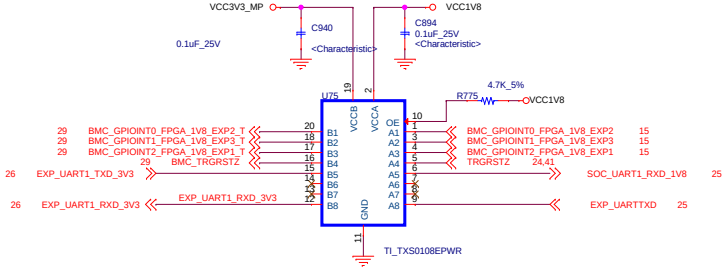


Note:GPIO8
0, SOC_UART0_Rxd -> UART1_Rxd
1, GPS_UARTRxd -> UART1_Rxd

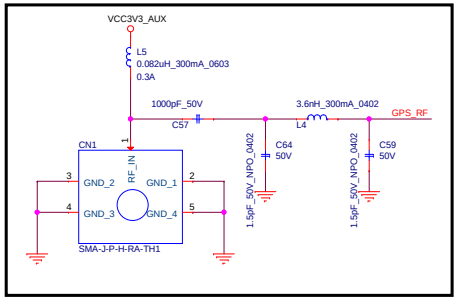


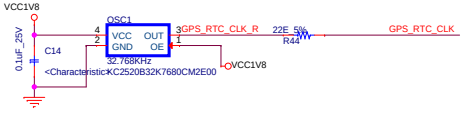
Note:GPIO11
0, SOC_UART1 -> EXP_UARTTX0
1, GPS_UART1 -> GPS_UARTTX0

SPI level shift 3.3V <=> 1.8V



FOR ANTENNA CIRCUIT

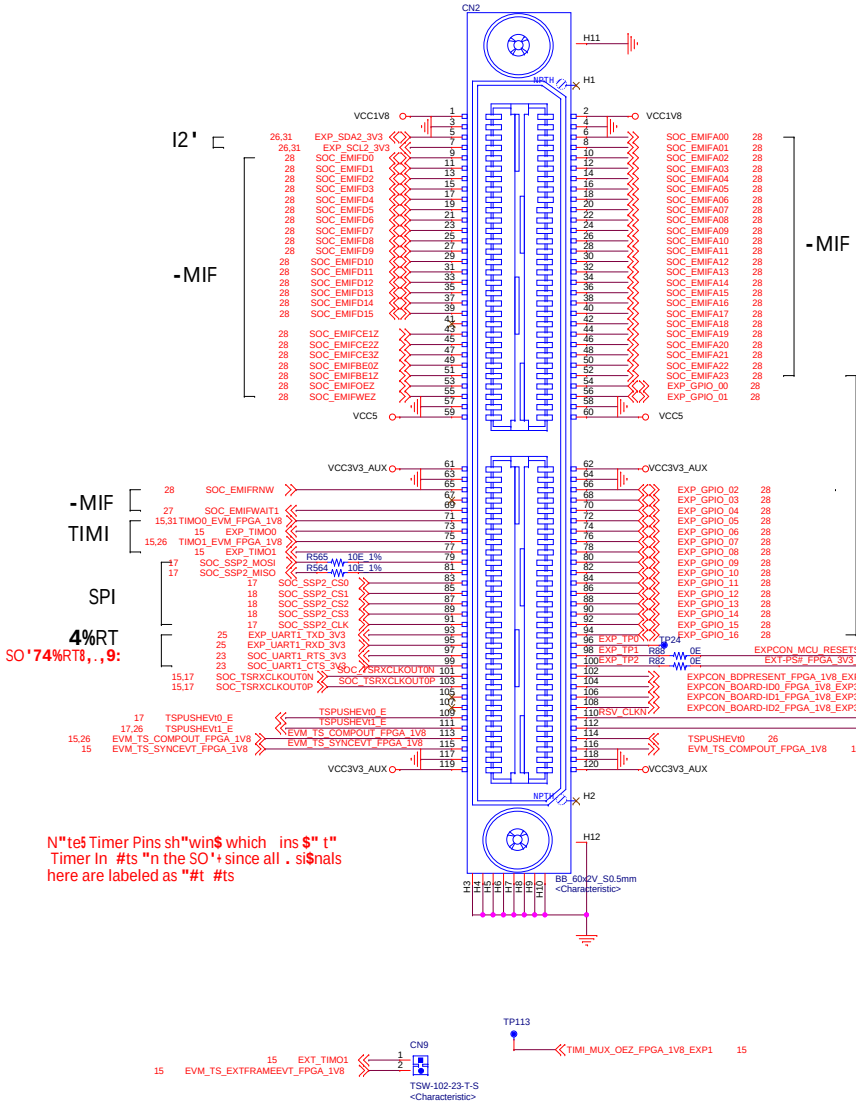




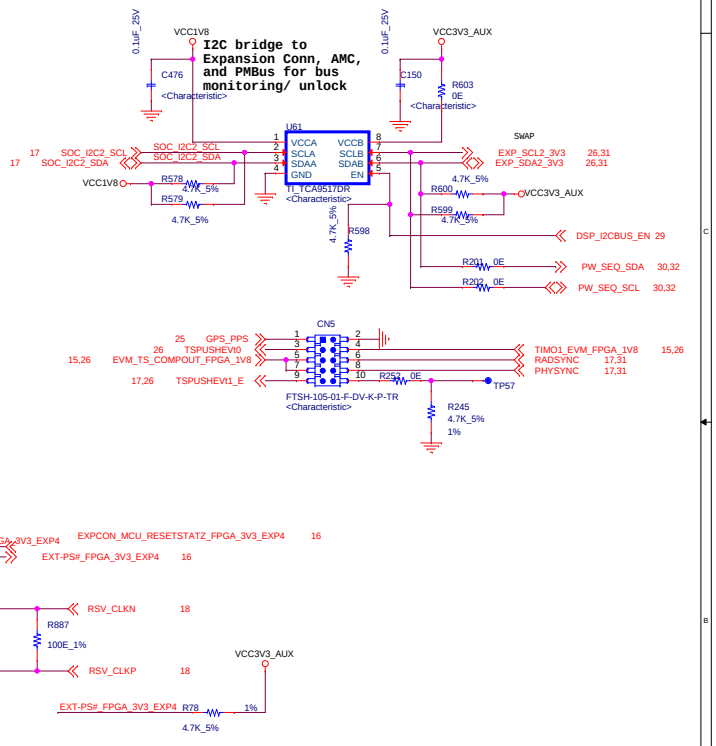
Project: K2L EVM		Designed for TI by eInfochips
Title: USIM, SOC UART 1.8v switching, 1.8v/3.3v GPIO INT, SOC UART, GPS		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 25 of 47	

Expansion Connector, I2C SOC to Expander 1.8v/3.3vAux

Expansion Connector



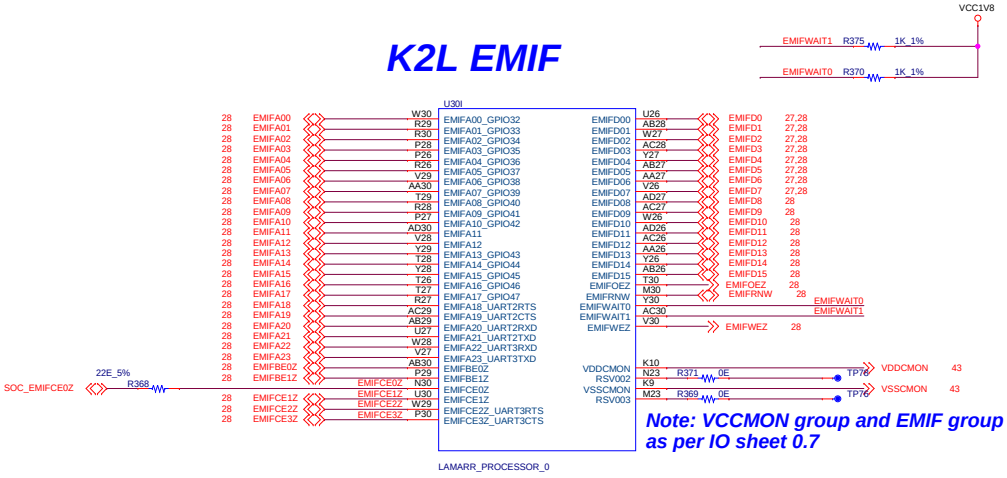
I2C SOC to Expander 1.8v/3.3vAux



Project: K2L EVM	Designed for TI by eInfochips	
Title: Expansion Connector, I2C SOC to Expander 1.8v/3.3vAux		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 26 of 47	

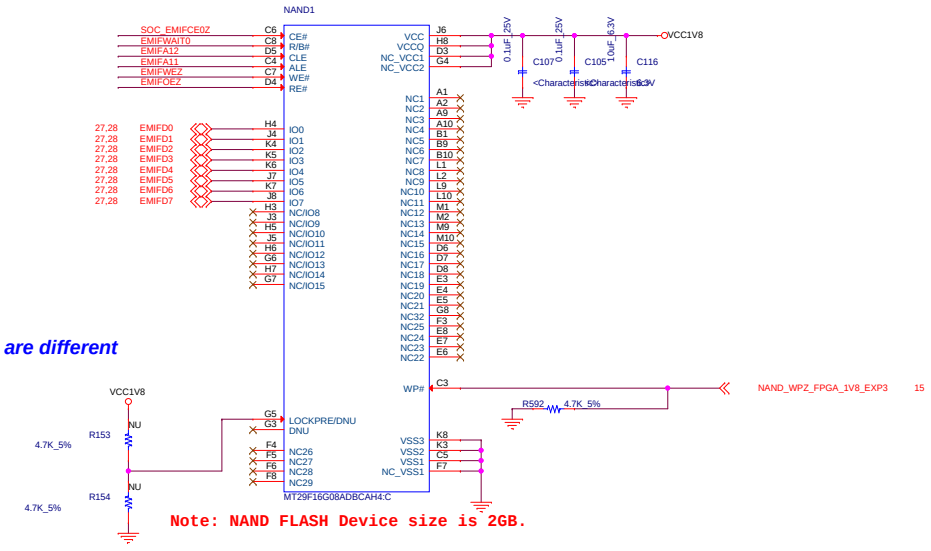
K2L EMIF, VDD and VSSMON, EMIFWAIT1 bfr, NAND Flash, I2C EEPROM

K2L EMIF



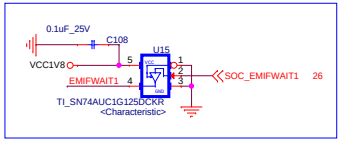
Note: VCCMON group and EMIF group are different as per IO sheet 0.7

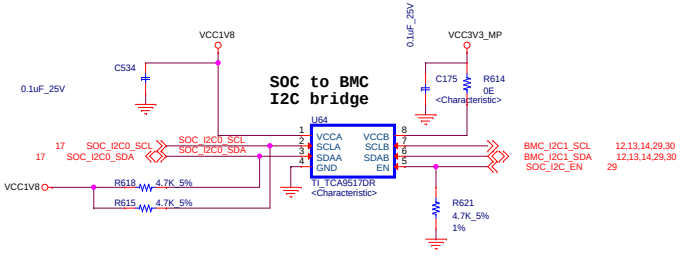
NAND FLASH

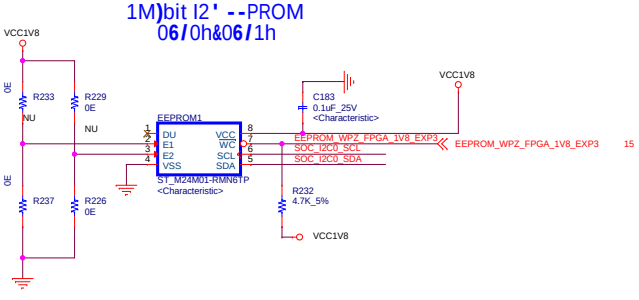


Note: NAND FLASH Device size is 2GB.

EMIFWAIT1 bfr

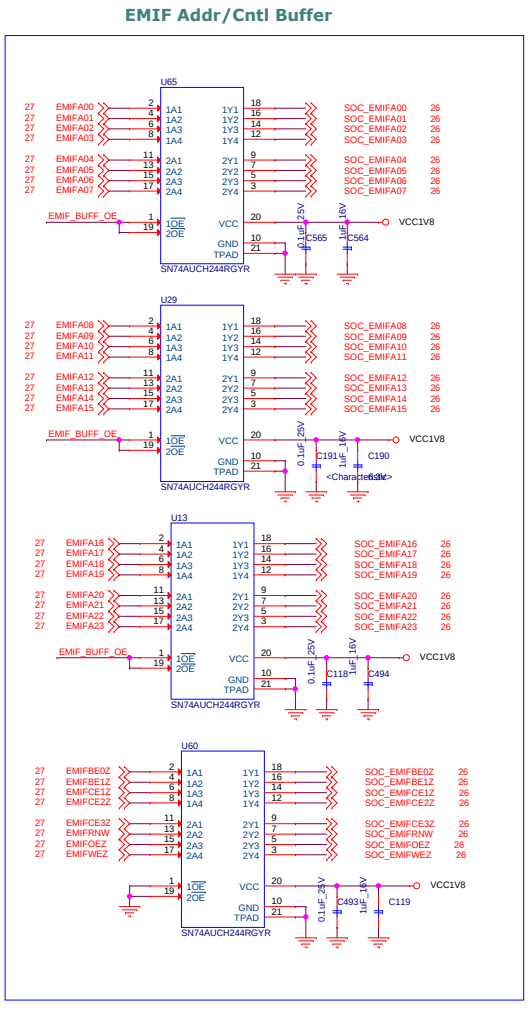


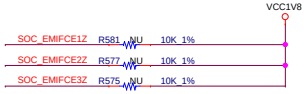


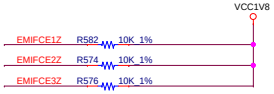


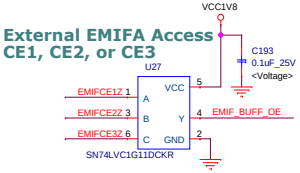
Project: K2L EVM	Designed for TI by eInfochips	
Title: K2L EMIF, VDD and VSSMON, EMIFWAIT1 bfr, NAND Flash, I2C EEPROM		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 27 of 47	

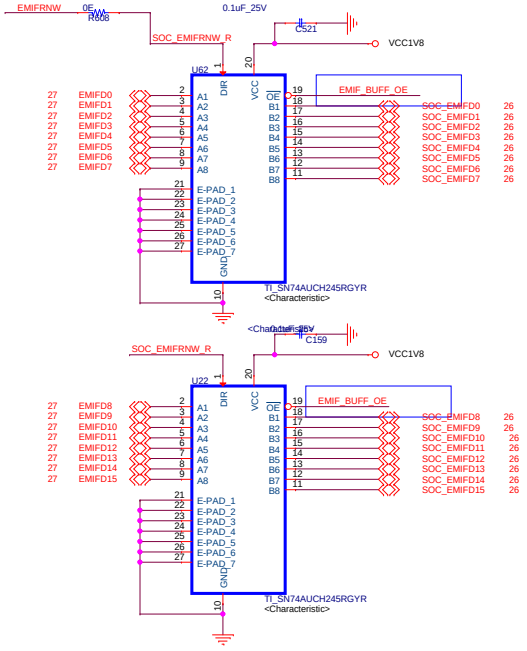
EMIF Addr/Cntl Buffer, Ext EMIF_OE, EMIF Data Transceiver

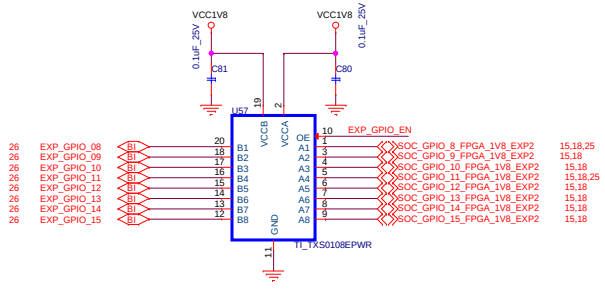


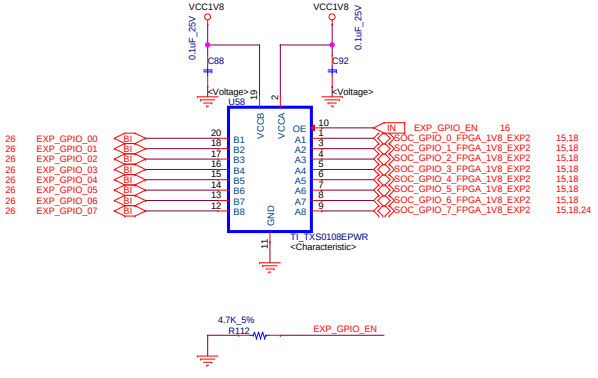


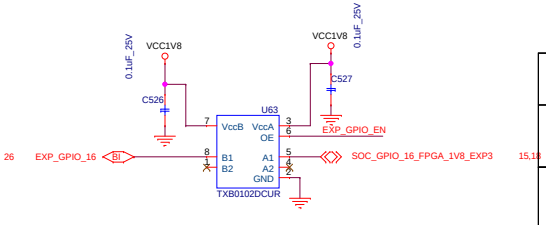






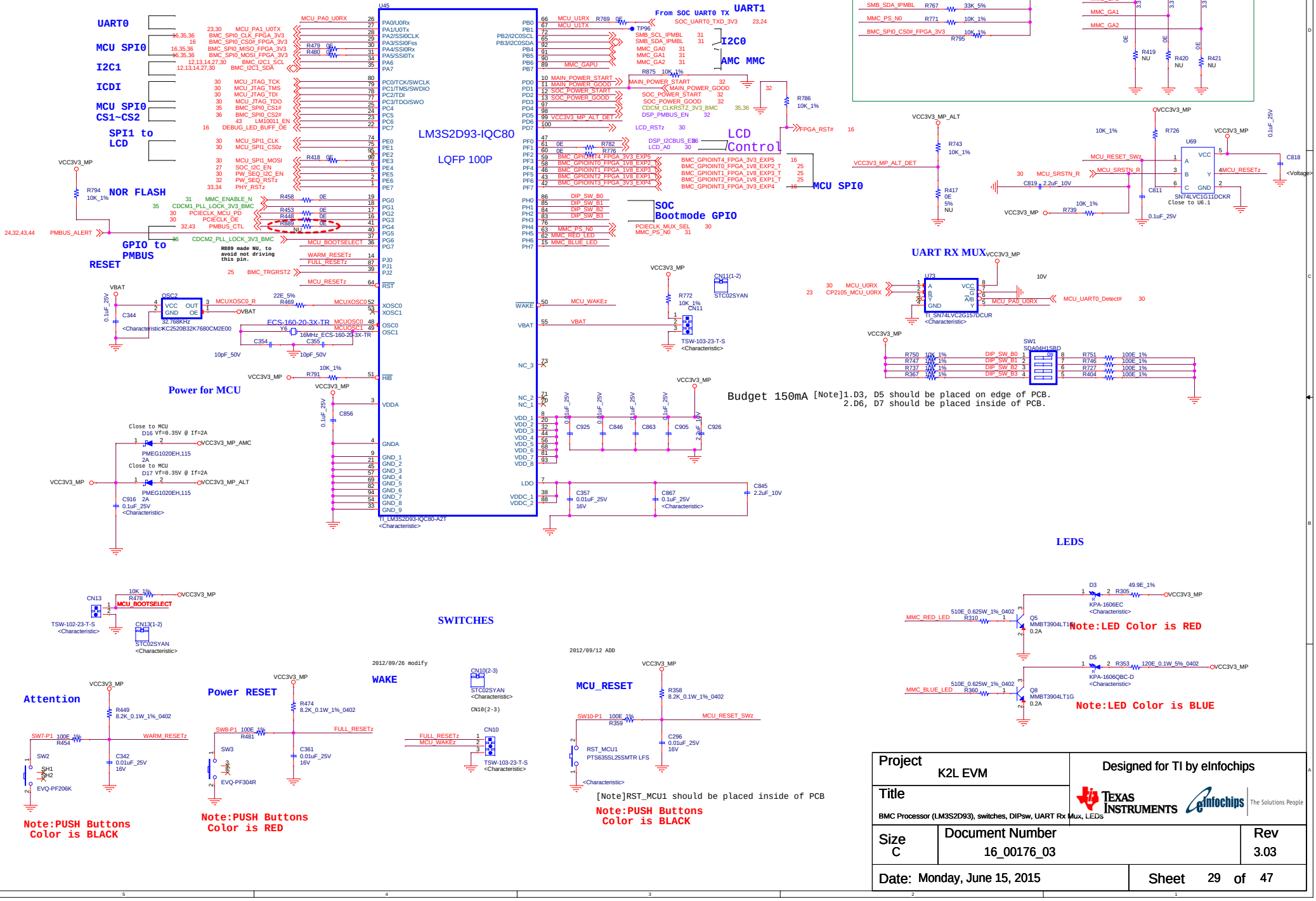






Project: K2L EVM	Designed for TI by eInfochips	
Title: EMIF Addr/Cntl Buffer, Ext EMIF_OE, EMIF Data Transceiver		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 28 of 47	

BMC Processor (LM3S2D93), switches, DIPsw, UART Rx Mux, LEDs



Project: K2L EVM		Designed for TI by eInfochips
Title: BMC Processor (LM3S2D93), switches, DIPsw, UART Rx Mux, LEDs		
Size: C	Document Number: 16_00176_03	Rev: 3.03
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LCD, LCD Power, BMC USB for UART, 4pin UART for BMC, BMC JTAG, BMC to PMBus isolator, PCIe clock

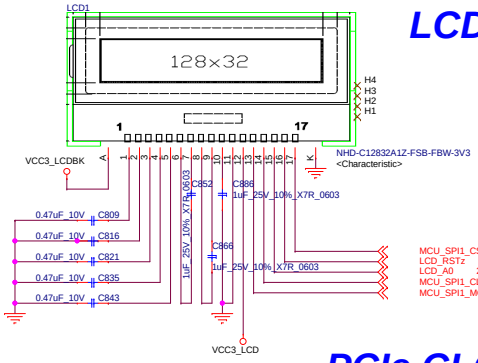
LCD Power

VO = 1.24v(1+R1/R2)+0.15uA*R1

3.018V =1.24 (1+10k/6.98k)+0.15u*10k

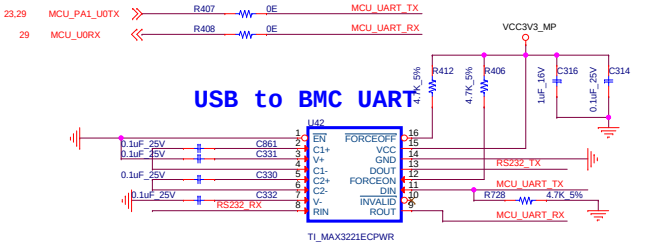
LCD

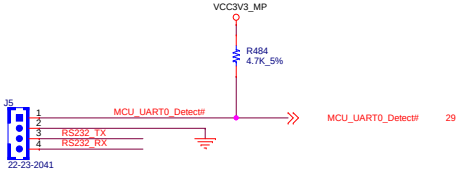
NHD-C12832A1Z-FSB-FBW-3V3



SPI1 CS0
LCD control

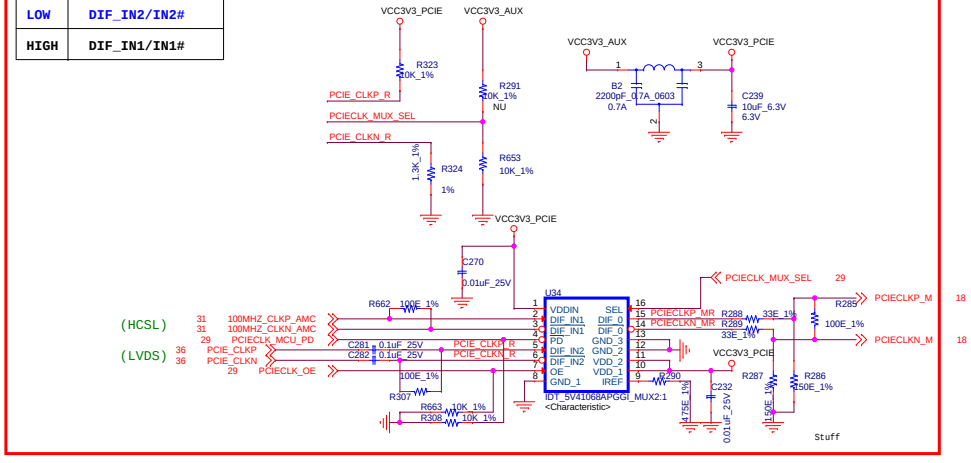
MCU UART



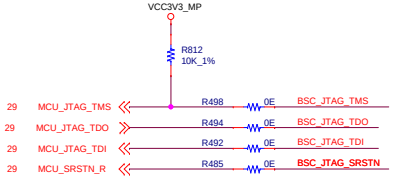


PCIe CLOCK MUX

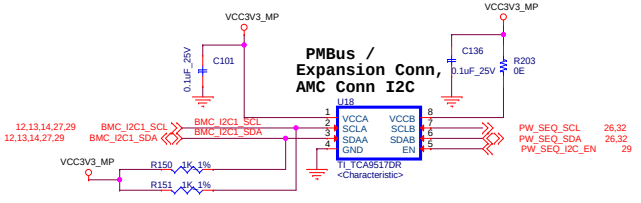
SEL	I/P PAIR SEL
LOW	DIF_IN2/IN2#
HIGH	DIF_IN1/IN1#

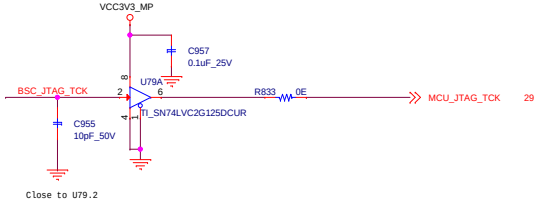


MCU JTAG



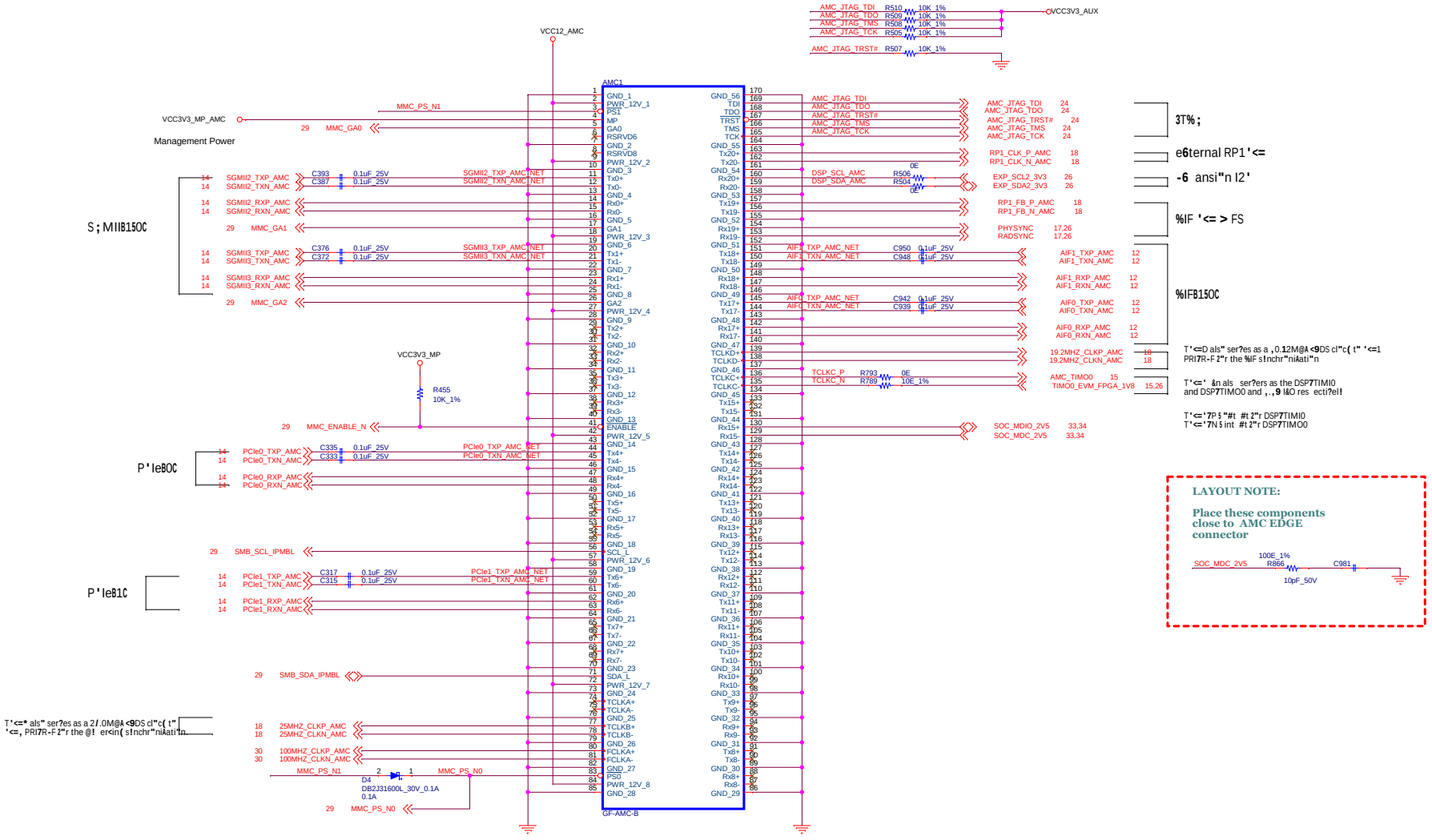
10 pos (50 mil pitch) connector





Project: K2L EVM		Designed for TI by eInfochips
Title: LCD, LCD Power, BMC USB for UART, 4pin UART for BMC, BMC		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 30 of 47	

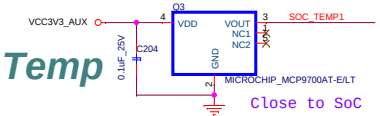
AMC connector



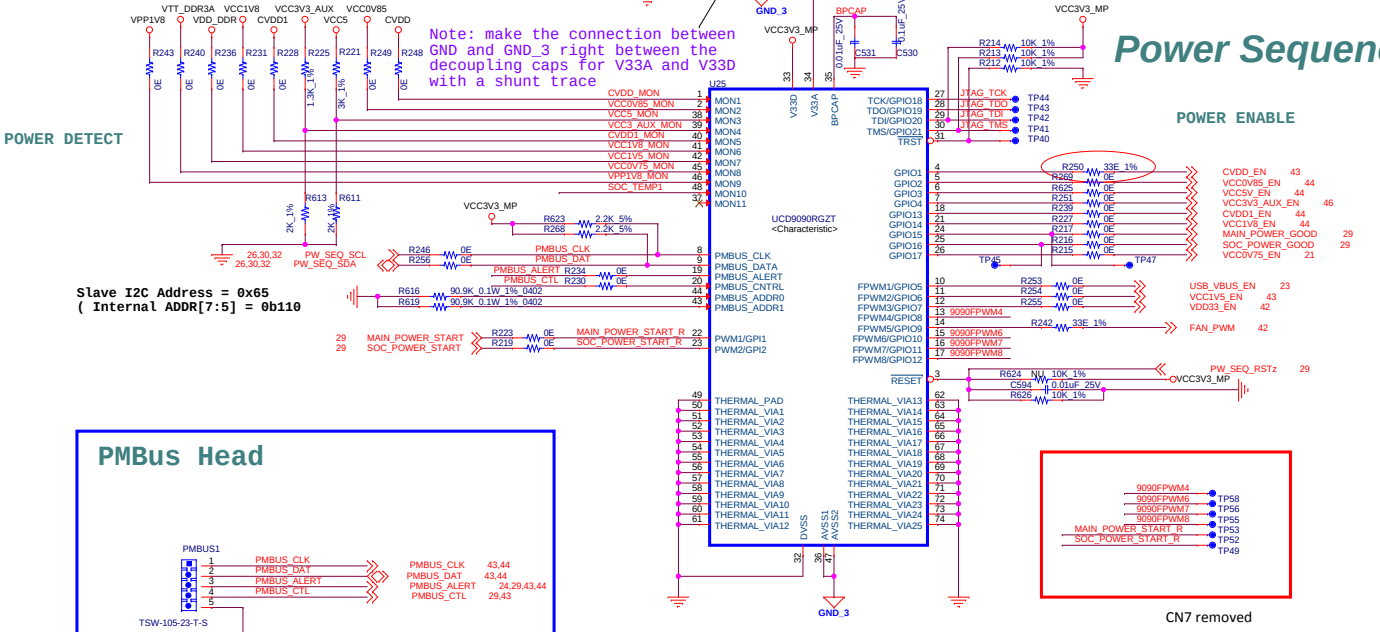
Project: K2L EVM		Designed for TI by eInfochips
Title: AMC connector		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015		Sheet 31 of 47

SOC Temp, UCD9090, PMBus Pgm conn, VID Isolator for PMBus

SOC Temp



Power Sequencing



PMBus Head

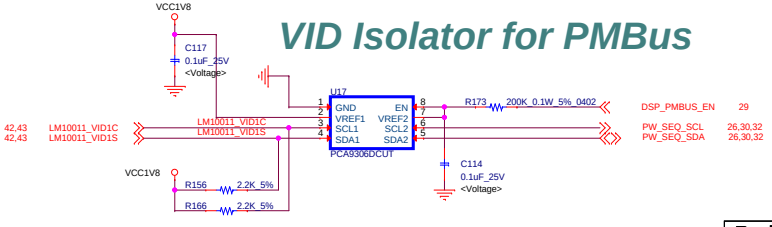
CN7 removed

Layout Note: The decoupling caps should be kept as close to the pins as possible with short traces (there is an AGND pin at the corner of the device by the power/ref pins) connecting back to the device, preferably without using vias for best performance.

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
SHORT	--

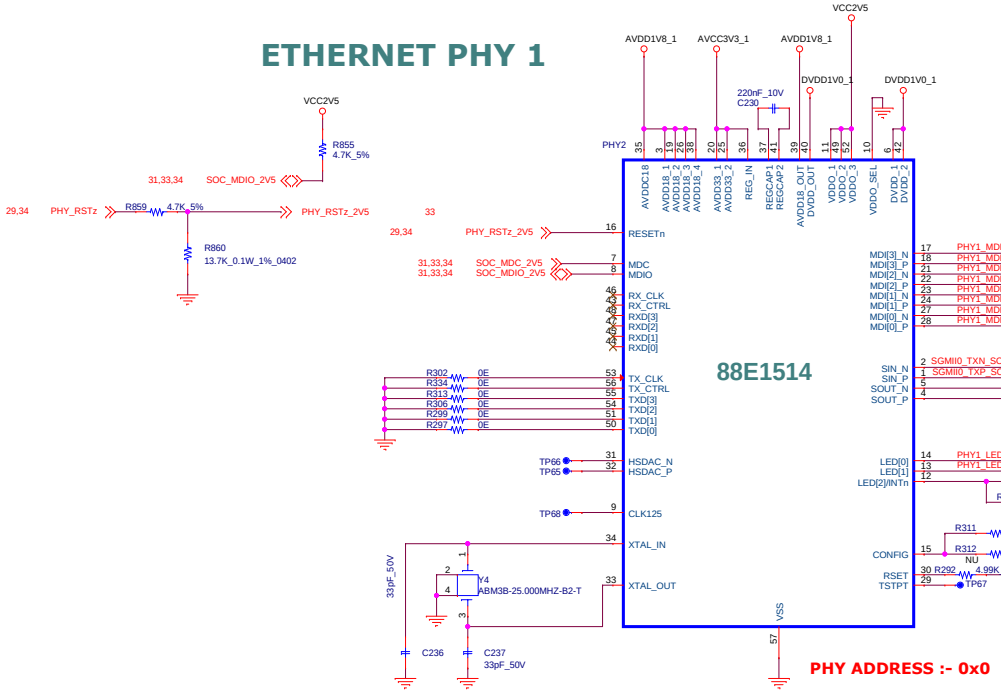
VID Isolator for PMBus



Project: K2L EVM		Designed for TI by eInfochips	
Title: SOC Temp, UCD9090, PMBus Pgm conn, VID Isolator for PMBus			
Size: C	Document Number: 16_00176_03		Rev: 3.03
Date: Monday, June 15, 2015		Sheet 32 of 47	

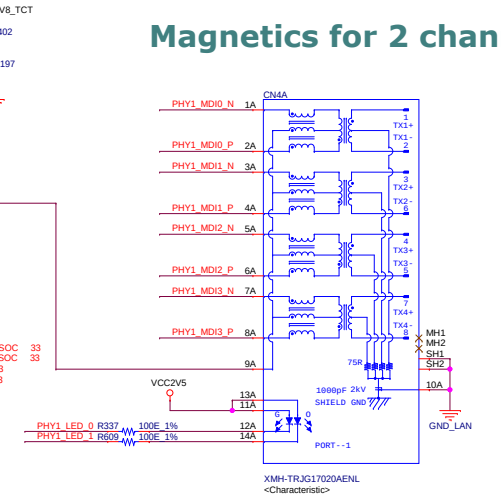
Ethernet PHY, Magnetics for 2 channel/ Tx/Rx, MDC/MDIO for AMC, K2L SGMII/ PCIe

ETHERNET PHY 1

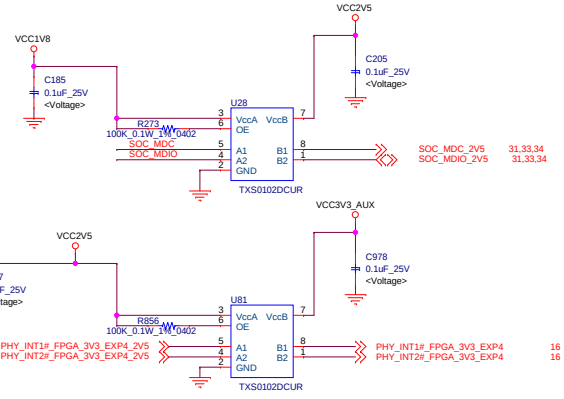


Pin	CONFIG Bit1	CONFIG Bit0	Value Assignment
Config	0	0	PHYAD[0]=0 VDDO_LEVEL=3.3V
Config	1	1	PHYAD[0]=1 VDDO_LEVEL=3.3V
Config	1	0	PHYAD[0]=0 VDDO_LEVEL=2.5V
Config	0	1	PHYAD[0]=1 VDDO_LEVEL=2.5V

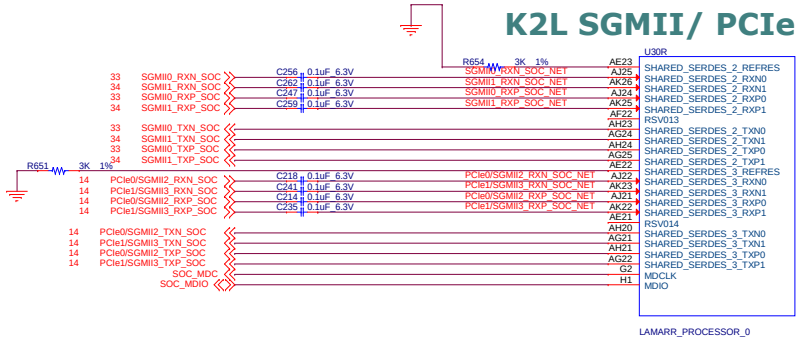
Magnetics for 2 channel/ Tx/Rx



MDC/MDIO for AMC



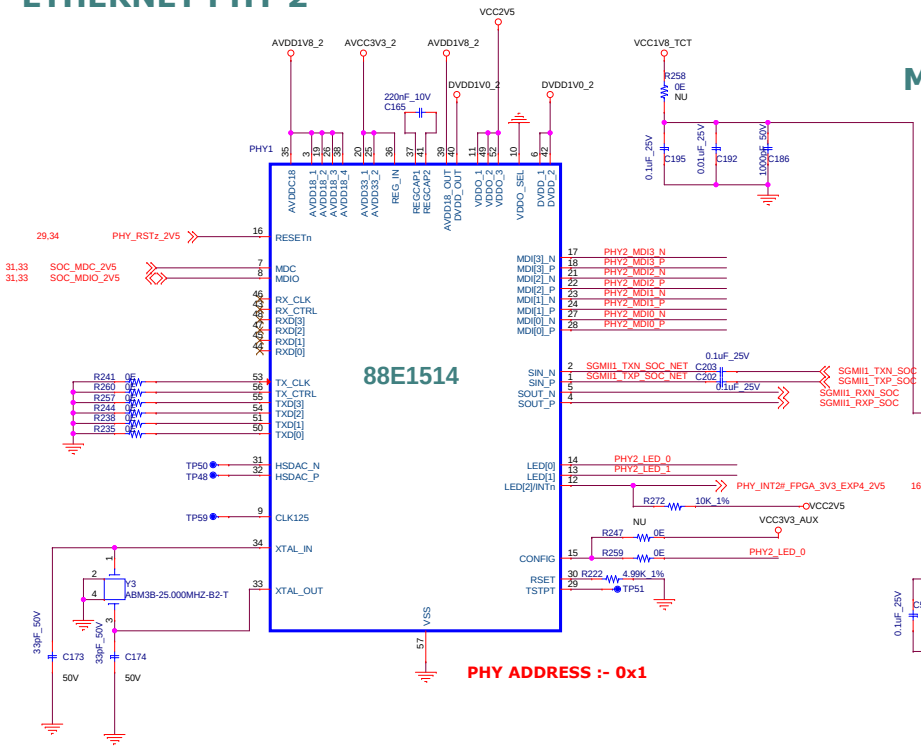
K2L SGMII/ PCIe



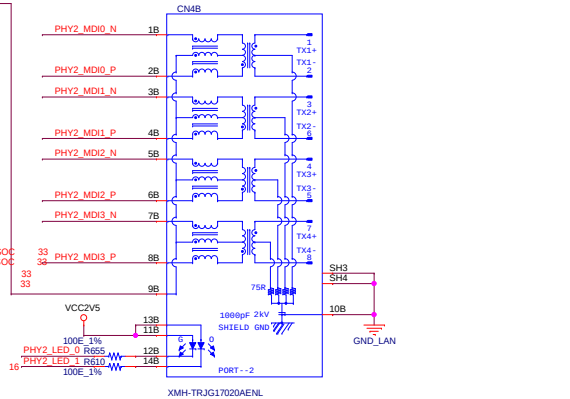
Project: K2L EVM		Designed for TI by eInfochips
Title: Ethernet PHY, Magnetics for 2 channel/ Tx/Rx,		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 33 of 47	

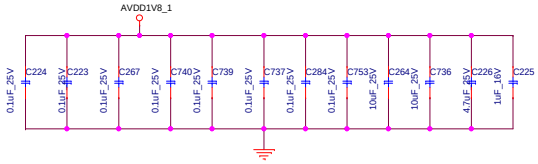
Ethernet PHY, Magnetics for 2 channel/ Tx/Rx

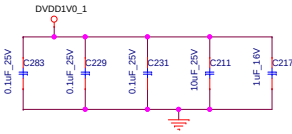
ETHERNET PHY 2

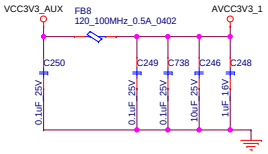


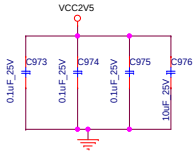
Magnetics for 2 channel/ Tx/Rx

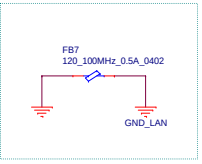


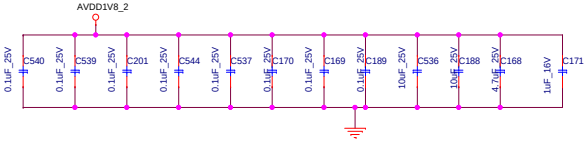


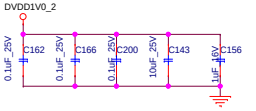


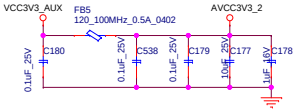


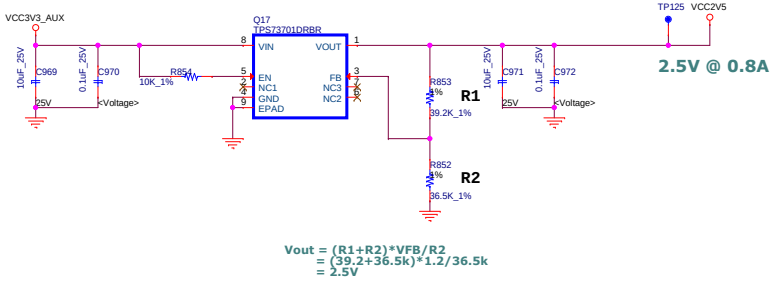






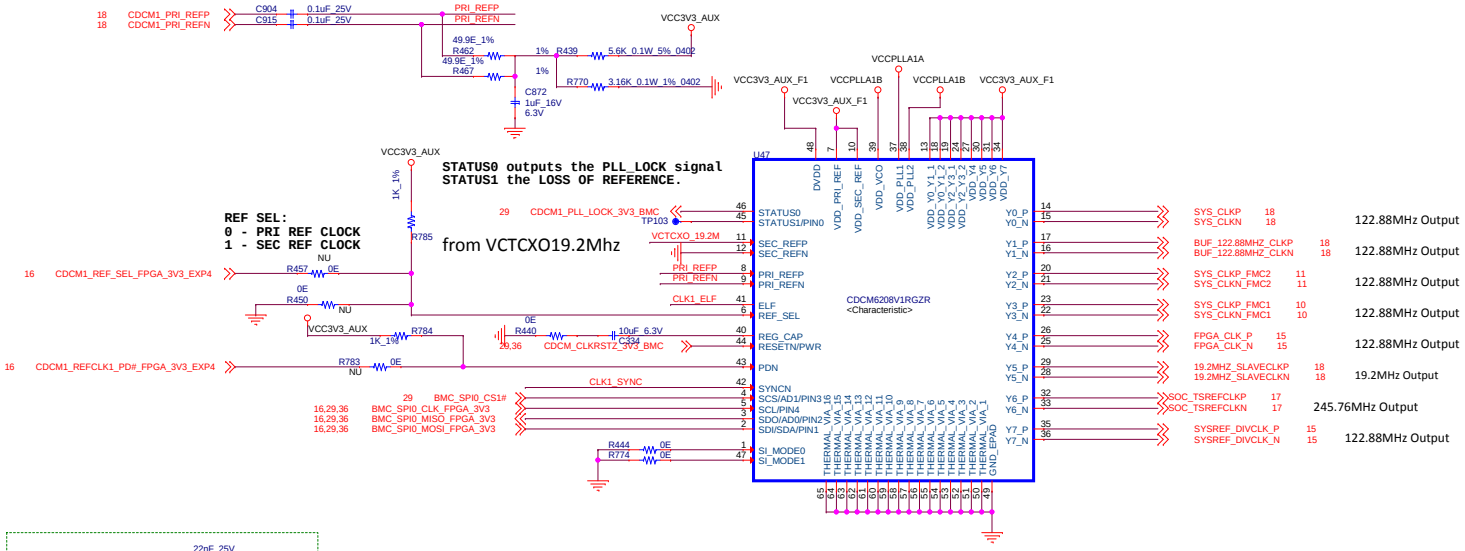


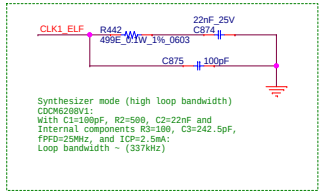




Project: K2L EVM	Designed for TI by eInfochips	
Title: Ethernet PHY, Magnetics for 2 channel/ Tx/Rx		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 34 of 47	

CDCM6208 Clk1, 122.88/19.2, Power Filter for Clock, VCTXCO, SPI 1.8/3.3v for 1588 DAC, VRef, 1588DAC



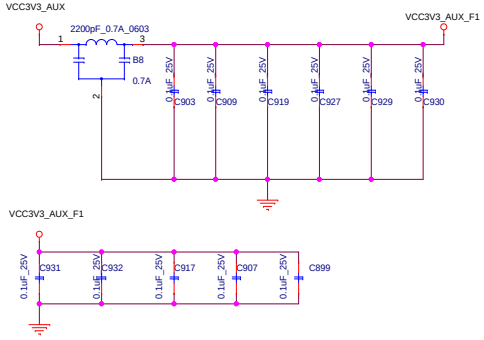


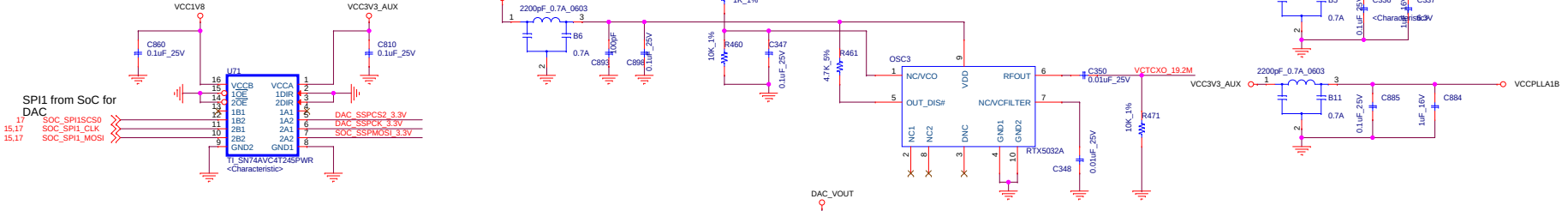
[Note]layout would place R440 and C334 close to U47.

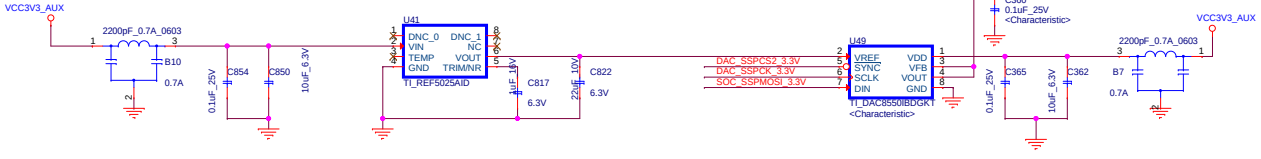
Serial Interface Mode or Pin Mode Selection

MCU_SI_MODE[1:0]	*DESCRIPTION*
00	*SPI MODE (Default)*
01	*I2C MODE*
10	*PIN MODE (NO SERIAL PROGRAMMING)*
11	*RESEERVED*

pull-up resister

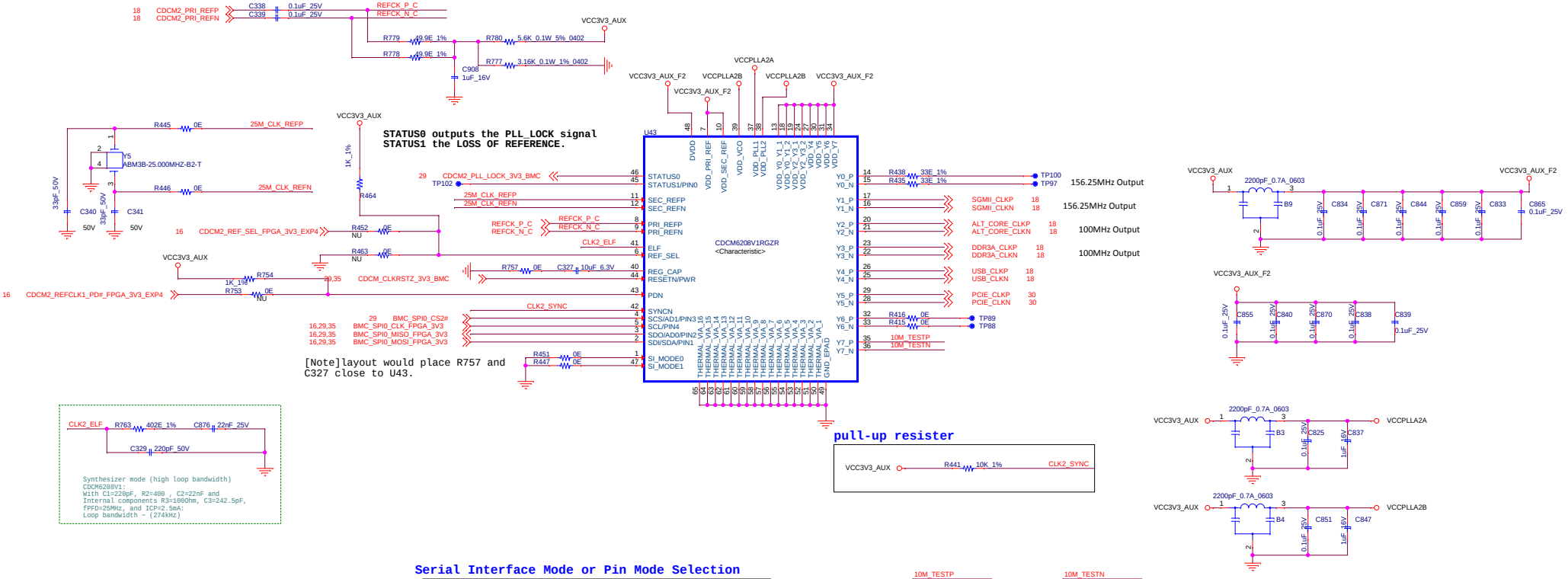






Project: K2L EVM	Designed for TI by eInfochips	
Title: CDCM62008 Clk1, 122.88/19.2, Power Filter for Clock,		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 35 of 47	

CDCM6208 Clk2, 100 / 156.25, Power Filter for Clock

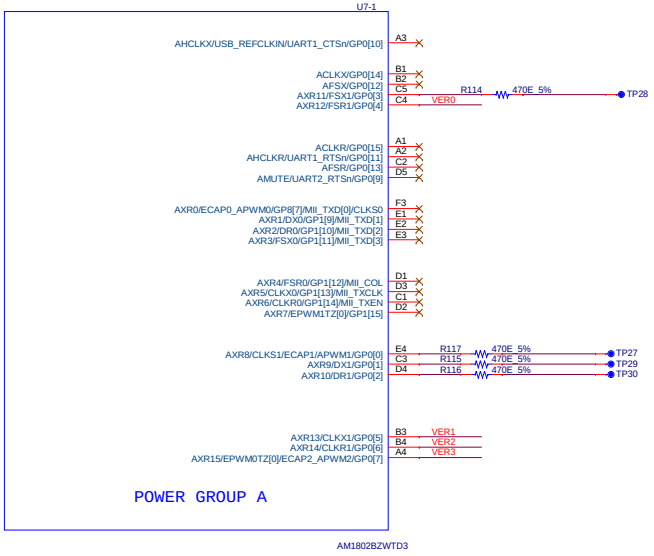


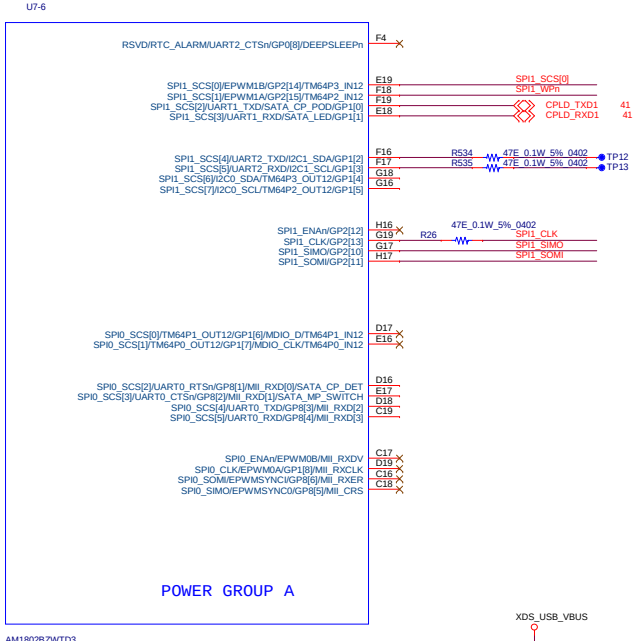
Serial Interface Mode or Pin Mode Selection

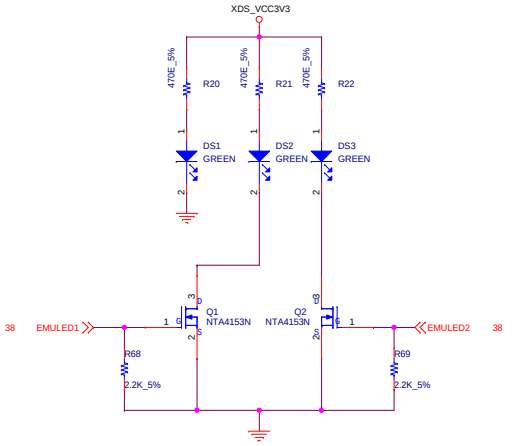
MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEERVED

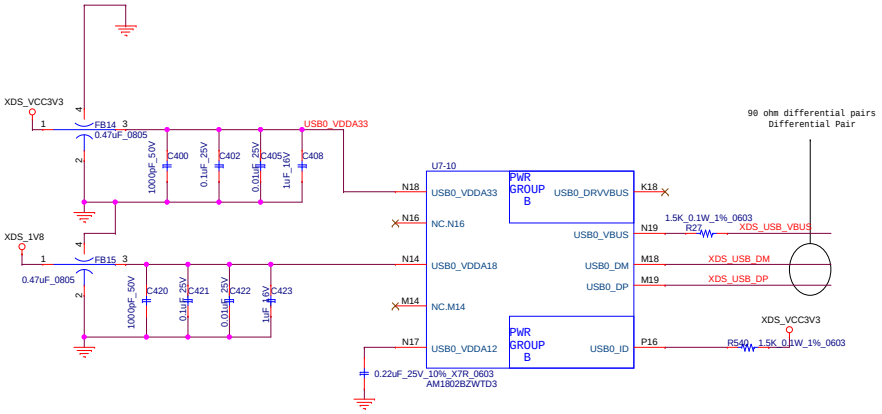
Project: K2L EVM		Designed for TI by eInfochips
Title: CDCM62008 Clk2, 100 / 156.25, Power Filter for Clock		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 36 of 47	

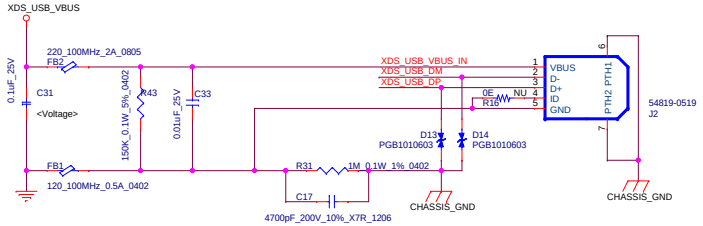
XDS200 / AM1802, flash, USB connector for Emulator



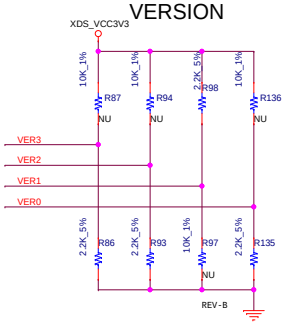


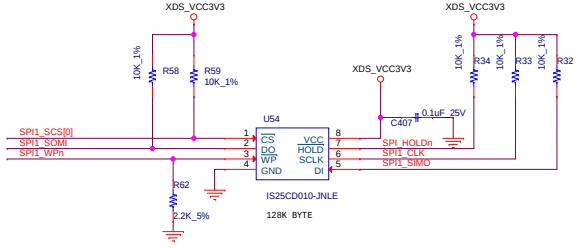






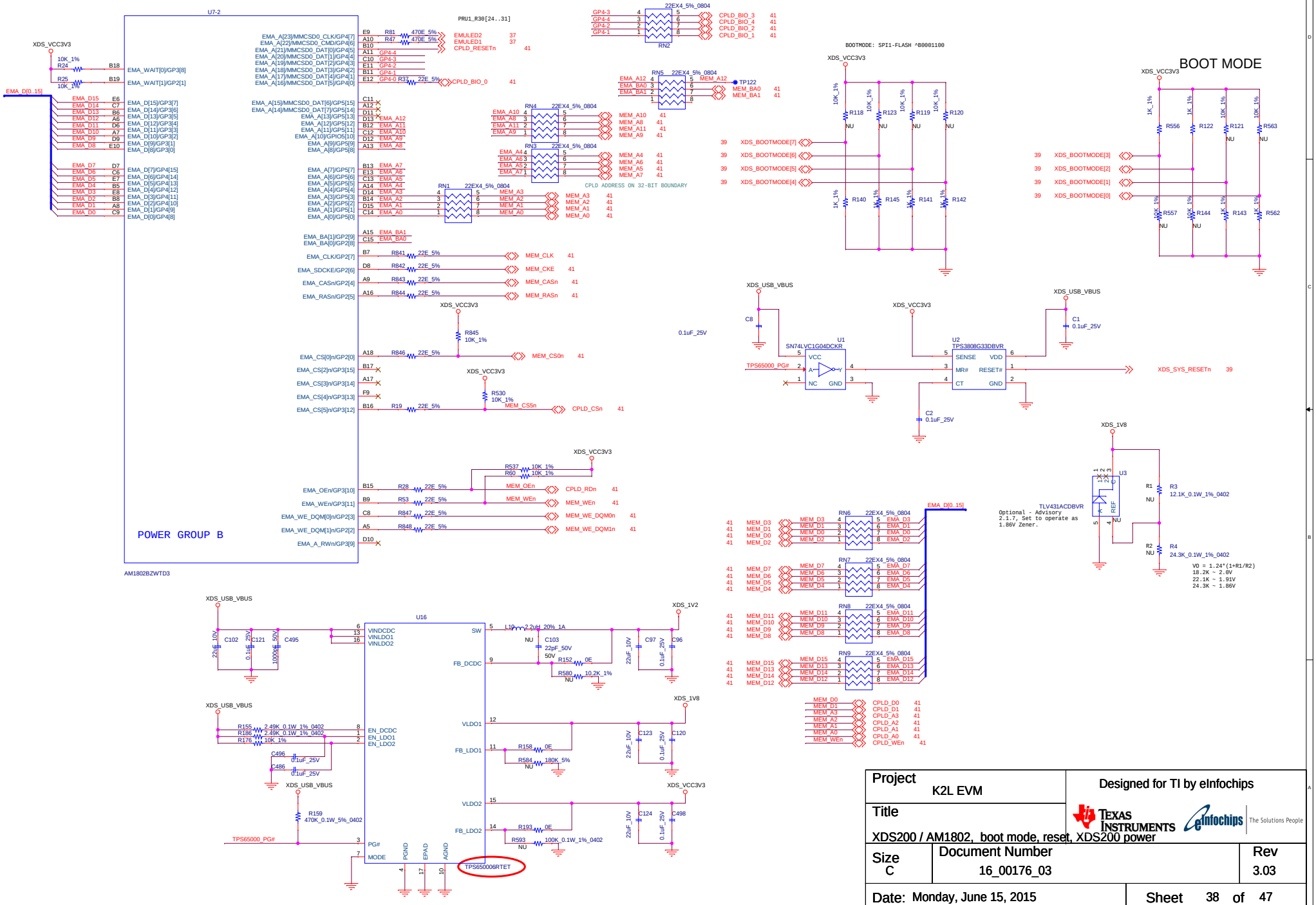
VERSION





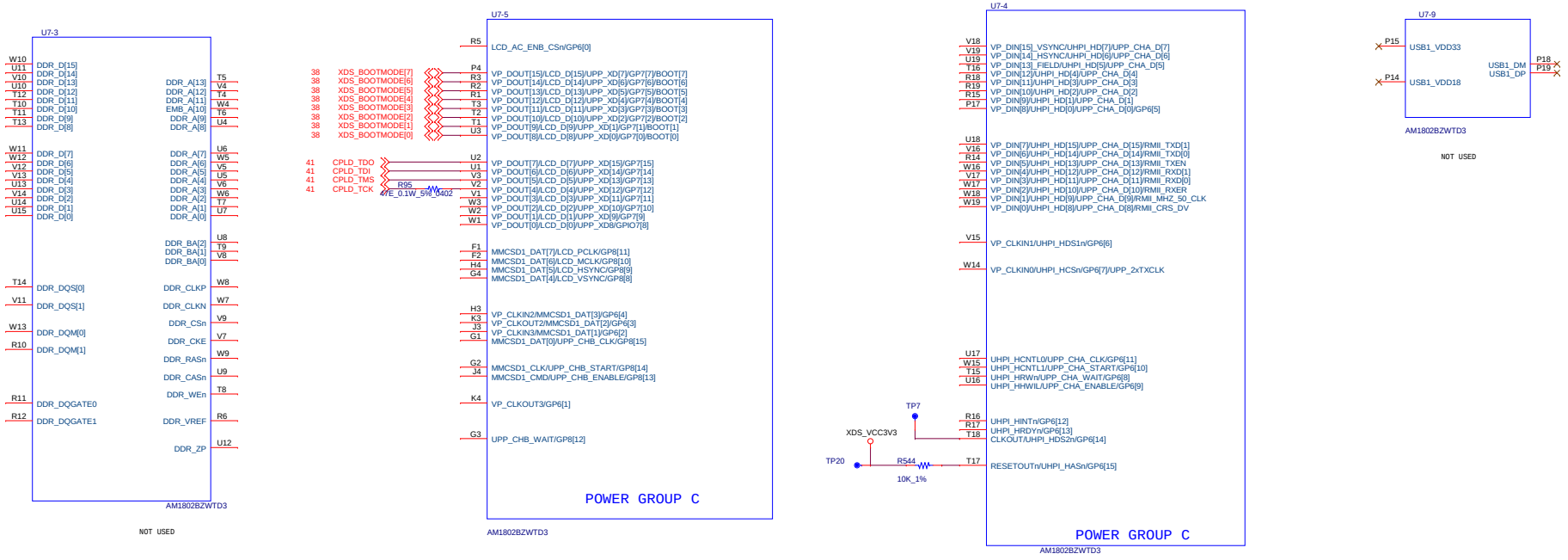
Project: K2L EVM	Designed for TI by eInfochips	
Title: XDS200 / AM1802, flash, USB connector for Emulator		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 37 of 47	

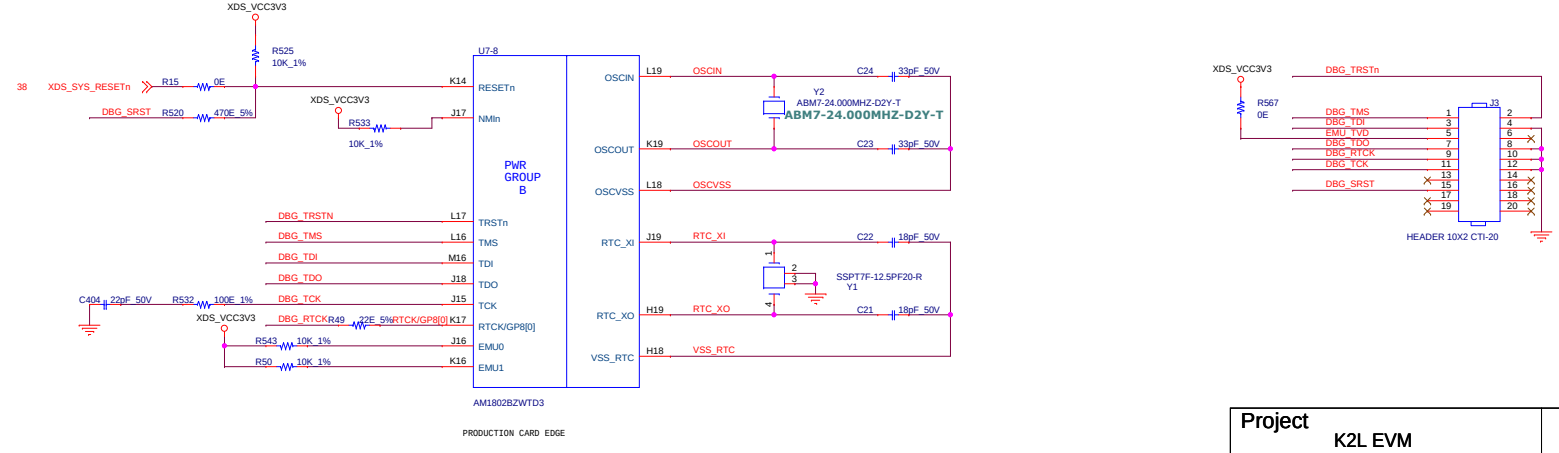
XDS200 / AM1802, boot mode, reset, XDS200 power



Project: K2L EVM		Designed for TI by eInfochips
Title: XDS200 / AM1802, boot mode, reset, XDS200 power		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 38 of 47	

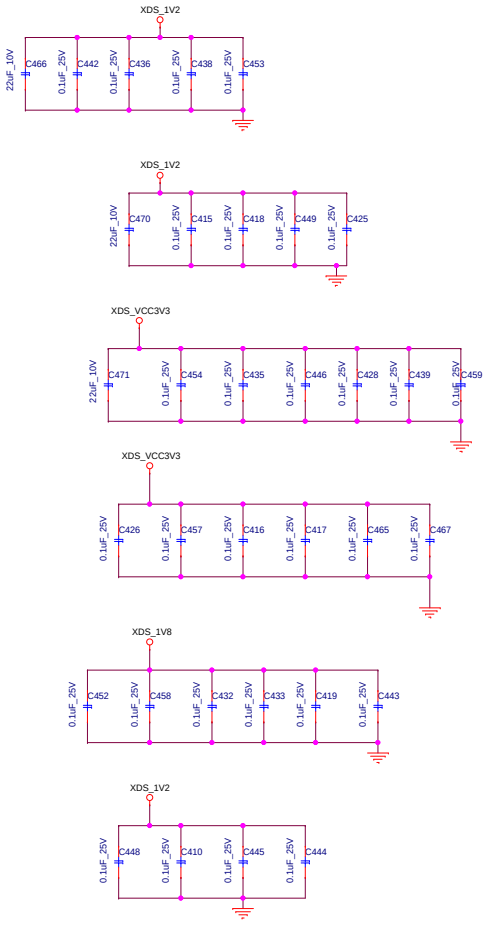
XDS200 / debug hdr, oscillators

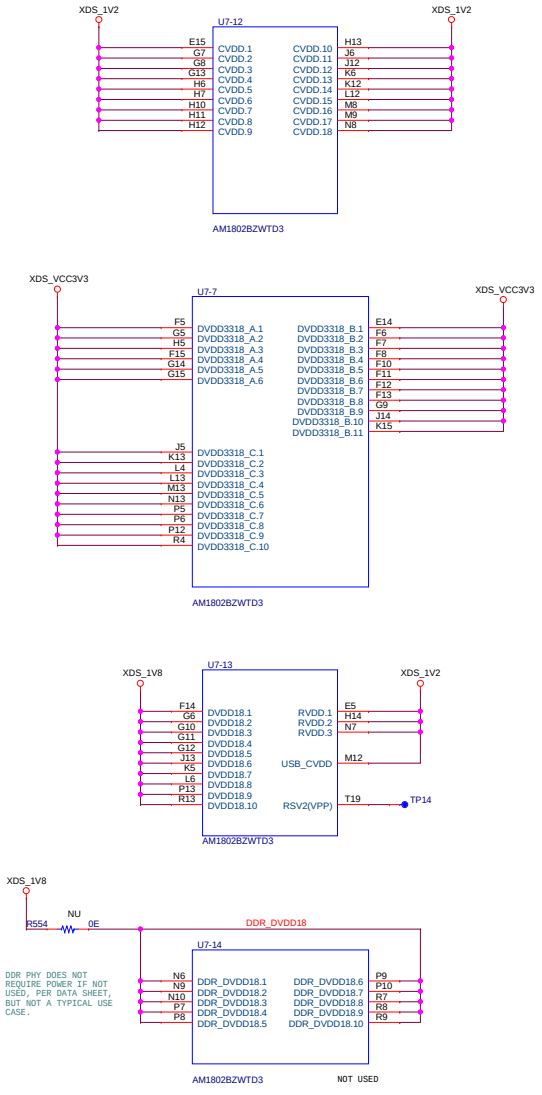


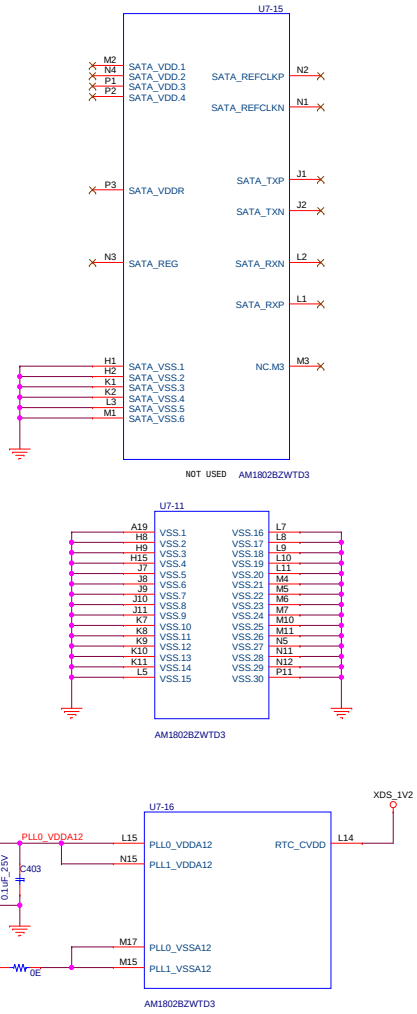


Project: K2L EVM		Designed for TI by eInfochips
Title: XDS200 / debug hdr, oscillators		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 39 of 47	

XDS200 Power

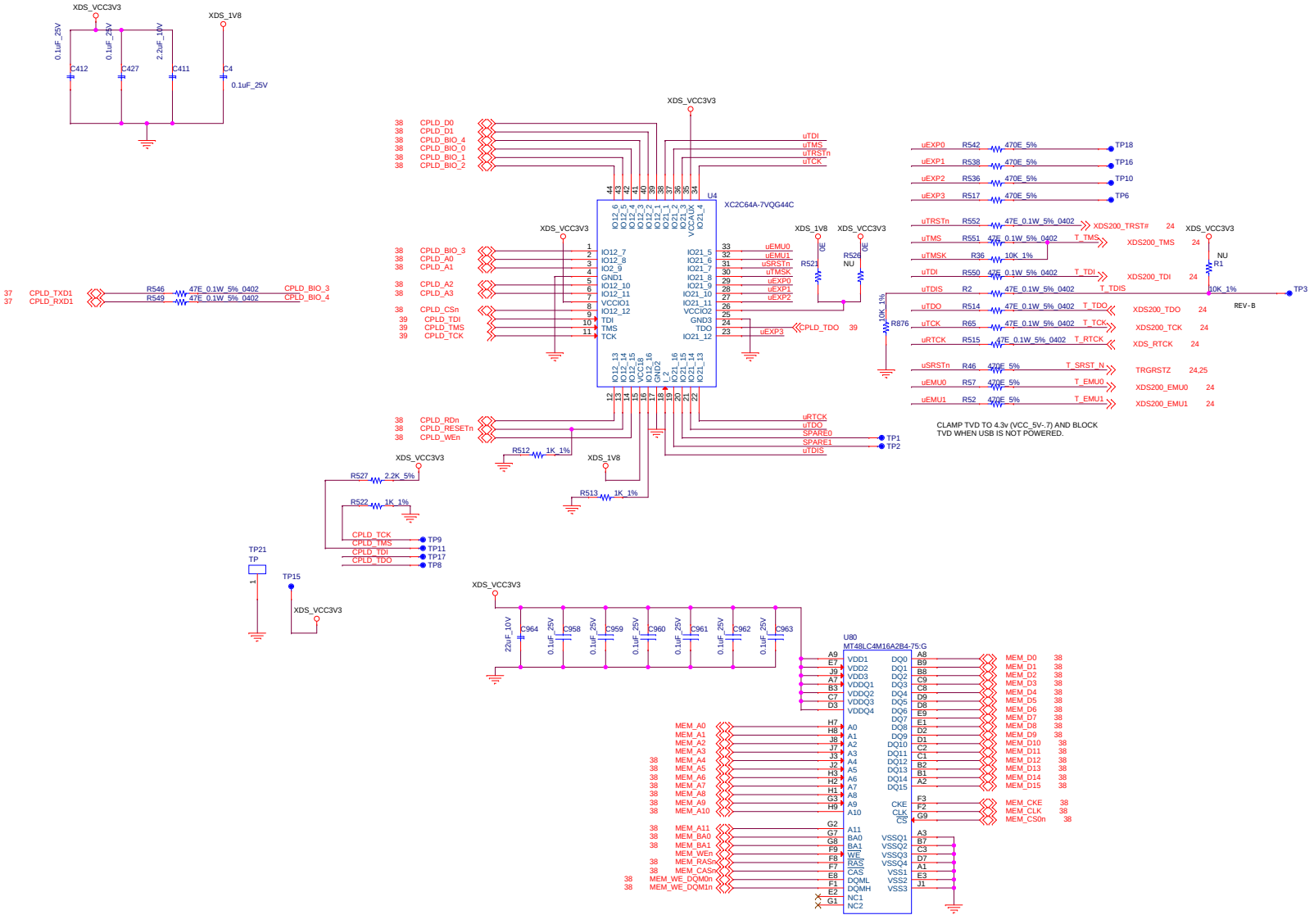






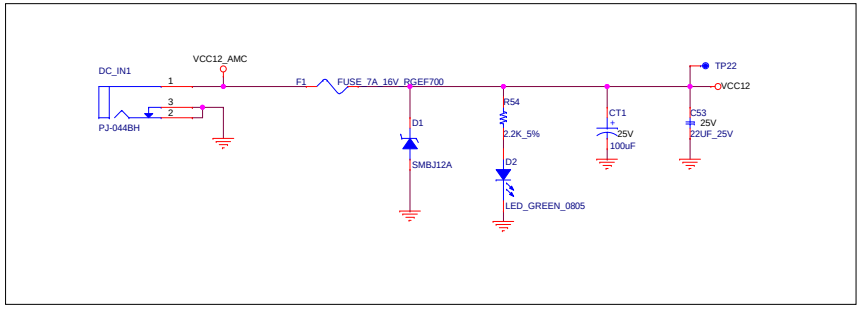
Project: K2L EVM		Designed for TI by eInfochips
Title: XDS200 Power		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015		Sheet 40 of 47

XDS200 Emulation CPLD

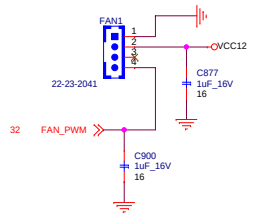


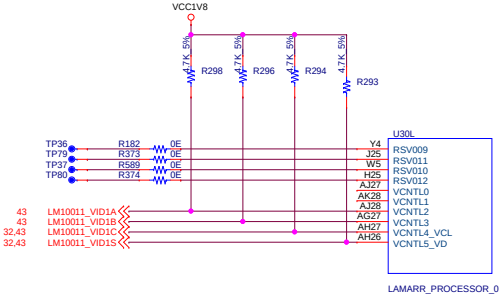
Project	K2L EVM	Designed for TI by eInfochips	
Title	XDS200 Emulation CPLD		
Size C	Document Number 16_00176_03		Rev 3.03
Date: Monday, June 15, 2015		Sheet 41 of 47	

12v input (fused), 12v to 3p3v MP, K2L VID, 1p8 to VPP1p8 switch, 3v3Aux to 3v3, FMC1 Power (fuse), FMC2 Power (fuse), fan connector

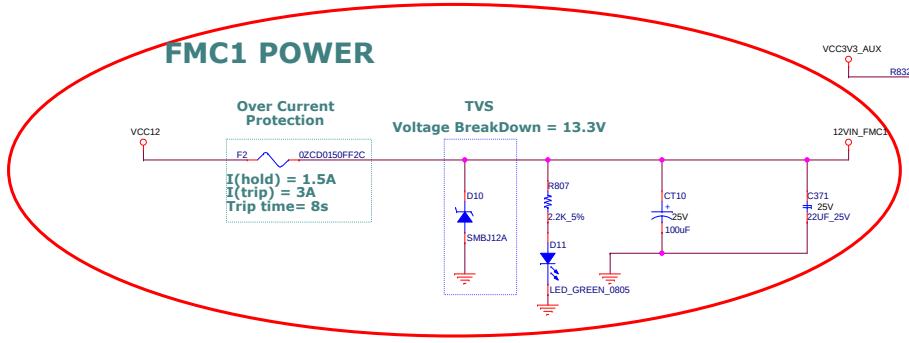


DC FAN Connector for SOC

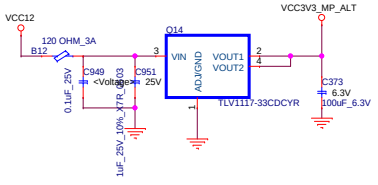




FMC1 POWER

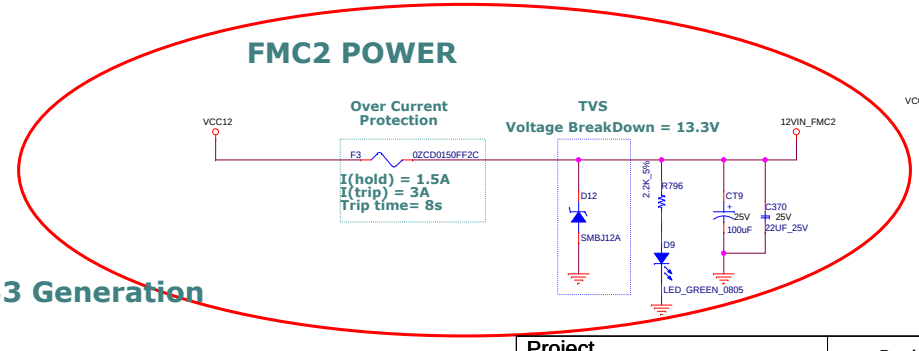


12V to VCC3V3_MP_ALT Generation

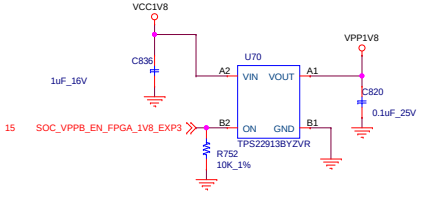


3V3_MP @ 150mA

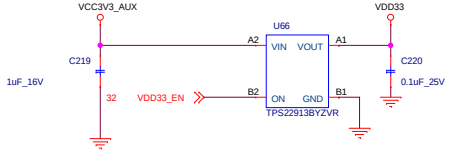
FMC2 POWER



VCC1V8 to VPP1V8



3V3_AUX to VDD33 Generation



Project: K2L EVM		Designed for TI by eInfochips
Title: 12v input (fused), 12v to 3p3v MP, K2L VID, 1p8 to VPP1p8 switch, 3v3Aux to 3v3, FMC1 Power (fuse),		
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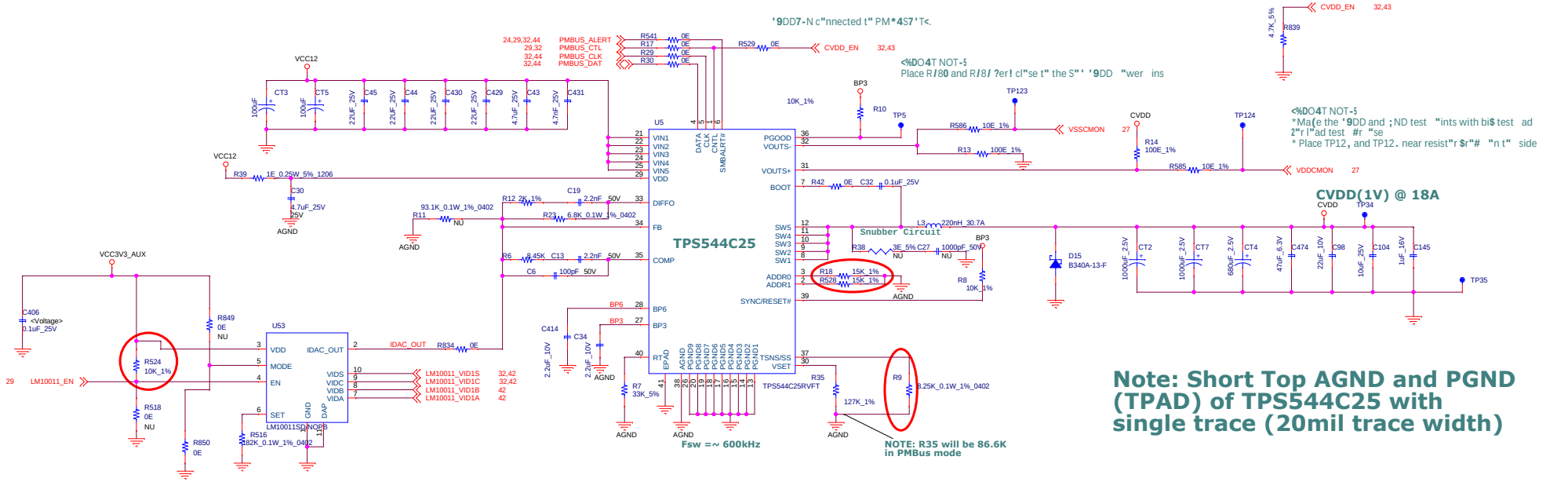
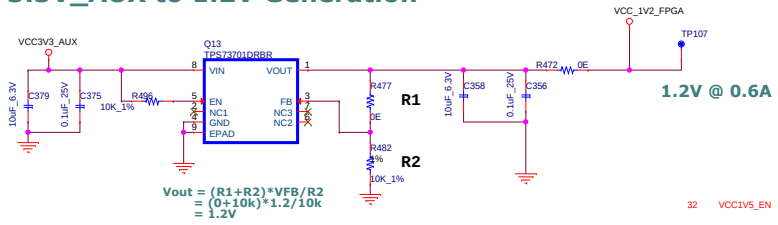
Top Avatar, 12v to CVVD , 12v to 1.5v, 3.3v aux -> 1.2v, 3.3v aux -> 1.8v

12V to CVDD Generation

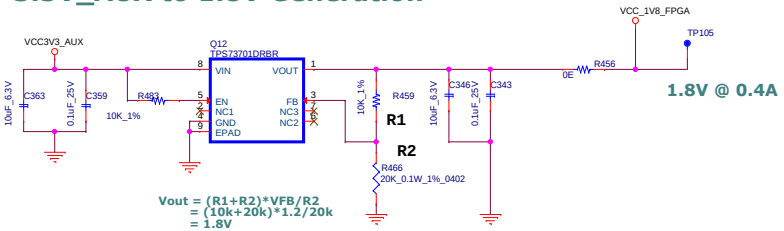


Note: Short Top AGND and PGND (TPAD) of TPS544C25 with single trace (20mil trace width)

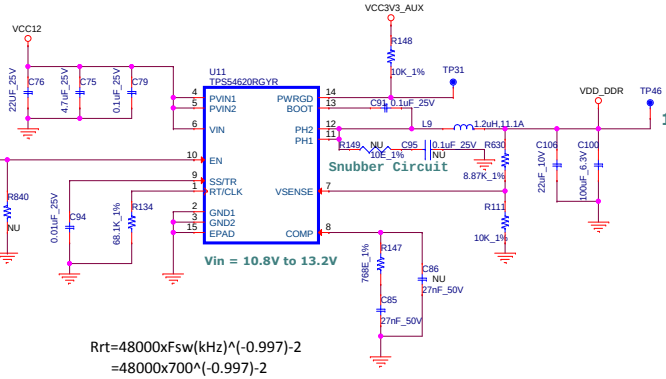
3.3V_AUX to 1.2V Generation



3.3V_AUX to 1.8V Generation



12V to 1.5V Generation



Vout=0.8 V*(R1/R2+1)
=0.8 V*(8.87k/10k+1)
=1.5V
(KIND=0.3)
+++Inductor Calculation+++
L = (Vin - Vout)/(Iout * Kind) * (Vout/(Vin * Fsw)
L = ((12 - 1.5)/(4.5A * 0.3) * (1.5 / (12 * 700kHz))
L = ~1.388u

Rrt=48000xFsw(kHz)^(-0.997)-2
=48000x700^(-0.997)-2
=~67.93 (k ohms)

(Over all tolerance is 5% ,DC tolerance is 2.5%)
+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*1/(700kHz*0.125)
Cout=~22.8uF

Project: K2L EVM	Designed for TI by eInfochips	
Title: Top Avatar, 12v to CVVD , 12v to 1.5v, 3.3v aux -> 1.2v, 3.3v aux -> 1.8v		
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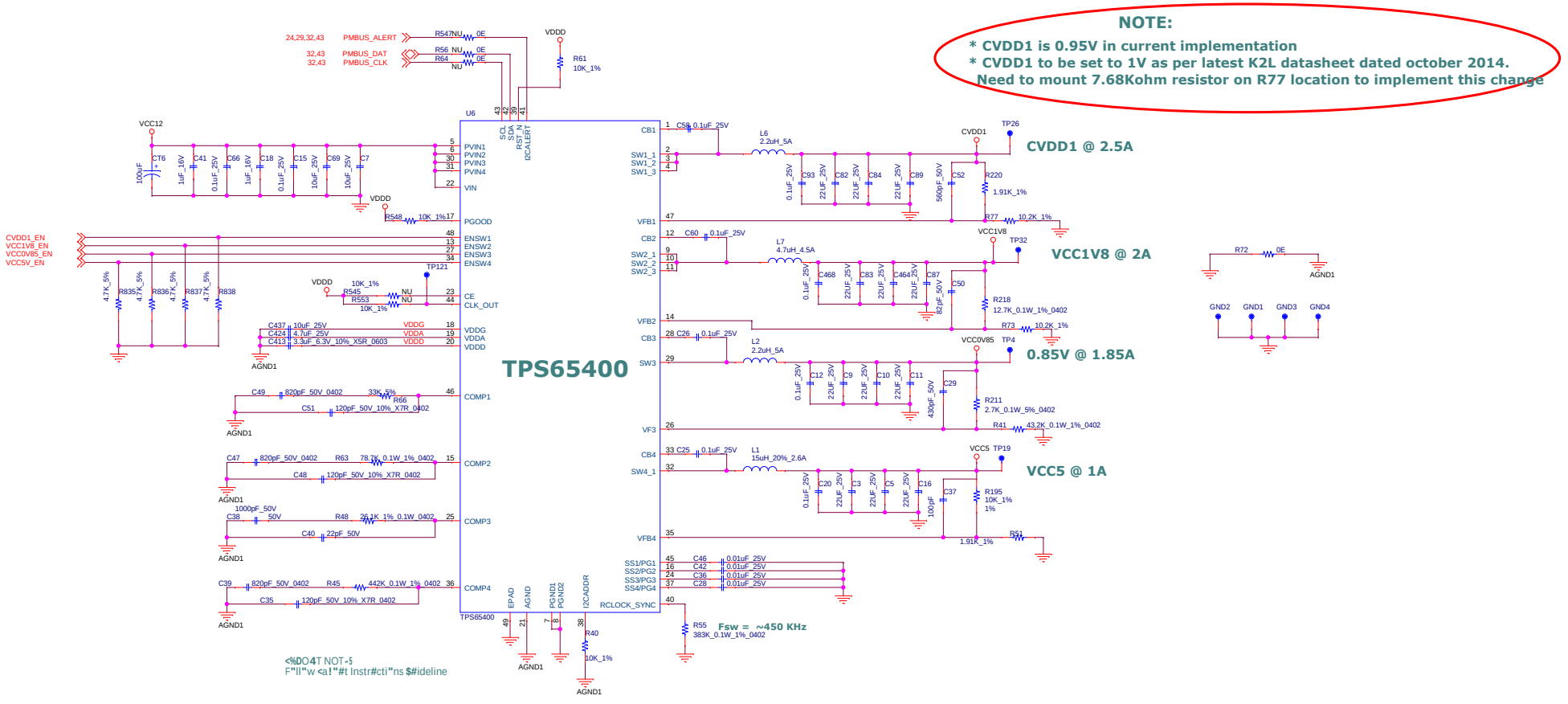
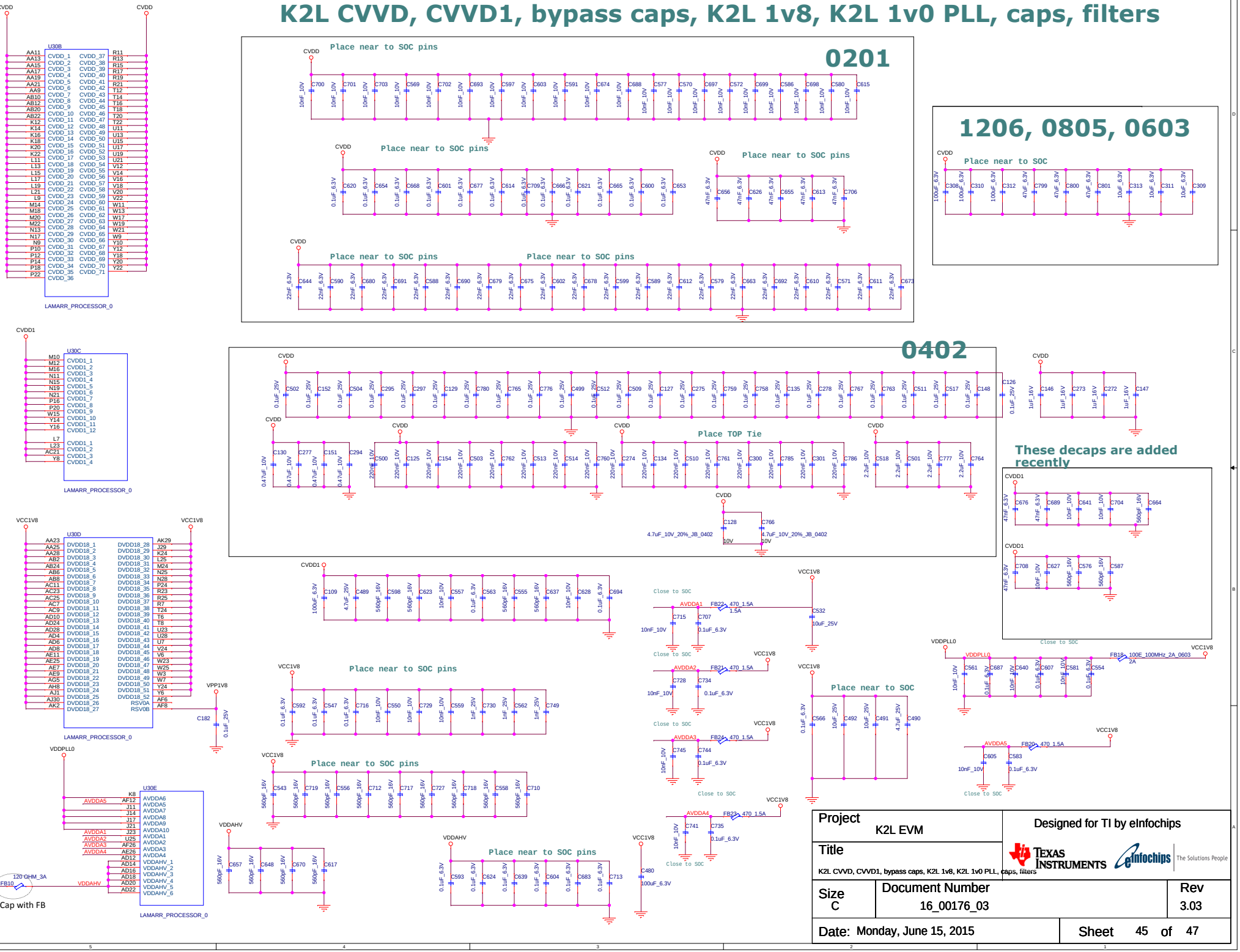
TPS65400, 12v -> CVVD1, 1v8, v85, 5v



Project: K2L EVM		Designed for TI by eInfochips
Title: LM26430, 12v -> CVVD1, 1v8, v85, 5v		
Size: C	Document Number: 16_00176_03	Rev: 3.03
Date: Monday, June 15, 2015	Sheet 44 of 47	

K2L CVVD, CVVD1, bypass caps, K2L 1v8, K2L 1v0 PLL, caps, filters



Project: K2L EVM		Designed for TI by eInfochips
Title: K2L CVVD, CVVD1, bypass caps, K2L 1v8, K2L 1v0 PLL, caps, filters		
Size: C	Document Number: 16_00176_03	Rev: 3.03
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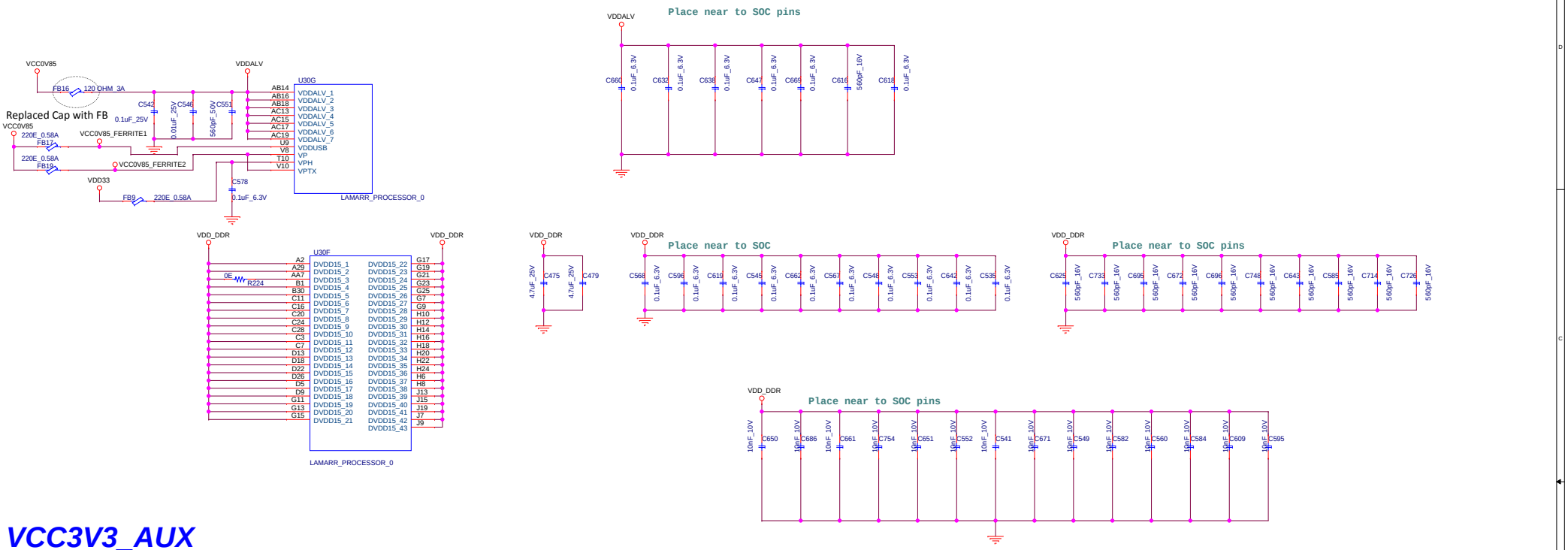
K2L VDDALV, v85 filter, bypass caps, 12v -> 3.3vaux

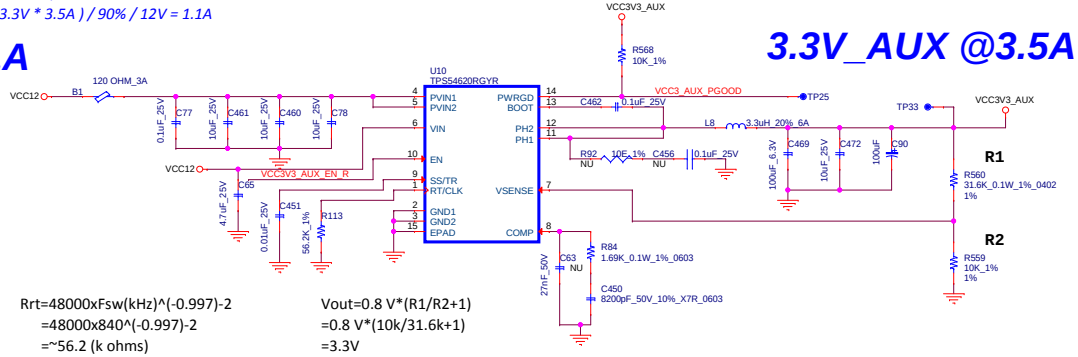


VCC3V3_AUX

Assume 90% Pe,
*Iin = (3.3V * 3.5A) / 90% / 12V = 1.1A*

12V@1.1A

3.3V_AUX @3.5A



Rrt=48000xFsw(kHz)^(-0.997)-2
=48000x840^(-0.997)-2
=~56.2 (k ohms)

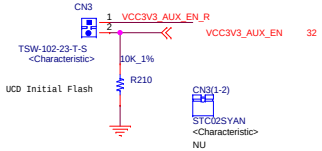
Vout=0.8 V*(R1/R2+1)
=0.8 V*(10k/31.6k+1)
=3.3V

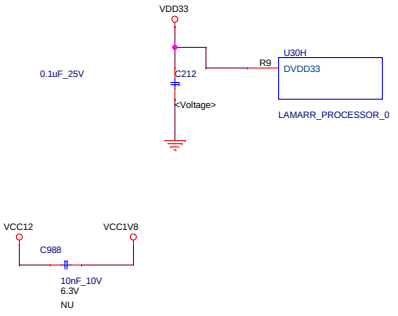
(Over all tolerance is 5% ,DC tolerance is 2.5%)
+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*3.5/(840kHz*0.0825)
Cout=~110.58uF

Re2erence 'a acit"rE100#F

(KIND=0.3)
+++Inductor Calculation+++
L = (Vin - Vout)/(Iout * Kind) * (Vout/(Vin * Fsw)
L = ((12 - 3.3)/(3.5A * 0.3) * (3.3 / (12 * 840kHz))
L = 8.2857 * 0.327u
L = ~2.71 uH

Re2erence Ind#ct"r ,.,#@





Project: K2L EVM	Designed for TI by eInfochips	
Title: K2L VDDALV, v85 filter, bypass caps, 12v -> 3.3vaux		
Size: C	Document Number: 16_00176_03	Rev: 3.03
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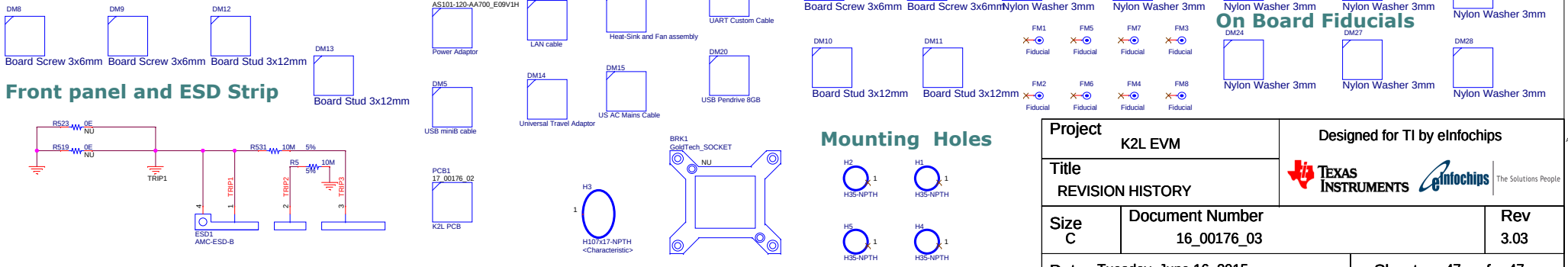
KEYSTONE2 LAMARR EVM - REVISION HISTORY

PCB. REV.	SCH. REV.	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	1.0	Release to Fabrication	24-DEC-2013	eInfochips
	1.01	1. SDRAM circuitry added in XDS section 2. TPS650006 is used instead of TPS650003 in XDS power section 3. Off page connectors used for SOC_I2C0_SDA, SOC_I2C0_SCL, SOC_I2C2_SDA, SOC_I2C2_SCL, LM10011_VID1C, LM10011_VID1S, SOC_UART0_TXD_3V3 nets 4. R626 made NU 5. J1 connector pin out details updated as per J5	23-JAN-2014	eInfochips
	1.02	1. Serdes switch settings changed to I2C mode from pin mode; [Pages - 12, 13, 14] 2. Ethernet configuration settings updated for 2.5V VDDO; [Pages - 31, 33, 34] 3. CP2105 - Self power mode option provided; [Page - 23]	12-MAR-2014	eInfochips
	1.03	1. Layout instruction is given for shorting AGND and PGND at a single point for Top Avatar section. [Page-43] 2. Termination provided for SOC_MDC_2V5 at AMC side. [Page-31] 3. Brightness reduced for the LEDs D5, DBG_D2 and DBG_D2., i.e, R353, R333 and R350 changed tp 120E from 10E [Page-16]	18-MAR-2014	eInfochips
	1.04	1. External networks provided for LVPECL logic implementation on U51 outputs. [Page-15] 2. Netname for the signal "CLK_MUXCTRL2_FPGA_3V3_EXP5" is changed to "CLK_MUXCTRL1_FPGA_3V3_EXP5". [Pages-16,18] 3. Netname for the signal "CLK_MUXCTRL3_FPGA_3V3_EXP5" is changed to "CLK_MUXCTRL2_FPGA_3V3_EXP5". [Pages-16,18]	25-MAR-2014	eInfochips
2.0	2.01	1. 10MHz clock circuit for clamping input signal to +1V. [Page18] 2. R1 made NU and C399 is replaced with R876. [Page41] 3. R90 made NU [Page24] 4. SPI2_MOSI/MISO option is mounted on board instead of UART1_TS/RTS - as UART1/SPI2 are multiplexed at SoC [Page17] 5. IRQ_FMC1_FPGA_3V3 is changed to pin R13 (I/O) from pin R8 (I) of FPGA; IRQ_FMC2_FPGA_3V3 is changed to pin T15 (I/O) from pin P13 (I) of FPGA. [Page16] 6. R413 made NU and R734 mounted with 10K 7. 100E resistor added to input of Clock buffer and other clocks 8. VBUS mode option provided instead of Self Powered Mode for CP2105 circuitry 9. In Cn14, Mfr Pno TSM-108-07-S-S is replaced with TSM-108-02-S-SV	1-MAY-2014	eInfochips
	2.02	1.CN21(2-3) changed to CN6(2-3); CN8(2-3) changed to CN10(2-3); CN2(1-2) changed to CN11(1-2) 2.CN24(1-2) changed to CN3(1-2)	10-JUL-2014	eInfochips
	2.03	DM21 to DM28 added	21-JUL-2014	eInfochips
	2.04	CN9(1-2) is replaced with CN13(1-2); R417 made NU.	4-AUG-2014	eInfochips
	2.05	CP2105 power changed to Vbus mode from Self Power mode	18-AUG-2014	eInfochips
	2.06	DDR3 SDRAM -ECC chip U31 made populated	2-SEP-2014	eInfochips
	2.06	Release to Fabrication	2-SEP-2014	eInfochips
3.0	3.00	1. JESD1 and JESD2 swapping for FMC1 and FMC2 connectors. 2. FMC power related components made NU (F2,F3,D9,D10,D11,D12,CT9,CT10,R796,R807,C370,C371,C377,C378,C952,C953) 3. 10MHz circuit changes implemented as per the 10MHz validation report uploaded on AC; R877,R879 made as NU;R878 replaced with 46.4K; R364 replaced with 3.16K 4. LM26430 is renamed as TPS65400. 5. R250 value changed to 33E resistor; R889 added and made NU 6. R9 value changed to 8.25K.	11-OCT-2014	eInfochips
	3.01	FMC power related components made Populated. (F2,F3,D9,D10,D11,D12,CT9,CT10,R796,R807,C370,C371,C377,C378,C952,C953)	28-OCT-2014	eInfochips
	3.02	R524 resistor is replaced with 10K resistor [page 43]	11-NOV-2014	eInfochips
	3.03	Main part number for U54 is updated to IS25CD010-JNLE from W25X10BVSNIG; Block diagram updated; Release to Fabrication	24-NOV-2014	eInfochips
	3.04	SoC pin name changed according to latest functionality	16-JUN-2015	eInfochips

Dummy Components



Front panel and ESD Strip

Mounting Holes

On Board Fiducials

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