TCIEVMK2LX Technical Reference Manual Version 1.0

Revised December 2014

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For EVMs not including a radio and not subject to the U.S. Federal Communications Commission (FCC) or Industry Canada (IC) regulations, TI intends EVMs to be used only for engineering development, demonstration, or evaluation purposes. EVMs are not finished products typically fit for general consumer use. EVMs may nonetheless generate, use, or radiate radio frequency energy, but have not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or the ICES-003 rules. Operation of such EVMs may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: For EVMs including a radio, the radio included in such EVMs is intended for development and/or professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability in such EVMs and their development application(s) must comply with local laws governing radio spectrum allocation and power limits for such EVMs. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by TI unless user has obtained appropriate experimental and/or development licenses from local regulatory authorities, which is the sole responsibility of the user, including its acceptable authorization.

U.S. Federal Communications Commission Compliance

For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Important Notice for Users of EVMs Considered "Radio Frequency Products" in Japan

EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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Preface

About this Document

This document is a Technical Reference Manual for the TCI6630K2L Evaluation Module designed and developed by eInfochips Limited for Texas Instruments, Inc.

Notational Conventions

This document uses the following conventions:

Program listings, program examples, and interactive displays are shown in a mono-spaced font. Examples use **bold** for emphasis, and interactive displays use bold to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Square brackets ([and]) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets. Unless the square brackets are in a bold typeface, do not enter the brackets themselves.

Underlined, italicized non-bold text in a command is used to mark place holder text that should be replaced by the appropriate value for the user's configuration.

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Document Revision History

Release	Chapter	Description of Change
1.0	All	Initial Draft

Acronyms

Acronym	Description
AMC or AdvancedMC	Advanced Mezzanine Card
AIL	Antenna Interface Link
CCS	Code Composer Studio
DDR3	Double Data Rate 3 Interface
DIP	Dual-In-Line Package
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
EEPROM	Electrically Erasable Programmable Read Only Memory
EMAC	Ethernet Media Access Controller
EMIF	External Memory Interface
EVM	Evaluation Module
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
I2C	Inter Integrated Circuit
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LED	Light Emitting Diode
McBSP	Multi Channel Buffered Serial Port
MCH	MicroTCA Carrier Hub
MTCA or MicroTCA	Micro Telecommunication Computing Architecture
MMC	Module Management Controller
PCIe	PCI Express
PICMG®	PCI Industrial Computer Manufacturers Group
RFU	Reserved for Future Use
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer-Deserializer
SGMII	Serial Gigabit Media Independent Interface
SRIO	Serial RapidIO
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

XDS560v2	Texas Instruments' XDS560v2 System Trace Emulator
XDS200	Texas Instruments' XDS200 Emulator

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1. Overview

This chapter provides an overview of the TCIEVMK2LX Evaluation Module (EVM) along with the key features and block diagram.

1.1 Key Features

The TCIEVMK2LX Evaluation Module (EVM) is a high performance, cost-efficient, standalone development platform that enables users to evaluate and develop applications for the Texas Instruments' Keystone II SoC. The TCIEVMK2LX Evaluation Module (EVM) also serves as a hardware reference design platform for the TCI6630K2L SoC. The EVM's form-factor is equivalent to a Double-wide PICMG® AMC.0 R2.0 AdvancedMC module.

Schematics, code examples and application notes are available, to ease the hardware development process and to reduce the time to market.

The key features of TCIEVMK2LX Evaluation Module (EVM) are:

- Texas instrument's Four DSP Core + Two ARM Core SoC
- 2 GB ECC DDR3 1600
- 512 MB of NAND Flash
- 128 MB of NOR Flash
- Four Gigabit Ethernet ports supporting 10/100/1000 Mbps data-rate – two on AMC connector and two RJ-45 connector
- 170 pin B+ style AMC Interface containing PCIe, SGMII, AIL
- Two FMC Connector for AFE7500EVM Interface containing high speed 4 JESD pairs and 2 JESD pairs
- One host USB3.0 port
- 128 KB I2C EEPROM for booting
- 4 User Indication LEDs, 1 Banks of DIP Switches
- Two RS232 serial interface on 4-Pin header or UART over USB miniB
- Timer, SPI,UART,I2C,GPIO,EMIF interfaces on 120-pin expansion header
- Supports On Board Emulation (XDS200) as well as External Emulator
- Supports External Emulator (i.e. XDS560) through MIPI 60-Pin connector
- Powered by DC power-brick adaptor (12V/7A) or AMC Carrier back-plane
- High-speed DSP interconnect enabled by Gigabit EMAC interfaces
- One USIM interface
- One GPS module on board
- One LCD display for debugging states
- RoHS Compliant Design
- Double wide PICMG ® AdvancedMC (AMC) form factor (7.11" x 5.84")
- Board Management Controller (BMC) for Intelligent Platform Management Interface (IPMI)

1.2 Functional Overview

The TCIEVMK2LX Evaluation Module (EVM) contains TCI6630K2L SoC platform. TCI6630K2L device is based on industry's leading high performance multi core Keystone II architecture. It has Four TMS320C66x™ DSP Core and Two ARM Cortex™-A15 MPCore™ Processors. TCI6630K2L is a low-power baseband solution with integrated digital front end (DFE) that meets the more stringent power, size, and cost requirements of small cell wireless base stations. This device's ARM and DSP cores deliver exceptional processing power on platforms for developing all wireless standards including WCDMA/HSPA/HSPA+, TD-SCDMA, GSM, TDD-LTE, FDD-LTE, and WiMAX.

The functional block diagram of TCIEVMK2LX Evaluation Module (EVM) is shown in below figure:

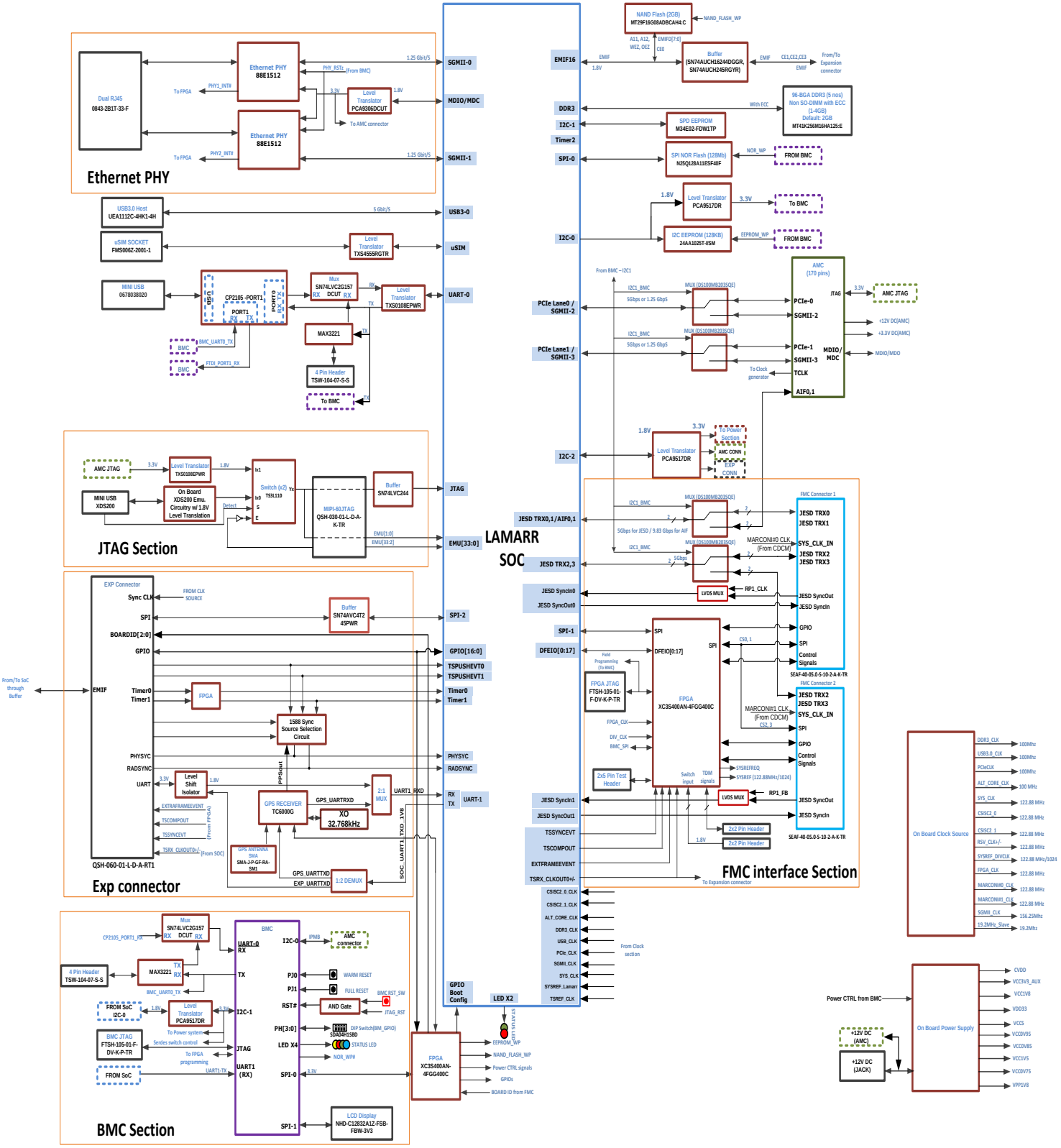


Figure 1.1: Block Diagram of TCIEVMK2LX EVM

1.3 Basic Operation

The TCIEVMK2LX EVM platform is designed to work with TI's Code Composer Studio (CCS) development environment and ships with a version specifically tailored for this board. CCS can interfaces with the board via on-board emulation circuitry using the USB cable supplied along with this EVM or through external emulator.

The EVM comes with the Texas Instruments Multicore Software Development Kit (MCSDK) for SYS/BIOS OS. The BIOS MCSDK provides the core foundational building blocks that facilitate application software development on TI's high performance and multicore DSPs. It also includes U-Boot, Kernel, File System and Matrix Demo. Follow the instruction in BIOS MCSDK Getting Started Guide to install all the necessary development tools, drivers and documentation.

To start operating the board, follow instructions given in the Quick Start Guide. This guide provides instructions for proper connections and configuration for booting Linux kernel and running the Matrix Demo. After completing the Matrix Demo, proceed with installations of CCS and the EVM support files by following the instructions given in the Flash Drive. This process will install all the necessary development tools, drivers and documentation.

After the installation is completed, follow below steps to run Code Composer Studio.

1. Power ON the board using power brick adaptor (12V/7A) supplied along with this EVM.
2. Connect USB cable from host PC to EVM board.
3. Launch Code Composer Studio from host PC by double clicking on its icon at PC desktop.

Detailed information about the EVM including examples and reference material is available in the Flash Drive available with this EVM kit.

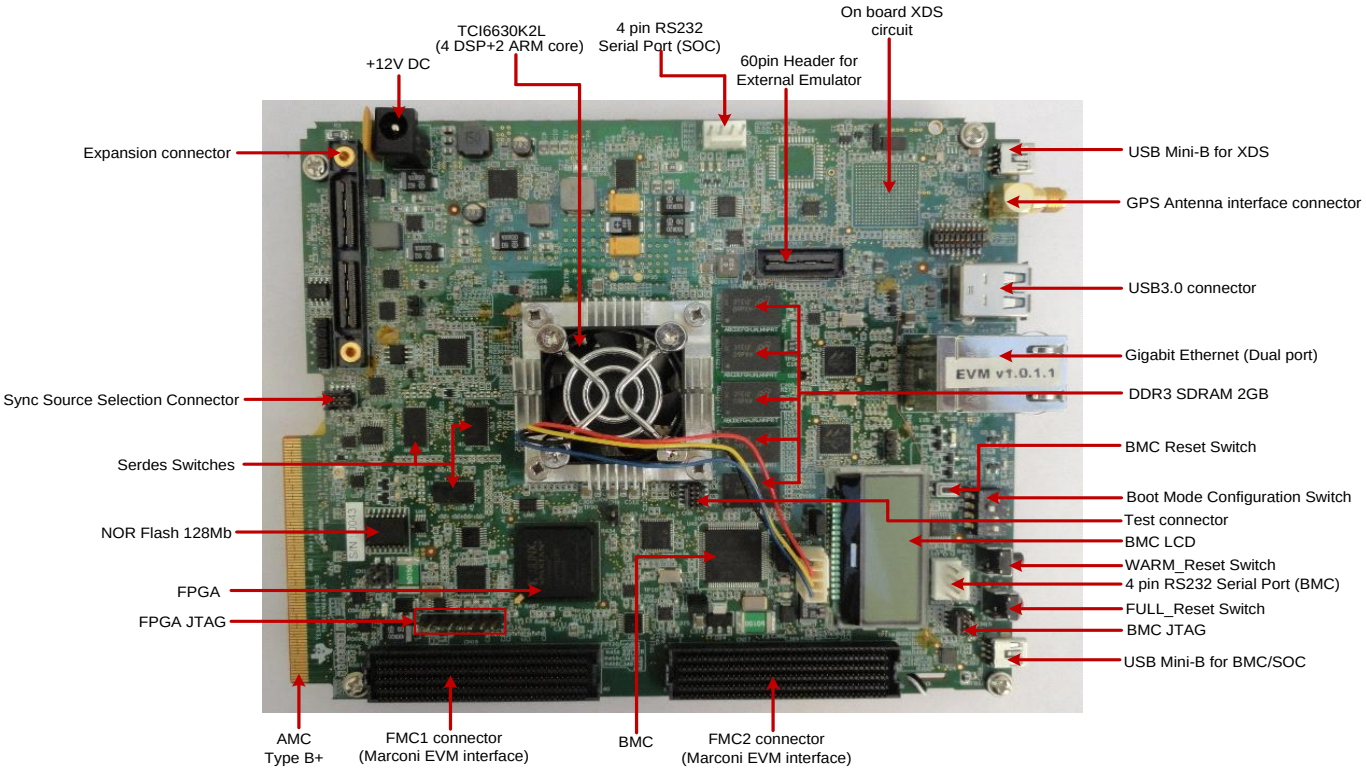


Figure 1.2: TCIEVMK2LX EVM Top Side

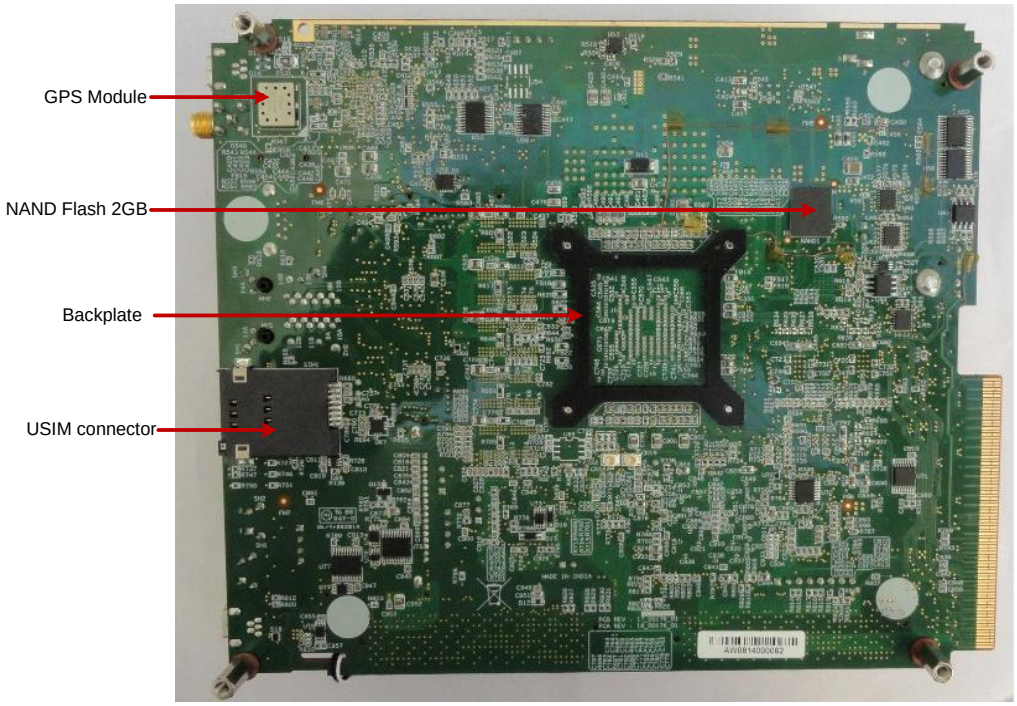


Figure 1.3: TCIEVMK2LX EVM Bottom Side

1.4 Boot Mode and Boot Configuration Switch Setting

The TCIEVMK2LX EVM has 4 sliding DIP switches (Board Ref. SW1) to determine boot mode, boot configuration, device number, Endian mode, CorePac PLL clock, JESD mode slection and PCIe mode selection. Mode selection options latch at every reset of the DSP. Please refer Table 3.23 for Boot mode configuration settings.

1.5 Power Supply

TCIEVMK2LX Evaluation Module (EVM) can be powered from a single +12V / 7A DC (84W) external power supply connected to DC power jack (DC_IN1). +12V input is converted into required voltage levels using on board DC-DC converters.

- +0.8 - +1.1 V is Smart Reflex enabled DSP core variable supply voltage
- +0.95V is used for DSP core fixed supply voltage and internal memory
- +1.5V is used for DDR3 I/O of SoC and DDR3 chips
- +0.75V is DDR3 reference voltage supply
- +0.85V is used for SerDes analog power supply voltage
- +0.85V is used for USB LV PHY power supply voltage
- +1.8V is used for SerDes I/O, Core PLL, DDR3 DLL and FPGA I/O
- +2.5V is used for Gigabit Ethernet PHY
- +3.3V is used for FPGA I/O, microcontroller and other on board circuit
- +1.2V is used for FPGA Core and Gigabit Ethernet PHY core
- +5.0V is used for USB power supply and XDS circuit
- +12V used to power up FMC card

The TCIEVMK2LX Evaluation Module (EVM) can also be powered up from the AMC edge connector (AMC1). If the board is inserted into a PICMG® AMC.0 R2.0 compliant system chassis or AMC Carrier back-plane, an external +12V supply from DC jack (DC_IN1) is not required.

Note:
External Power Supply Requirements:
Nom Voltage: 12 VDC
Max Current: 7000 mA
Efficiency Level V

External Power Supply Regulatory Compliance Certifications: Recommend selection and use of an external a power supply which meets TI's required minimum electrical ratings in addition to complying with applicable regional product regulatory/safety certification requirements such as (by example) UL, CSA, VDE, CCC, PSE, etc.

2. Introduction to TCIEVMK2LX Evaluation board

This chapter provides an introduction and details of interfaces for the TCIEVMK2LX EVM board. It contains:

2.1 Memory Map

The memory map of the TCI6630K2L device is as shown in Table 2.1.

Table 2.1: TCI6630K2L Memory Map

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 0000 0000	00 0003 FFFF	256K	ARM ROM	Reserved	ARM ROM
00 0004 0000	00 007F FFFF	8M-256K	Reserved	Reserved	Reserved
00 0080 0000	00 008F FFFF	1M	Reserved	L2 SRAM	L2 SRAM
00 0090 0000	00 00DF FFFF	5M	Reserved	Reserved	Reserved
00 00E0 0000	00 00E0 7FFF	32K	Reserved	L1P SRAM	L1P SRAM
00 00E0 8000	00 00EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 00F0 0000	00 00F0 7FFF	32K	Reserved	L1D SRAM	L1D SRAM
00 00F0 8000	00 00FF FFFF	1M-32K	Reserved	Reserved	Reserved
00 0100 0000	00 0100 FFFF	64K	ARM AXI2VBUSM Master Registers	C66x CorePac registers	C66x CorePac registers
00 0101 0000	00 010F FFFF	1M-64K	Reserved	C66x CorePac registers	C66x CorePac registers
00 0110 0000	00 0110 FFFF	64K	ARM STM Stimulus Ports	C66x CorePac registers	C66x CorePac registers
00 0111 0000	00 01BF FFFF	11M-64K	Reserved	C66x CorePac registers	C66x CorePac registers
00 01C0 0000	00 01CF FFFF	1M	Reserved	Reserved	Reserved
00 01D0 0000	00 01D0 007F	128	Tracer CFG0	Tracer CFG0	Tracer CFG0
00 01D0 0080	00 01D0 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D0 8000	00 01D0 807F	128	Tracer CFG1	Tracer CFG1	Tracer CFG1
00 01D0 8080	00 01D0 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D1 0000	00 01D1 007F	128	Tracer CFG2	Tracer CFG2	Tracer CFG2
00 01D1 0080	00 01D1 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D1 8000	00 01D1 807F	128	Tracer CFG3	Tracer CFG3	Tracer CFG3
00 01D1 8080	00 01D1 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D2 0000	00 01D2 007F	128	Tracer CFG23	Tracer CFG23	Tracer CFG23
00 01D2 0080	00 01D2 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D2 8000	00 01D2 807F	128	Tracer CFG8	Tracer CFG8	Tracer CFG8
00 01D2 8080	00 01D2 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D3 0000	00 01D3 007F	128	Tracer CFG20	Tracer CFG20	Tracer CFG20
00 01D3 0080	00 01D3 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D3 8000	00 01D3 807F	128	Tracer CFG21	Tracer CFG21	Tracer CFG21
00 01D3 8080	00 01D3 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D4 0000	00 01D4 007F	128	Tracer CFG25	Tracer CFG25	Tracer CFG25
00 01D4 0080	00 01D4 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D4 8000	00 01D4 807F	128	Tracer CFG09	Tracer CFG09	Tracer CFG09
00 01D4 8080	00 01D4 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D5 0000	00 01D5 007F	128	Tracer CFG10	Tracer CFG10	Tracer CFG10
00 01D5 0080	00 01D5 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D5 8000	00 01D5 807F	128	Tracer CFG11	Tracer CFG11	Tracer CFG11
00 01D5 8080	00 01D5 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D6 0000	00 01D6 007F	128	Tracer CFG12	Tracer CFG12	Tracer CFG12

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 01D6 0080	00 01D6 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D6 8000	00 01D6 807F	128	Reserved	Reserved	Reserved
00 01D6 8080	00 01D6 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D7 0000	00 01D7 007F	128	Reserved	Reserved	Reserved
00 01D7 0080	00 01D7 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D7 8000	00 01D7 807F	128	Reserved	Reserved	Reserved
00 01D7 8080	00 01D7 FFFF	32K-128	Reserved	Reserved	Reserved
00 01D8 0000	00 01D8 007F	128	Reserved	Reserved	Reserved
00 01D8 0080	00 01D8 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D8 8000	00 01D8 807F	128	Tracer CFG26	Tracer CFG26	Tracer CFG26
00 01D8 8080	00 01D8 8FFF	32K-128	Reserved	Reserved	Reserved
00 01D9 0000	00 01D9 007F	128	Tracer CFG27	Tracer CFG27	Tracer CFG28
00 01D9 0080	00 01D9 7FFF	32K-128	Reserved	Reserved	Reserved
00 01D9 8000	00 01D9 807F	128	Tracer CFG28	Tracer CFG28	Tracer CFG28
00 01D9 8080	00 01D9 FFFF	32K-128	Reserved	Reserved	Reserved
00 01DA 0000	00 01DA 007F	128	Tracer CFG22	Tracer CFG22	Tracer CFG22
00 01DA 0080	00 01DA 7FFF	32K-128	Reserved	Reserved	Reserved
00 01DA 8000	00 01DA 807F	128	Reserved	Reserved	Reserved
00 01DA 8080	00 01DA FFFF	32K-128	Reserved	Reserved	Reserved
00 01DB 0000	00 01DB 007F	128	Tracer CFG31	Tracer CFG31	Tracer CFG31
00 01DB 0080	00 01DB 7FFF	32K-128	Reserved	Reserved	Reserved
00 01DB 8000	00 01DB 807F	128	Reserved	Reserved	Reserved
00 01DB 8080	00 01DB 8FFF	32K-128	Reserved	Reserved	Reserved
00 01DC 0000	00 01DC 007F	128	Tracer CFG17	Tracer CFG17	Tracer CFG17
00 01DC 0080	00 01DC 7FFF	32K-128	Reserved	Reserved	Reserved
00 01DC 8000	00 01DC 807F	128	Tracer CFG18	Tracer CFG18	Tracer CFG18
00 01DC 8080	00 01DC FFFF	32K-128	Reserved	Reserved	Reserved
00 01DD 0000	00 01DD 007F	128	Tracer CFG19	Tracer CFG19	Tracer CFG19
00 01DD 0080	00 01DD 7FFF	32K-128	Reserved	Reserved	Reserved
00 01DD 8000	00 01DD 807F	128	Tracer CFG4	Tracer CFG4	Tracer CFG4
00 01DD 8080	00 01DD FFFF	32K-128	Reserved	Reserved	Reserved
00 01DE 0000	00 01DE 007F	128	Tracer CFG5	Tracer CFG5	Tracer CFG5
00 01DE 0080	00 01DE 03FF	1K-128	Reserved	Reserved	Reserved
00 01DE 0400	00 01DE 047F	128	Tracer CFG6	Tracer CFG6	Tracer CFG6
00 01DD 0480	00 01DD 07FF	1K-128	Reserved	Reserved	Reserved
00 01DE 0800	00 01DE 087F	128	Tracer CFG7	Tracer CFG7	Tracer CFG7
00 01DE 0880	00 01DE 7FFF	30K-128	Reserved	Reserved	Reserved
00 01DE 8000	00 01DE 807F	128	Tracer CFG24	Tracer CFG24	Tracer CFG24
00 01DE 8080	00 01DF FFFF	64K-128	Reserved	Reserved	Reserved
00 01E0 0000	00 01E3 FFFF	256K	Reserved	Reserved	Reserved
00 01E4 0000	00 01E4 3FFF	16K	Reserved	Reserved	Reserved
00 01E4 4000	00 01E7 FFFF	240k	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 01E8 0000	00 01E8 3FFF	16K	ARM CorePac VBUSP Memory Mapped Registers	ARM CorePac VBUSP Memory Mapped Registers	ARM CorePac VBUSP Memory Mapped Registers
00 01E8 4000	00 01EB FFFF	240k	Reserved	Reserved	Reserved
00 01EC 0000	00 01EF FFFF	256K	Reserved	Reserved	Reserved
00 01F0 0000	00 01F7 FFFF	512K	Reserved	Reserved	Reserved
00 01F8 0000	00 01F8 FFFF	64K	Reserved	Reserved	Reserved
00 01F9 0000	00 01F9 FFFF	64K	Reserved	Reserved	Reserved
00 01FA 0000	00 01FB FFFF	128K	Reserved	Reserved	Reserved
00 01FC 0000	00 01FD FFFF	128K	Reserved	Reserved	Reserved
00 01FE 0000	00 01FF FFFF	128K	Reserved	Reserved	Reserved
00 0200 0000	00 020F FFFF	1M	Reserved	Reserved	Reserved
00 0210 0000	00 0210 FFFF	64K	RAC - FEI configuration	RAC - FEI configuration	RAC - FEI configuration
00 0211 0000	00 0211 FFFF	64K	RAC - BEI configuration	RAC - BEI configuration	RAC - BEI configuration
00 0212 0000	00 0213 FFFF	128K	RAC - GCCP 0 configuration	RAC - GCCP 0 configuration	RAC - GCCP 0 configuration
00 0214 0000	00 0215 FFFF	128K	RAC - GCCP 1 configuration	RAC - GCCP 1 configuration	RAC - GCCP 1 configuration
00 0216 0000	00 0217 FFFF	128K	Reserved	Reserved	Reserved
00 0218 0000	00 0218 7FFF	32k	Reserved	Reserved	Reserved
00 0218 8000	00 0218 FFFF	32k	Reserved	Reserved	Reserved
00 0219 0000	00 0219 FFFF	64k	Reserved	Reserved	Reserved
00 021A 0000	00 021A FFFF	64K	Reserved	Reserved	Reserved
00 021B 0000	00 021B FFFF	64K	Reserved	Reserved	Reserved
00 021C 0000	00 021C 03FF	1K	TCP3d_0 configuration	TCP3d_0 configuration	TCP3d_0 configuration
00 021C 0400	00 021C 3FFF	15K	Reserved	Reserved	Reserved
00 021C 4000	00 021C 43FF	1K	Reserved	Reserved	Reserved
00 021C 4400	00 021C 5FFF	7K	Reserved	Reserved	Reserved
00 021C 6000	00 021C 63FF	1K	Reserved	Reserved	Reserved
00 021C 6400	00 021C 7FFF	7K	Reserved	Reserved	Reserved
00 021C 8000	00 021C 83FF	1K	TCP3d_1 configuration	TCP3d_1 configuration	TCP3d_1 configuration
00 021C 8400	00 021C FFFF	31K	Reserved	Reserved	Reserved
00 021D 0000	00 021D 00FF	256	VCP2_0 configuration	VCP2_0 configuration	VCP2_0 configuration
00 021D 0100	00 021D 3FFF	16K	Reserved	Reserved	Reserved
00 021D 4000	00 021D 40FF	256	VCP2_1 configuration	VCP2_1 configuration	VCP2_1 configuration
00 021D 4100	00 021D 7FFF	16K	Reserved	Reserved	Reserved
00 021D 8000	00 021D 80FF	256	VCP2_2 configuration	VCP2_2 configuration	VCP2_2 configuration
00 021D 8100	00 021D BFFF	16K	Reserved	Reserved	Reserved
00 021D C000	00 021D C0FF	256	VCP2_3 configuration	VCP2_3 configuration	VCP2_3 configuration
00 021D C100	00 021D EFFF	12K-256	Reserved	Reserved	Reserved
00 021D F000	00 021D F07F	128	Reserved	Reserved	Reserved
00 021D F080	00 021D FFFF	4K-128	Reserved	Reserved	Reserved
00 021E 0000	00 021E FFFF	64K	Reserved	Reserved	Reserved
00 021F 0000	00 021F 07FF	2K	FFTC_0 configuration	FFTC_0 configuration	FFTC_0 configuration
00 021F 0800	00 021F 0FFF	2K	Reserved	Reserved	Reserved
00 021F 1000	00 021F 17FF	2K	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 021F 1800	00 021F 3FFF	10K	Reserved	Reserved	Reserved
00 021F 4000	00 021F 47FF	2K	FFTC_1 configuration	FFTC_1 configuration	FFTC_1 configuration
00 021F 4800	00 021F 7FFF	14K	Reserved	Reserved	Reserved
00 021F 8000	00 021F 87FF	Reserved	Reserved	Reserved	Reserved
00 021F 8800	00 021F BFFF	Reserved	Reserved	Reserved	Reserved
00 021F C000	00 021F C7FF	Reserved	Reserved	Reserved	Reserved
00 021F C800	00 021F FFFF	14K	Reserved	Reserved	Reserved
00 0220 0000	00 0220 007F	128	Timer0	Timer0	Timer0
00 0220 0080	00 0220 FFFF	64K-128	Reserved	Reserved	Reserved
00 0221 0000	00 0221 007F	128	Timer1	Timer1	Timer1
00 0221 0080	00 0221 FFFF	64K-128	Reserved	Reserved	Reserved
00 0222 0000	00 0222 007F	128	Timer2	Timer2	Timer2
00 0222 0080	00 0222 FFFF	64K-128	Reserved	Reserved	Reserved
00 0223 0000	00 0223 007F	128	Timer3	Timer3	Timer3
00 0223 0080	00 0223 FFFF	64K-128	Reserved	Reserved	Reserved
00 0224 0000	00 0224 007F	128	Reserved	Reserved	Reserved
00 0224 0080	00 0224 FFFF	64K-128	Reserved	Reserved	Reserved
00 0225 0000	00 0225 007F	128	Reserved	Reserved	Reserved
00 0225 0080	00 0225 FFFF	64K-128	Reserved	Reserved	Reserved
00 0226 0000	00 0226 007F	128	Reserved	Reserved	Reserved
00 0226 0080	00 0226 FFFF	64K-128	Reserved	Reserved	Reserved
00 0227 0000	00 0227 007F	128	Reserved	Reserved	Reserved
00 0227 0080	00 0227 FFFF	64K-128	Reserved	Reserved	Reserved
00 0228 0000	00 0228 007F	128	Timer 8	Timer 8	Timer 8
00 0228 0080	00 0228 FFFF	64K-128	Reserved	Reserved	Reserved
00 0229 0000	00 0229 007F	128	Timer 9	Timer 9	Timer 9
00 0229 0080	00 0229 FFFF	64K-128	Reserved	Reserved	Reserved
00 022A 0000	00 022A 007F	128	Timer 10	Timer 10	Timer 10
00 022A 0080	00 022A FFFF	64K-128	Reserved	Reserved	Reserved
00 022B 0000	00 022B 007F	128	Timer 11	Timer 11	Timer 11
00 022B 0080	00 022B FFFF	64K-128	Reserved	Reserved	Reserved
00 022C 0000	00 022C 007F	128	Timer 12	Timer 12	Timer 12
00 022C 0080	00 022C FFFF	64K-128	Reserved	Reserved	Reserved
00 022D 0000	00 022D 007F	128	Timer 13	Timer 13	Timer 13
00 022D 0080	00 022D FFFF	64K-128	Reserved	Reserved	Reserved
00 022E 0000	00 022E 007F	128	Timer 14	Timer 14	Timer 14
00 022E 0080	00 022E FFFF	64K-128	Reserved	Reserved	Reserved
00 022F 0000	00 022F 007F	128	Timer 15	Timer 15	Timer 15
00 022F 0080	00 022F 00FF	128	Timer 16	Timer 16	Timer 16
00 022F 0100	00 022F 017F	128	Timer 17	Timer 17	Timer 17
00 022F 0180	00 022F 01FF	128	Reserved	Reserved	Reserved
00 022F 0200	00 022F 027F	128	Reserved	Reserved	Reserved
00 0230 0000	00 0230 FFFF	64K	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 0231 0000	00 0231 01FF	512	PLL Controller	PLL Controller	PLL Controller
00 0231 0200	00 0231 9FFF	40K-512	Reserved	Reserved	Reserved
00 0231 A000	00 0231 BFFF	8K	Reserved	Reserved	Reserved
00 0231 C000	00 0231 DFFF	8K	Reserved	Reserved	Reserved
00 0231 E000	00 0231 FFFF	8K	Reserved	Reserved	Reserved
00 0232 0000	00 0232 1FFF	8K	CSISC2 SerDes Config 3	CSISC2 SerDes Config 3	CSISC2 SerDes Config 3
00 0232 2000	00 0232 3FFF	8K	Reserved	Reserved	Reserved
00 0232 4000	00 0232 5FFF	8K	CSISC2 SerDes Config 0	CSISC2 SerDes Config 0	CSISC2 SerDes Config 0
00 02326000	00 0232 7FFF	4K	CSISC2 SerDes Config 1	CSISC2 SerDes Config 1	CSISC2 SerDes Config 1
00 0232 8000	00 0232 8FFF	8K	Reserved	Reserved	Reserved
00 0232 9000	00 0232 9FFF	4K	DDRA PHY Config	DDRA PHY Config	DDRA PHY Config
00 0232 A000	00 0232 BFFF	8K	CSISC2 SerDes Config 2	CSISC2 SerDes Config 2	CSISC2 SerDes Config 2
00 0232 C000	00 0232 CFFF	4K	Reserved	Reserved	Reserved
00 0232 D000	00 0232 DFFF	4K	Reserved	Reserved	Reserved
00 0232 E000	00 0232 EFFF	4K	Reserved	Reserved	Reserved
00 0232 F000	00 0232 FFFF	4K	Reserved	Reserved	Reserved
00 0233 0000	00 0233 03FF	1K	SmartReflex0	SmartReflex0	SmartReflex0
00 0233 0400	00 0233 07FF	1K	Reserved	Reserved	Reserved
00 0233 0400	00 0233 FFFF	62K	Reserved	Reserved	Reserved
00 0234 0000	00 0234 03FF	1K	Memory protection unit (MPU) 15	Memory protection unit (MPU) 15	Memory protection unit (MPU) 15
00 0234 0400	00 0234 07FF	1K	Reserved	Reserved	Reserved
00 0234 0800	00 0234 087F	128	Tracer CFG30	Tracer CFG30	Tracer CFG30
00 0234 0880	00 0234 0BFF	1K-128	Reserved	Reserved	Reserved
00 0234 0C00	00 0234 3FFF	13K	Reserved	Reserved	Reserved
00 0234 4000	00 0234 7FFF	16K	Reserved	Reserved	Reserved
00 0234 8000	00 0234 80FF	256	GPIO1 configuration	GPIO1 configuration	GPIO1 configuration
00 0234 8100	00 0234 83FF	768	Reserved	Reserved	Reserved
00 0234 8400	00 0234 843F	64	UART2 configuration	UART2 configuration	UART2 configuration
00 02348440	00 0234 87FF	1K-64	Reserved	Reserved	Reserved
00 0234 8800	00 0234 883F	64	UART3 configuration	UART3 configuration	UART3 configuration
00 0234 8840	00 0234 8BFF	1K-64	Reserved	Reserved	Reserved
00 0234 8C00	00 0234 8FFF	1K	OSR configuration	OSR configuration	OSR configuration
00 0234 9000	00 0234 FFFF	28K	Reserved	Reserved	Reserved
00 0235 0000	00 0235 0FFF	4K	Power sleep controller (PSC)	Power sleep controller (PSC)	Power sleep controller (PSC)
00 0235 1000	00 0235 FFFF	64K-4K	Reserved	Reserved	Reserved
00 0236 0000	00 0236 03FF	1K	Memory protection unit (MPU) 0	Memory protection unit (MPU) 0	Memory protection unit (MPU) 0
00 0236 0400	00 0236 7FFF	31K	Reserved	Reserved	Reserved
00 0236 8000	00 0236 83FF	1K	Memory protection unit (MPU) 1	Memory protection unit (MPU) 1	Memory protection unit (MPU) 1
00 0236 8400	00 0236 FFFF	31K	Reserved	Reserved	Reserved
00 0237 0000	00 0237 03FF	1K	Memory protection unit (MPU) 2	Memory protection unit (MPU) 2	Memory protection unit (MPU) 2

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 0237 0400	00 0237 7FFF	31K	Reserved	Reserved	Reserved
00 0237 8000	00 0237 83FF	1K	Memory protection unit (MPU) 3	Memory protection unit (MPU) 3	Memory protection unit (MPU) 3
00 0237 8400	00 0237 FFFF	31K	Reserved	Reserved	Reserved
00 0238 0000	00 0238 03FF	1K	Memory protection unit (MPU) 4	Memory protection unit (MPU) 4	Memory protection unit (MPU) 4
00 0238 8000	00 0238 83FF	1K	Memory protection unit (MPU) 5	Memory protection unit (MPU) 5	Memory protection unit (MPU) 5
00 0238 8400	00 0238 87FF	1K	Memory protection unit (MPU) 6	Memory protection unit (MPU) 6	Memory protection unit (MPU) 6
00 0238 8800	00 0238 8BFF	1K	Memory protection unit (MPU) 7	Memory protection unit (MPU) 7	Memory protection unit (MPU) 7
00 0238 8C00	00 0238 8FFF	1K	Memory protection unit (MPU) 8	Memory protection unit (MPU) 8	Memory protection unit (MPU) 8
00 0238 9000	00 0238 93FF	1K	Memory protection unit (MPU) 9	Memory protection unit (MPU) 9	Memory protection unit (MPU) 9
00 0238 9400	00 0238 97FF	1K	Memory protection unit (MPU) 10	Memory protection unit (MPU) 10	Memory protection unit (MPU) 10
00 0238 9800	00 0238 9BFF	1K	Memory protection unit (MPU) 11	Memory protection unit (MPU) 11	Memory protection unit (MPU) 11
00 0238 9C00	00 0238 9FFF	1K	Memory protection unit (MPU) 12	Memory protection unit (MPU) 12	Memory protection unit (MPU) 12
00 0238 A000	00 0238 A3FF	1K	Memory protection unit (MPU) 13	Memory protection unit (MPU) 13	Memory protection unit (MPU) 13
00 0238 A400	00 0238 A7FF	1K	Memory protection unit (MPU) 14	Memory protection unit (MPU) 14	Memory protection unit (MPU) 14
00 0238 A800	00 023F FFFF	471K	Reserved	Reserved	Reserved
00 0240 0000	00 0243 FFFF	256K	Reserved	Reserved	Reserved
00 0244 0000	00 0244 3FFF	16K	DSP trace formatter 0	DSP trace formatter 0	DSP trace formatter 0
00 0244 4000	00 0244 FFFF	48K	Reserved	Reserved	Reserved
00 0245 0000	00 0245 3FFF	16K	DSP trace formatter 1	DSP trace formatter 1	DSP trace formatter 1
00 0245 4000	00 0245 FFFF	48K	Reserved	Reserved	Reserved
00 0246 0000	00 0246 3FFF	16K	DSP trace formatter 2	DSP trace formatter 2	DSP trace formatter 2
00 0246 4000	00 0246 FFFF	48K	Reserved	Reserved	Reserved
00 0247 0000	00 0247 3FFF	16K	DSP trace formatter 3	DSP trace formatter 3	DSP trace formatter 3
00 0247 4000	00 0247 FFFF	48K	Reserved	Reserved	Reserved
00 0248 0000	00 0248 3FFF	16K	Reserved	Reserved	Reserved
00 0248 4000	00 0248 FFFF	48K	Reserved	Reserved	Reserved
00 0249 0000	00 0249 3FFF	16K	Reserved	Reserved	Reserved
00 0249 4000	00 0249 FFFF	48K	Reserved	Reserved	Reserved
00 024A 0000	00 024A 3FFF	16K	Reserved	Reserved	Reserved
00 024A 4000	00 024A FFFF	48K	Reserved	Reserved	Reserved
00 024B 0000	00 024B 3FFF	16K	Reserved	Reserved	Reserved
00 024B 4000	00 024B FFFF	48K	Reserved	Reserved	Reserved
00 024C 0000	00 024C 01FF	512	Reserved	Reserved	Reserved
00 024C 0200	00 024C 03FF	1K-512	Reserved	Reserved	Reserved
00 024C 0400	00 024C 07FF	1K	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 024C 0800	00 024C FFFF	62K	Reserved	Reserved	Reserved
00 024D 0000	00 024F FFFF	192K	Reserved	Reserved	Reserved
00 0250 0000	00 0250 007F	128	Reserved	Reserved	Reserved
00 0250 0080	00 0250 7FFF	32K-128	Reserved	Reserved	Reserved
00 0250 8000	00 0250 FFFF	32K	Reserved	Reserved	Reserved
00 0251 0000	00 0251 FFFF	64K	Reserved	Reserved	Reserved
00 0252 0000	00 0252 03FF	1K	Reserved	Reserved	Reserved
00 0252 0400	00 0252 FFFF	64K-1K	Reserved	Reserved	Reserved
00 0253 0000	00 0253 007F	128	I^2C0	I^2C0	I^2C0
00 0253 0080	00 0253 03FF	1K-128	Reserved	Reserved	Reserved
00 0253 0400	00 0253 047F	128	I^2C1	I^2C1	I^2C1
00 0253 0480	00 0253 07FF	1K-128	Reserved	Reserved	Reserved
00 0253 0800	00 0253 087F	128	I^2C2	I^2C2	I^2C2
00 0253 0880	00 0253 0BFF	1K-128	Reserved	Reserved	Reserved
00 0253 0C00	00 0253 0C3F	64	UART0	UART0	UART0
00 0253 0C40	00 0253 FFFF	1K-64	Reserved	Reserved	Reserved
00 0253 1000	00 0253 103F	64	UART1	UART1	UART1
00 0253 1040	00 0253 FFFF	60K-64	Reserved	Reserved	Reserved
00 0254 0000	00 0255 FFFF	128K	BCP	BCP	BCP
00 0256 0000	00 0257 FFFF	128K	ARM CorePac INTC (GIC400) Memory Mapped Registers	ARM CorePac INTC (GIC400) Memory Mapped Registers	ARM CorePac INTC (GIC400) Memory Mapped Registers
00 0258 0000	00 025B FFFF	256K	TAC	TAC	TAC
00 025C 0000	00 025CFFFF	256K	Reserved	Reserved	Reserved
00 0260 0000	00 0260 1FFF	8K	Secondary interrupt controller (INTC) 0	Secondary interrupt controller (INTC) 0	Secondary interrupt controller (INTC) 0
00 0260 2000	00 0260 3FFF	8K	Reserved	Reserved	Reserved
00 0260 4000	00 0260 5FFF	8K	Reserved	Reserved	Reserved
00 0260 6000	00 0260 7FFF	8K	Reserved	Reserved	Reserved
00 0260 8000	00 0260 9FFF	8K	Secondary interrupt controller (INTC) 2	Secondary interrupt controller (INTC) 2	Secondary interrupt controller (INTC) 2
00 0260 A000	00 0260 BEFF	8K-256	Reserved	Reserved	Reserved
00 0260 BF00	00 0260 BFFF	256	GPIO Config	GPIO Config	GPIO Config
00 0260 C000	00 0261 BFFF	64K	Reserved	Reserved	Reserved
00 0261 C000	00 0261 FFFF	16K	Reserved	Reserved	Reserved
00 0262 0000	00 0262 0FFF	4K	BOOTCFG chip-level registers	BOOTCFG chip-level registers	BOOTCFG chip-level registers
00 0262 1000	00 0262 FFFF	60K	Reserved	Reserved	Reserved
00 0263 0000	00 0263 FFFF	64K	USB PHY Config	USB PHY Config	USB PHY Config
00 0264 0000	00 0264 07FF	2K	Semaphore Config	Semaphore Config	Semaphore Config
00 0264 0800	00 0264 FFFF	62K	Reserved	Reserved	Reserved
00 0265 0000	00 0267 FFFF	192K	Reserved	Reserved	Reserved
00 0268 0000	00 0268 FFFF	512K	USB MMR Config	USB MMR Config	USB MMR Config
00 0270 0000	00 0270 7FFF	32K	EDMA channel controller (TPCC) 0	EDMA channel controller (TPCC) 0	EDMA channel controller (TPCC) 0

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 0270 8000	00 0270 FFFF	32K	Reserved	Reserved	Reserved
00 0271 0000	00 0271 FFFF	64K	Reserved	Reserved	Reserved
00 0272 0000	00 0272 7FFF	32K	EDMA channel controller (TPCC) 1	EDMA channel controller (TPCC) 1	EDMA channel controller (TPCC) 1
00 0272 8000	00 0272 FFFF	32K	Reserved	Reserved	Reserved
00 0273 0000	00 0273 FFFF	64K	Reserved	Reserved	Reserved
00 0274 0000	00 0274 7FFF	32K	EDMA channel controller (TPCC) 2	EDMA channel controller (TPCC) 2	EDMA channel controller (TPCC) 2
00 0274 8000	00 0275 FFFF	96K	Reserved	Reserved	Reserved
00 0276 0000	00 0276 03FF	1K	EDMA TPCC0 transfer controller (TPTC) 0	EDMA TPCC0 transfer controller (TPTC) 0	EDMA TPCC0 transfer controller (TPTC) 0
00 0276 0400	00 0276 7FFF	31K	Reserved	Reserved	Reserved
00 0276 8000	00 0276 83FF	1K	EDMA TPCC0 transfer controller (TPTC) 1	EDMA TPCC0 transfer controller (TPTC) 1	EDMA TPCC0 transfer controller (TPTC) 1
00 0276 8400	00 0276 FFFF	31K	Reserved	Reserved	Reserved
00 0277 0000	00 0277 03FF	1K	EDMA TPCC1 transfer controller (TPTC) 0	EDMA TPCC1 transfer controller (TPTC) 0	EDMA TPCC1 transfer controller (TPTC) 0
00 0277 0400	00 0277 7FFF	31K	Reserved	Reserved	Reserved
00 0277 8000	00 0277 83FF	1K	EDMA TPCC1 transfer controller (TPTC) 1	EDMA TPCC1 transfer controller (TPTC) 1	EDMA TPCC1 transfer controller (TPTC) 1
00 0278 0400	00 0277 FFFF	31K	Reserved	Reserved	Reserved
00 0278 0000	00 0278 03FF	1K	EDMA TPCC1 transfer controller (TPTC) 2	EDMA TPCC1 transfer controller (TPTC) 2	EDMA TPCC1 transfer controller (TPTC) 2
00 0278 0400	00 0278 7FFF	31K	Reserved	Reserved	Reserved
00 0278 8000	00 0278 83FF	1K	EDMA TPCC1 transfer controller (TPTC) 3	EDMA TPCC1 transfer controller (TPTC) 3	EDMA TPCC1 transfer controller (TPTC) 3
00 0278 8400	00 0278 FFFF	31K	Reserved	Reserved	Reserved
00 0279 0000	00 0279 03FF	1K	EDMA TPCC2 transfer controller (TPTC) 0	EDMA TPCC2 transfer controller (TPTC) 0	EDMA TPCC2 transfer controller (TPTC) 0
00 0279 0400	00 0279 7FFF	31K	Reserved	Reserved	Reserved
00 0279 8000	00 0279 83FF	1K	EDMA TPCC2 transfer controller (TPTC) 1	EDMA TPCC2 transfer controller (TPTC) 1	EDMA TPCC2 transfer controller (TPTC) 1
00 0279 8400	00 0279 FFFF	31K	Reserved	Reserved	Reserved
00 027A 0000	00 027A 03FF	1K	EDMA TPCC2 transfer controller (TPTC) 2	EDMA TPCC2 transfer controller (TPTC) 2	EDMA TPCC2 transfer controller (TPTC) 2
00 027A 0400	00 027A 7FFF	31K	Reserved	Reserved	Reserved
00 027A 8000	00 027A 83FF	1K	EDMA TPCC2 transfer controller (TPTC) 3	EDMA TPCC2 transfer controller (TPTC) 3	EDMA TPCC2 transfer controller (TPTC) 3
00 027A 8400	00 027A FFFF	31K	Reserved	Reserved	Reserved
00 027B 0000	00 027B 03FF	1K	Reserved	Reserved	Reserved
00 027B 0400	00 027B 7FFF	31K	Reserved	Reserved	Reserved
00 027B 8000	00 027B 83FF	1K	Reserved	Reserved	Reserved
00 027B 8400	00 027B 87FF	1K	Reserved	Reserved	Reserved
00 027B 8800	00 027B 8BFF	1K	Reserved	Reserved	Reserved
00 027B 8C00	00 027B FFFF	29K	Reserved	Reserved	Reserved
00 027C 0000	00 027C 03FF	1K	Reserved	Reserved	Reserved
00 027C 0400	00 027C FFFF	63K	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 027D 0000	00 027D 3FFF	16K	TI embedded trace buffer (TETB) - CorePac0	TI embedded trace buffer (TETB) - CorePac0	TI embedded trace buffer (TETB) - CorePac0
00 027D 4000	00 027D 7FFF	16K	TBR ARM CorePac - Trace buffer - ARM CorePac	TBR ARM CorePac - Trace buffer - ARM CorePac	TBR ARM CorePac - Trace buffer - ARM CorePac
00 027D 8000	00 027D FFFF	32K	Reserved	Reserved	Reserved
00 027E 0000	00 027E 3FFF	16K	TI embedded trace buffer (TETB) - CorePac1	TI embedded trace buffer (TETB) - CorePac1	TI embedded trace buffer (TETB) - CorePac1
00 027E 4000	00 027E FFFF	48K	Reserved	Reserved	Reserved
00 027F 0000	00 027F 3FFF	16K	TI embedded trace buffer (TETB) - CorePac2	TI embedded trace buffer (TETB) - CorePac2	TI embedded trace buffer (TETB) - CorePac2
00 027F 4000	00 027F FFFF	48K	Reserved	Reserved	Reserved
00 0280 0000	00 0280 3FFF	16K	TI embedded trace buffer (TETB) - CorePac3	TI embedded trace buffer (TETB) - CorePac3	TI embedded trace buffer (TETB) - CorePac3
00 0280 4000	00 0280 FFFF	48K	Reserved	Reserved	Reserved
00 0281 0000	00 0281 3FFF	16K	Reserved	Reserved	Reserved
00 0281 4000	00 0281 FFFF	48K	Reserved	Reserved	Reserved
00 0282 0000	00 0282 3FFF	16K	Reserved	Reserved	Reserved
00 0282 4000	00 0282 FFFF	48K	Reserved	Reserved	Reserved
00 0283 0000	00 0283 3FFF	16K	Reserved	Reserved	Reserved
00 0283 4000	00 0283 FFFF	48K	Reserved	Reserved	Reserved
00 0284 0000	00 0284 3FFF	16K	Reserved	Reserved	Reserved
00 0284 4000	00 0284 FFFF	48K	Reserved	Reserved	Reserved
00 0285 0000	00 0285 7FFF	32K	TBR_SYS-Trace Buffer -System	TBR_SYS-Trace Buffer -System	TBR_SYS-Trace Buffer -System
00 0285 8000	00 0285 FFFF	32K	Reserved	Reserved	Reserved
00 0286 0000	00 028F FFFF	640K	Reserved	Reserved	Reserved
00 0290 0000	00 0293 FFFF	256K	Reserved	Reserved	Reserved
00 0294 0000	00 029F FFFF	768K	Reserved	Reserved	Reserved
00 02A0 0000	00 02AF FFFF	1M	Navigator configuration	Navigator configuration	Navigator configuration
00 02B0 0000	00 02BF FFFF	1M	Navigator linking RAM	Navigator linking RAM	Navigator linking RAM
00 02C0 0000	00 02C0 FFFF	64K	Reserved	Reserved	Reserved
00 02C1 0000	00 02C1 FFFF	64K	Reserved	Reserved	Reserved
00 02C2 0000	00 02C3 FFFF	128K	Reserved	Reserved	Reserved
00 02C4 0000	00 02C5 FFFF	128K	Reserved	Reserved	Reserved
00 02C6 0000	00 02C7 FFFF	128K	Reserved	Reserved	Reserved
00 02C8 0000	00 02C8 FFFF	64K	Reserved	Reserved	Reserved
00 02C9 0000	00 02C9 FFFF	64K	Reserved	Reserved	Reserved
00 02CA 0000	00 02CB FFFF	128K	Reserved	Reserved	Reserved
00 02CC 0000	00 02CD FFFF	128K	Reserved	Reserved	Reserved
00 02CE 0000	00 02EF FFFF	15M-896K	Reserved	Reserved	Reserved
00 02F0 0000	00 02FF FFFF	1M	Reserved	Reserved	Reserved
00 0300 0000	00 030F FFFF	1M	Debug_SS Configuration	Debug_SS Configuration	Debug_SS Configuration
00 0310 0000	00 07FF FFFF	79M	Reserved	Reserved	Reserved
00 0800 0000	00 0801 FFFF	128K	Extended memory controller (XMC) configuration	Extended memory controller (XMC) configuration	Extended memory controller (XMC) configuration

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 0802 0000	00 0BBF FFFF	60M-128K	Reserved	Reserved	Reserved
00 0BC0 0000	00 0BCF FFFF	1M	Multicore shared memory controller (MSMC) config	Multicore shared memory controller (MSMC) config	Multicore shared memory controller (MSMC) config
00 0BD0 0000	00 0BFF FFFF	3M	Reserved	Reserved	Reserved
00 0C00 0000	00 0C1F FFFF	2M	Multicore shared memory (MSM)	Multicore shared memory (MSM)	Multicore shared memory (MSM)
00 0C20 0000	00 0FFF FFFF	62M	Reserved	Reserved	Reserved
00 1000 0000	00 107F FFFF	8M	Reserved	Reserved	Reserved
00 1080 0000	00 108F FFFF	1M	CorePac0 L2 SRAM	CorePac0 L2 SRAM	CorePac0 L2 SRAM
00 1090 0000	00 10DF FFFF	5M	Reserved	Reserved	Reserved
00 10E0 0000	00 10E0 7FFF	32K	CorePac0 L1P SRAM	CorePac0 L1P SRAM	CorePac0 L1P SRAM
00 10E0 8000	00 10EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 10F0 0000	00 10F0 7FFF	32K	CorePac0 L1D SRAM	CorePac0 L1D SRAM	CorePac0 L1D SRAM
00 10F0 8000	00 117F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1180 0000	00 118F FFFF	1M	CorePac1 L2 SRAM	CorePac1 L2 SRAM	CorePac1 L2 SRAM
00 1190 0000	00 11DF FFFF	5M	Reserved	Reserved	Reserved
00 11E0 0000	00 11E0 7FFF	32K	CorePac1 L1P SRAM	CorePac1 L1P SRAM	CorePac1 L1P SRAM
00 11E0 8000	00 11EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 11F0 0000	00 11F0 7FFF	32K	CorePac1 L1D SRAM	CorePac1 L1D SRAM	CorePac1 L1D SRAM
00 11F0 8000	00 127F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1280 0000	00 128F FFFF	1M	CorePac2 L2 SRAM	CorePac2 L2 SRAM	CorePac2 L2 SRAM
00 1290 0000	00 12DF FFFF	5M	Reserved	Reserved	Reserved
00 12E0 0000	00 12E0 7FFF	32K	CorePac2 L1P SRAM	CorePac2 L1P SRAM	CorePac2 L1P SRAM
00 12E0 8000	00 12EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 12F0 0000	00 12F0 7FFF	32K	CorePac2 L1D SRAM	CorePac2 L1D SRAM	CorePac2 L1D SRAM
00 12F0 8000	00 137F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1380 0000	00 1388 FFFF	1M	CorePac3 L2 SRAM	CorePac3 L2 SRAM	CorePac3 L2 SRAM
00 1390 0000	00 13DF FFFF	5M	Reserved	Reserved	Reserved
00 13E0 0000	00 13E0 7FFF	32K	CorePac3 L1P SRAM	CorePac3 L1P SRAM	CorePac3 L1P SRAM
00 13E0 8000	00 13EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 13F0 0000	00 13F0 7FFF	32K	CorePac3 L1D SRAM	CorePac3 L1D SRAM	CorePac3 L1D SRAM
00 13F0 8000	00 147F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1480 0000	00 148F FFFF	1M	Reserved	Reserved	Reserved
00 1490 0000	00 14DF FFFF	5M	Reserved	Reserved	Reserved
00 14E0 0000	00 14E0 7FFF	32K	Reserved	Reserved	Reserved
00 14E0 8000	00 14EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 14F0 0000	00 14F0 7FFF	32K	Reserved	Reserved	Reserved
00 14F0 8000	00 157F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1580 0000	00 158F FFFF	1M	Reserved	Reserved	Reserved
00 1590 0000	00 15DF FFFF	5M	Reserved	Reserved	Reserved
00 15E0 0000	00 15E0 7FFF	32K	Reserved	Reserved	Reserved
00 15E0 8000	00 15EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 15F0 0000	00 15F0 7FFF	32K	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 15F0 8000	00 167F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1680 0000	00 168F FFFF	1M	Reserved	Reserved	Reserved
00 1690 0000	00 16DF FFFF	5M	Reserved	Reserved	Reserved
00 16E0 0000	00 16E0 7FFF	32K	Reserved	Reserved	Reserved
00 16E0 8000	00 16EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 16F0 0000	00 16F0 7FFF	32K	Reserved	Reserved	Reserved
00 16F0 8000	00 177F FFFF	9M-32K	Reserved	Reserved	Reserved
00 1780 0000	00 178F FFFF	1M	Reserved	Reserved	Reserved
00 1790 0000	00 17DF FFFF	5M	Reserved	Reserved	Reserved
00 17E0 0000	00 17E0 7FFF	32K	Reserved	Reserved	Reserved
00 17E0 8000	00 17EF FFFF	1M-32K	Reserved	Reserved	Reserved
00 17F0 0000	00 17F0 7FFF	32K	Reserved	Reserved	Reserved
00 17F0 8000	00 1FFF FFFF	129M-32K	Reserved	Reserved	Reserved
00 2000 0000	00 200F FFFF	1M	System trace manager (STM) configuration	System trace manager (STM) configuration	System trace manager (STM) configuration
00 2010 0000	00 201F FFFF	1M	Reserved	Reserved	Reserved
00 2020 0000	00 205F FFFF	4M	Reserved	Reserved	Reserved
00 2060 0000	00 206F FFFF	1M	TCP3d_1 data	TCP3d_1 data	TCP3d_1 data
00 2070 0000	00 207F FFFF	1M	Reserved	Reserved	Reserved
00 2080 0000	00 208F FFFF	1M	TCP3d_0 data	TCP3d_0 data	TCP3d_0 data
00 2090 0000	00 209F FFFF	1M	Reserved	Reserved	Reserved
00 20A0 0000	00 20A3 FFFF	256K	Reserved	Reserved	Reserved
00 20A4 0000	00 20A4 FFFF	64K	Reserved	Reserved	Reserved
00 20A5 0000	00 20AF FFFF	704K	Reserved	Reserved	Reserved
00 20B0 0000	00 20B3 FFFF	256K	Boot ROM	Boot ROM	Boot ROM
00 20B4 0000	00 20BE FFFF	704K	Reserved	Reserved	Reserved
00 20BF 0000	00 20BF 01FF	64K	Reserved	Reserved	Reserved
00 20C0 0000	00 20FF FFFF	4M	Reserved	Reserved	Reserved
00 2100 0000	00 2100 03FF	1K	Reserved	Reserved	Reserved
00 2100 0400	00 2100 05FF	512	SPI0	SPI0	SPI0
00 2100 0600	00 2100 07FF	512	SPI1	SPI1	SPI1
00 2100 0800	00 2100 09FF	512	SPI2	SPI2	SPI2
00 2100 0A00	00 2100 0AFF	256	AEMIF Config	AEMIF Config	AEMIF Config
00 2100 0B00	00 2100 FFFF	62K-768	Reserved	Reserved	Reserved
00 2101 0000	00 2101 01FF	512	DDR3A EMIF Config	Reserved	DDR3A EMIF Config
00 2101 0200	00 2101 07FF	2K-512	Reserved	Reserved	Reserved
00 2101 0800	00 2101 09FF	512	Reserved	Reserved	Reserved
00 2101 0A00	00 2101 0FFF	2K-512	Reserved	Reserved	Reserved
00 2101 1000	00 2101 FFFF	60K	Reserved	Reserved	Reserved
00 2102 0000	00 2102 7FFF	32K	PCIe1 config	PCIe1 config	PCIe1 config
00 2102 8000	00 217F FFFF	4M-192K	Reserved	Reserved	Reserved
00 2140 0000	00 2140 00FF	256	Reserved	Reserved	Reserved
00 2140 0100	00 2140 01FF	256	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
00 2140 0400	00 217F FFFF	4M-512	Reserved	Reserved	Reserved
00 2180 0000	00 2180 7FFF	32K	PCIe0 config	PCIe0 config	PCIe0 config
00 2180 8000	00 21BF FFFF	4M-32K	Reserved	Reserved	Reserved
00 21C0 0000	00 21FF FFFF	4M	Reserved	Reserved	Reserved
00 2200 0000	00 229F FFFF	10M	Reserved	Reserved	Reserved
00 22A0 0000	00 22A0 FFFF	64K	VCP2_0 Data	VCP2_0 Data	VCP2_0 Data
00 22A1 0000	00 22AF FFFF	1M-64K	Reserved	Reserved	Reserved
00 22B0 0000	00 22B0 FFFF	64K	VCP2_1 Data	VCP2_1 Data	VCP2_1 Data
00 22B1 0000	00 22BF FFFF	1M-64K	Reserved	Reserved	Reserved
00 22C0 0000	00 22C0 FFFF	64K	VCP2_2 Data	VCP2_2 Data	VCP2_2 Data
00 22C1 0000	00 22CF FFFF	1M-64K	Reserved	Reserved	Reserved
00 22D0 0000	00 22D0 FFFF	64K	VCP2_3 Data	VCP2_3 Data	VCP2_3 Data
00 22D1 0000	00 22DF FFFF	1M-64K	Reserved	Reserved	Reserved
00 22E0 0000	00 22E0 FFFF	64K	Reserved	Reserved	Reserved
00 22E1 0000	00 22EF FFFF	1M-64K	Reserved	Reserved	Reserved
00 22F0 0000	00 22F0 FFFF	64K	Reserved	Reserved	Reserved
00 22F1 0000	00 22FF FFFF	1M-64K	Reserved	Reserved	Reserved
00 2300 0000	00 2300 FFFF	64K	Reserved	Reserved	Reserved
00 2301 0000	00 230F FFFF	1M-64K	Reserved	Reserved	Reserved
00 2310 0000	00 2310 FFFF	64K	Reserved	Reserved	Reserved
00 2311 0000	00 231F FFFF	1M-64K	Reserved	Reserved	Reserved
00 2320 0000	00 2323 FFFF	256K	TAC BEI	TAC BEI	TAC BEI
00 2324 0000	00 239F FFFF	8M-256K	Reserved	Reserved	Reserved
00 23A0 0000	00 23BF FFFF	2M	Navigator	Navigator	Navigator
00 23C0 0000	00 23CF FFFF	1M	Reserved	Reserved	Reserved
00 23D0 0000	00 23FF FFFF	3M	Reserved	Reserved	Reserved
00 2400 0000	00 25FF FFFF	32M	DFE configuration	DFE configuration	DFE configuration
00 2600 0000	00 26FF FFFF	16M	NetCP configuration	NetCP configuration	NetCP configuration
00 2700 0000	00 273 F FFFF	4M	IQNet configuration	IQNet configuration	IQNet configuration
00 274 0000	00 2FFF FFFF	140M	Reserved	Reserved	Reserved
00 3000 0000	00 33FF FFFF	64M	EMIF16 CE0	EMIF16 CE0	EMIF16 CE0
00 3400 0000	00 37FF FFFF	64M	EMIF16 CE1	EMIF16 CE1	EMIF16 CE1
00 3800 0000	00 3BFF FFFF	64M	EMIF16 CE2	EMIF16 CE2	EMIF16 CE2
00 3C00 0000	00 3FFF FFFF	64M	EMIF16 CE3	EMIF16 CE3	EMIF16 CE3
00 4000 0000	00 4FFF FFFF	256M	Reserved	Reserved	Reserved
00 5000 0000	00 5FFF FFFF	256M	PCIe 0 data	PCIe 0 data	PCIe 0 data
006000 0000	00 6FFF FFFF	256M	PCIe 1 data	PCIe 1 data	PCIe 1 data
00 7000 0000	00 700F FFFF	1M	OSR data	OSR data	OSR data
00 7010 0000	00 7FFF FFFF	255M	Reserved	Reserved	Reserved
00 8000 0000	00 FFFF FFFF	2G	DDR3A data	DDR3A data	DDR3A data
01 0000 0000	01 2100 FFFF	528M+64K	Reserved	Reserved	Reserved
01 2101 0000	01 2101 01FF	512	DDR3A EMIF configuration (1)	DDR3A EMIF configuration (2)	DDR3A EMIF configuration (3)
01 2101 0200	07 FFFF FFFF	32G-512	Reserved	Reserved	Reserved

Physical 40 bit Address		Bytes	ARM View	DSP View	SOC View
Start	End				
08 0000 0000	09 FFFF FFFF	8G	DDR3A data	DDR3A data (2)	DDR3A data (3)
0A 0000 0000	FF FFFF FFFF	984G	Reserved	Reserved	Reserved

2.2 EVM Boot mode and Boot Configuration Switch Settings

The EVM has one configuration DIP switch (SW1) that can set up to 16 different pre-defined configurations to the BMC. Each DIP configuration results in the BMC latching in a different boot mode when the SoC RESETFULL reset signal is de-asserted. This occurs when power is applied the board, after the user presses the MCU_RESET push button or after a POR reset is requested from the MMC.

SW1 determines general DSP configuration, Little or Big Endian mode as well as boot mode selection.

Please refer to Section 3.3 of this document for default switch setting and details of each switch. For more information on DSP supported Bootmode, refer SoC Data Manual and C66x Boot Loader User Guide.

2.3 Board Revision ID

Board PCB (Printed Circuit Board) and PCA (Printed Circuit Assembly) revision are located below FMC Connector in bottom silk, as shown in Figure 2.1. Table 3 describes the PCA/PCB revisions.

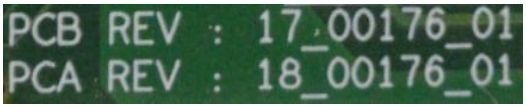


Figure 2.1: EVM Board Revision

Table 2.2: PCA/PCB revision description

Kit Revision	PCA Rev	PCB Rev	Description
1.0.1.1	18_00176_01	17_00176_01	Proto (Initial Engineering Samples) + Alpha Build

Note: Last two digits represent major PCB / PCA revision number.

2.4 JTAG - Emulation Overview

TCIEVMK2LX Evaluation Module (EVM) has on-board embedded XDS200 JTAG emulation circuitry; hence user does not require any external emulator to connect EVM with Code Composer Studio. User can connect CCS with target DSP in EVM through USB cable supplied along with this board. The EVM supports two different types of DSP Emulation - “USB mini-B” and “60-pin TI JTAG-DSP”. USB emulation is supported through an on-board, optimized XDS200 emulation circuit.

In case user wishes to connect external emulator to EVM, the TI 60-pin JTAG header (EMU1) is provided on-board for high speed real-time emulation. The TI 60-pin JTAG supports all standard (XDS510 or XDS560 or XDS200) TI DSP emulators. Please refer to the documentation supplied with your emulator for connection assistance.

On-board embedded JTAG emulator is the default connection to DSP, however when external emulator is connected to EVM, board circuitry switches automatically to give DSP’s emulation access to external emulator. When on-board emulator and external emulator both are connected at the same time, external emulator has priority and on-board emulator is disconnected from DSP.

SoC can also be accessed through the JTAG port on the AMC edge connector. When both the emulators (i.e. on board XDS200 and external emulator) are not present then AMC backplane JTAG takes priority and hence SoC can be accessed through it.

The JTAG interface among the SoC, on-board emulator, external emulator and the AMC edge connector is shown in the below figure.

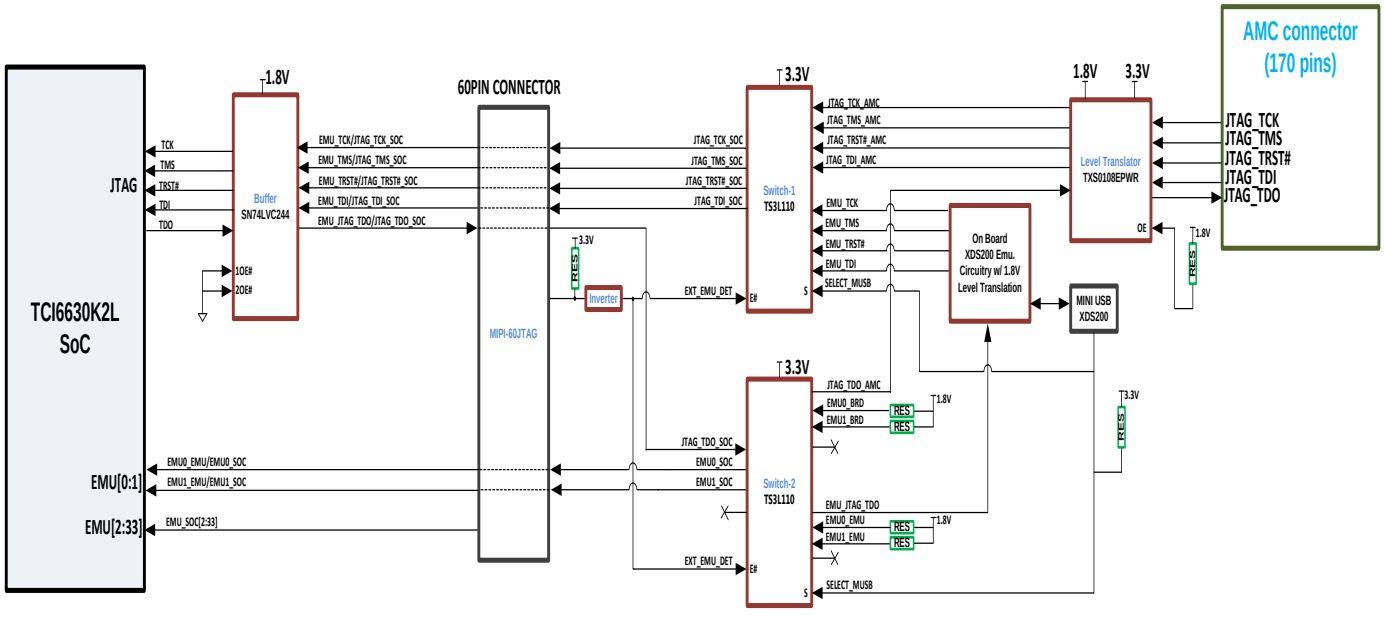


Figure 2.2: TCIEVMK2LX Evaluation Module JTAG emulation

2.5 Clock Domains

The TCIEVMK2LX Evaluation Module (EVM) incorporates variety of clocks to the TCI6630K2L as well as other devices which are configured automatically during the power up configuration sequence by microcontroller. The figure below illustrates the clocking for the system in EVM module.

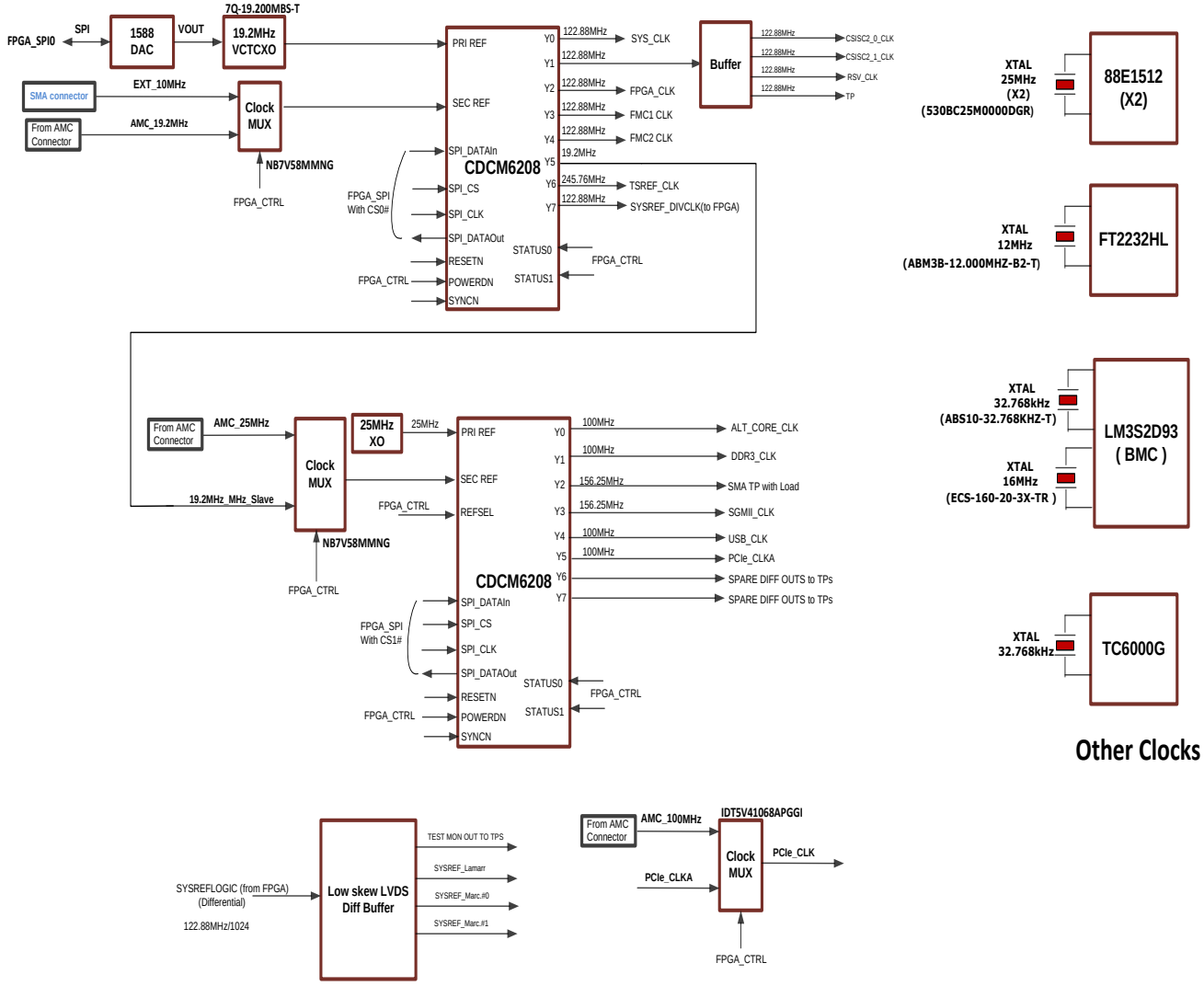


Figure 2.3: TCIEVMK2LX EVM Clock Domains

Table 2.3: Clock Configuration

Clock	Frequency	Description
ALT_CORE_CLK	100.00MHz	Core Clock Input for SoC (Differential)
DDR3_CLK	100.00MHz	DDR3 Clock Input for SoC (Differential)
SGMII_CLK	156.25MHz	SGMII Clock Input for SoC (Differential)
USB_CLK	100.00MHz	USB Clock Input for DSP (Differential)
PCIe_CLKA	100.00MHz	PCIe Clock Input for DSP (Differential)
SYS_CLK	122.88MHz	System Clock Input for SoC (Differential)
CSISC2_0_CLK	122.88MHz	SerDes Clock Input for SoC (Differential)

CSISC2_1_CLK	122.88MHz	SerDes Clock Input for SoC (Differential)
TSREF_CLK	245.76MHz	TSREF Clock Input for SoC (Differential)
FPGA_CLK	122.88MHz	Clock input for FPGA (Differential)
FMC#1 CLK	122.88MHz	FMC1 Clock input to AFE7500EVM (Differential)
FMC#2 CLK	122.88MHz	FMC2 Clock input to AFE7500EVM (Differential)
RSV_CLK+/-	122.88MHz	RSV_CLK Clock input to Expansion Connector (Differential)
SYSREF_Lamarr	120KHz	DFESYSREF Clock input to SoC (Differential)
SYSREF_Marc.#0	120KHz	FMC1 Reference Clock input to AFE7500EVM (LVPECL)
SYSREF_Marc.#1	120KHz	FMC2 Reference Clock input to AFE7500EVM (LVPECL)
EXT_10MHz	10MHz	External Clock input to EVM
TCLKD	19.2MHz	AMC Clock input to EVM
TCLKB	25MHz	AMC Clock input to EVM
FCLKA	100MHz	AMC Clock input to EVM

2.6 I2C Boot EEPROM / SPI NOR Flash

The I2C modules on the TCIEVMK2LX EVM may be used by the DSP to control local peripheral ICs (DACs, ADCs, etc.) or may be used to communicate with other controllers in a system or to implement a user interface.

The I2C bus is connected to one EEPROM and to the 80-pin expansion header (TEST_PH1). There are two banks in the I2C EEPROM which respond separately at addresses 0x50 and 0x51.

The Serial Peripheral Interconnect (SPI) module provides an interface between the DSP and other SPI-compliant devices. The primary intent of this interface is to allow for connection to a SPI ROM for boot. The SPI module on TCI6630K2L is supported only in Master mode.

32MB NOR FLASH (part number N25Q032A11 from NUMONYX) is attached to CS0z on TCI6630K2L. It can contain U-Boot. By default NOR flash contains U-Boot.

.

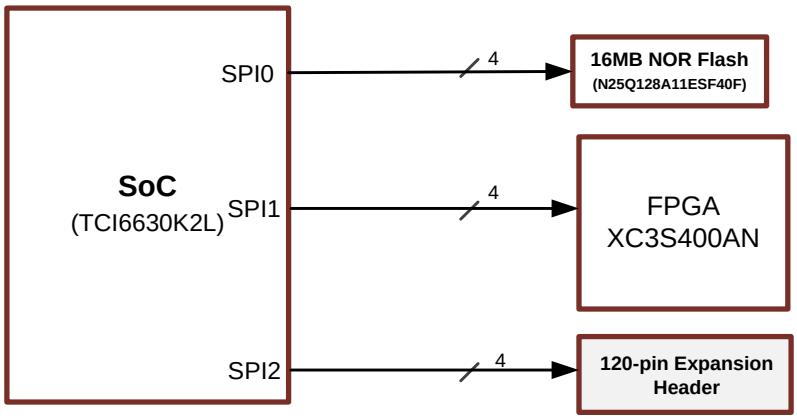


Figure 2.4: TCIEVMK2LX Evaluation Module (EVM) Bus Diagram

2.7 FPGA

The FPGA device (Xilinx XC3S400AN) on TCIEVMK2LX provides complete glue logic for controlling two AFE7500EVM card using two FMC connectors respectively. TCI6630K2L SoC can also access AFE7500 chip of both the cards using SPI expansion logic. The TCI6630K2L SoC's GPIO and DFE GPIO are mapped to AFE7500 GPIO and some of its control signal in side FPGA.

Apart from AFE7500EVM Glue logic signals, FPGA also provides GPIO expander logic, timer logic etc. The GPIOs are accessible to Board Management Controller (BMC) through SPI bus using configuration registers. Refer section 5 for more detailed explanation about FPGA functionality and it's registers.

FPGA uses onboard generated clock with 122.88MHz frequency for its primary operations.

The figure below shows the interface between SoC, FPGA and FMC connectors.

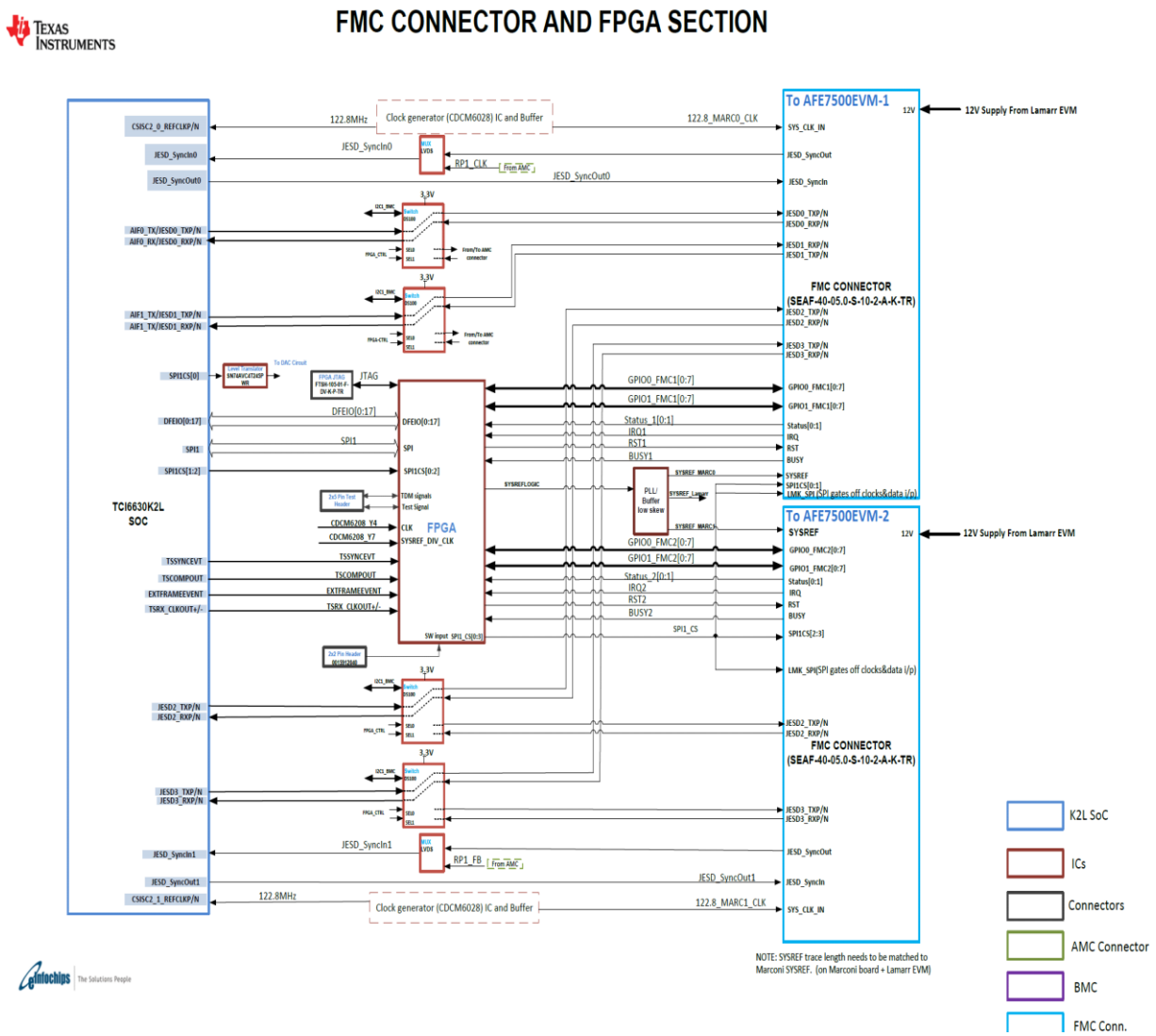


Figure 2.5: TCIEVMK2LX FPGA FMC Interface

The figure below shows the GPIO Expander logic accessed by BMC.

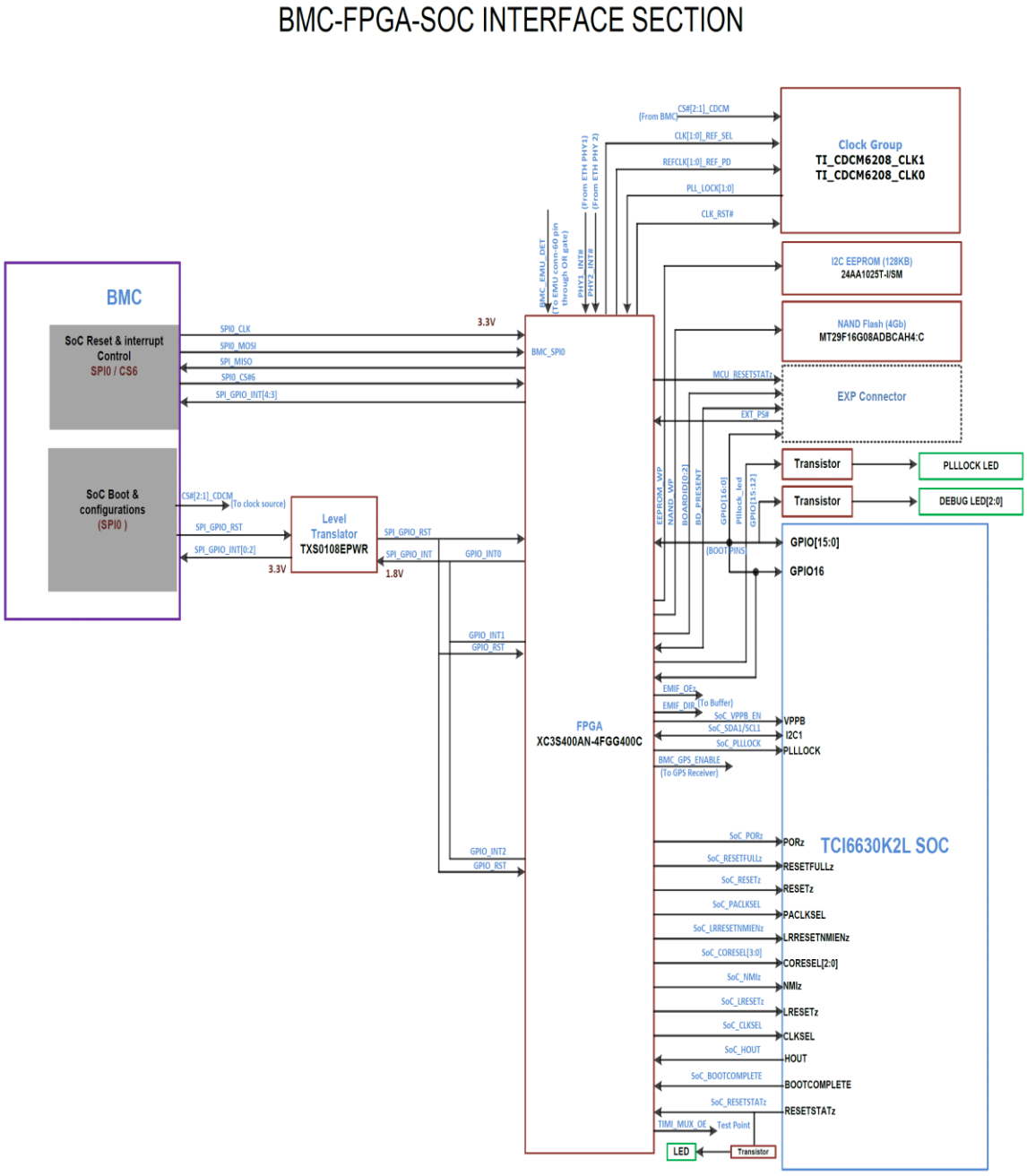


Figure 2.6: TCIEVMK2LX BMC Expander Logic

2.8 Ethernet Switch

The TCIEVMK2LX EVM supports two Ethernet port over two Gigabit RJ-45 connectors (Copper interface) and two SGMII port over two SGMII port of AMC connectors respectively. SGMII0 and SGMII1 of TCI6630K2L go to two separate 88E1512 chips which are connected to dual RJ-45 connector. SGMII2 and SGMII3 (which are muxed internally with PCIe in SoC) of TCI6630K2L go to AMC connector through SERDES switch. The data rate supported by each SGMII port is 1.25Gbps.

The figure below shows the interface between the SoC with Ethernet PHYs and AMC connector:

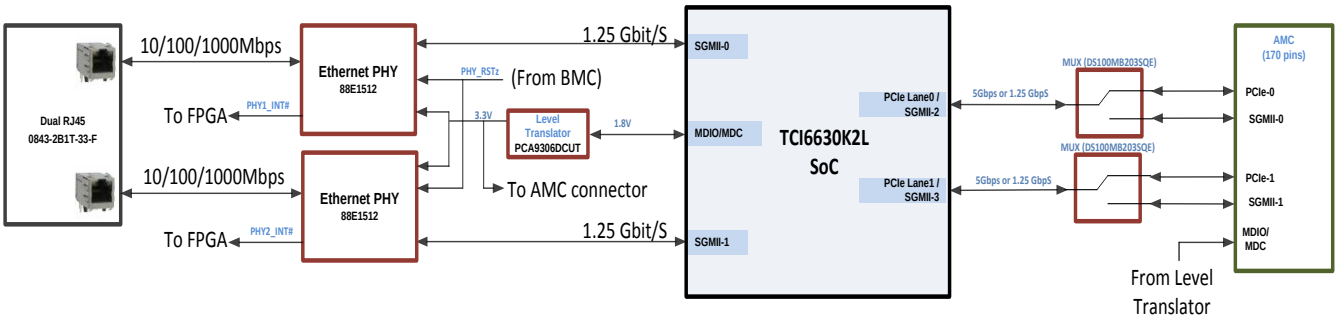


Figure 2.7: TCIEVMK2LX EVM Ethernet PHY Routing

2.9 DDR3 External Memory Interface

The TCIEVMK2LX EVM DDR3 interface connects to four 4Gbit (256Meg x 16) DDR3 1600 devices. TCI6630K2L Soc supports 64bit DDR3 interface. This configuration allows the use of “narrow (16-bit)”, “normal (32-bit)” and “wide (64-bit)” modes of the DDR3 interface. Micron DDR3 MT41K256M16HA125:E SDRAMs (256Mx16; 800MHz) chips are used. Please note that the default total size of DDR3 memory installed is 2GByte and it supports expansion up to 4GByte. For more information, see DDR3 Memory Controller for KeyStone Devices User Guide.

The figure below shows the implementation for the DDR3 SDRAM memory.

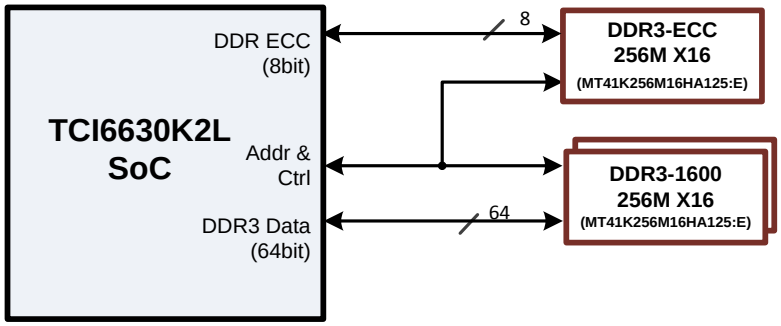


Figure 2.8: TCIEVMK2LX EVM DDR3 Interface

2.10 16-bit Asynchronous External Memory Interface (EMIF-16)

The TCIEVMK2LX EVM EMIF-16 interface connects to one 16Gbit (2GB) NAND flash device. It also connects to 120-pin expansion header (CN2) through sets of buffer. The EMIF16 module provides an interface between SoC and asynchronous external memories such as NAND and NOR flash. Micron MT29F16G08ADBCAH4:C device is used on board. For more information, see External Memory Interface (EMIF16) for KeyStone Devices User Guide.

The figure below shows the EMIF-16 connections.

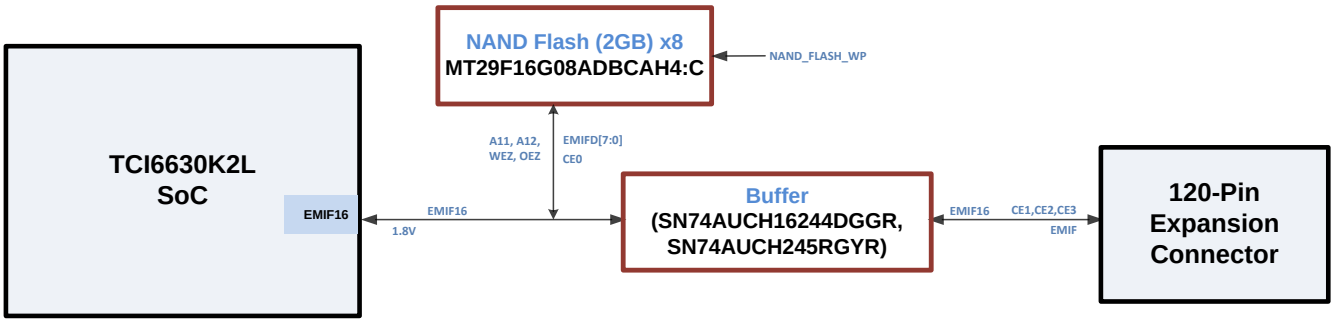


Figure 2.9: TCIEVMK2LX EVM EMIF16 Interface

2.11 AFE7500EVM Card Interface

The TCIEVMK2LX EVM supports two FMC connectors (CN16 and CN17) for two AFE7500EVM card interfaces. TCI6630K2L SoC communicates with both the AFE7500EVM card through FPGA. Please refer “2.7 FPGA” section for detailed FMC Glue logic. TCI6630K2L SoC can configure AFE7500EVM clock chip (i.e. LMK04828) and generates required clock for it. CDCM6207 clock generator chip on TCIEVMK2LX EVM provides SYSCLK (i.e 122.88MHz) clock for both the AFE7500EVM cards where as FPGA provides SYSREF signal to both the card. There is also provision of 12V/1.5A supply to each AFE7500EVM card from TCIEVMK2LX EVM. FMC1 interface contains four high speed JESD lanes (JESD0-JESD3) where as FMC2 contains two high speed JESD lanes (JESD2-JESD3). Each JESD lane provides high-speed data transfer at the rate of 7.3728Gbps per lane on the serial links.

The figure below shows FMC interface connections in TCIEVMK2LX EVM.

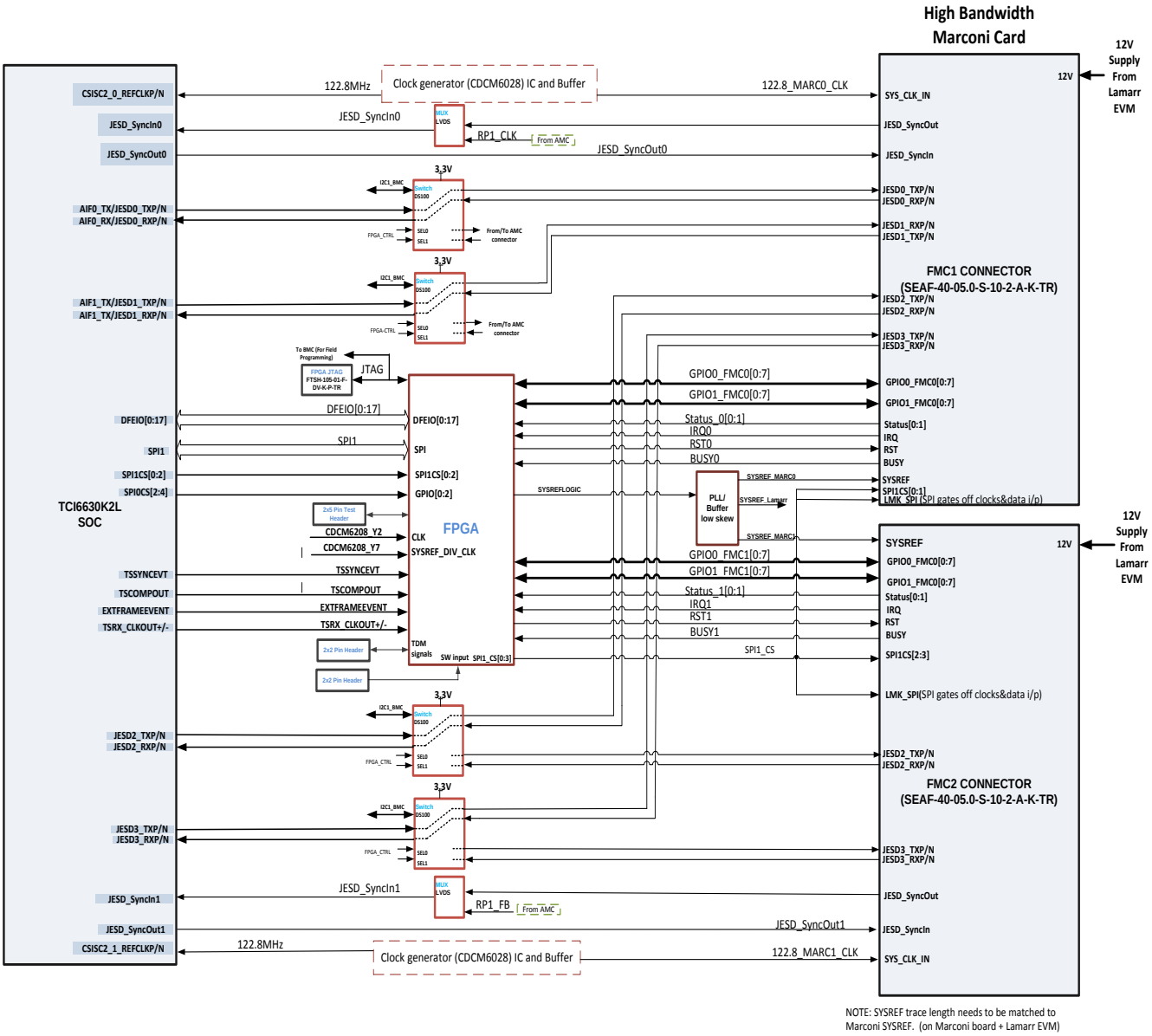


Figure 2.10: TCIEVMK2LX EVM AFE7500EVM Card Interfaces

2.12 PCIe Interface

The 2 lane PCI express (PCIe) interface on TCIEVMK2LX EVM provides a connection between the SoC and AMC edge connector through SERDES multiplexer. The PCI Express interface provides low pin count, high reliability, and high-speed data transfer at rates of 5.0 Gbps per lane on the serial links. For more information, see the Peripheral Component Interconnect Express (PCIe) for KeyStone Devices User Guide.

The figure below shows the PCIe connectivity to AMC backplane on EVM.

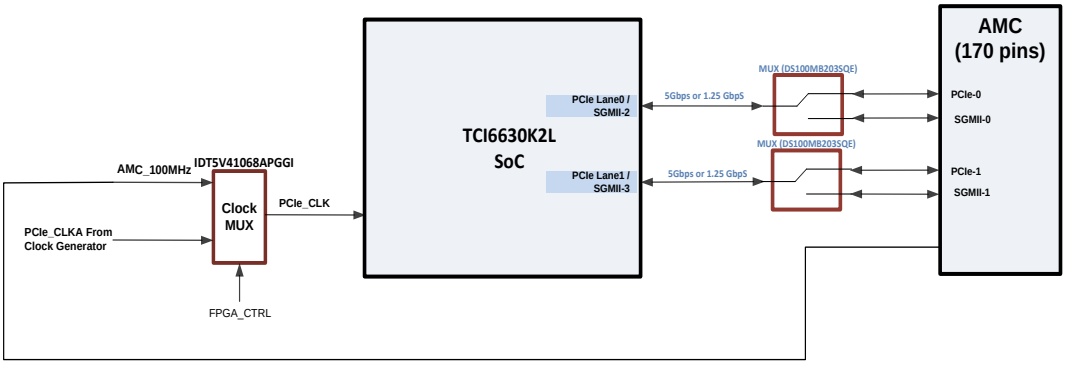


Figure 2.11: TCIEVMK2LX EVM PCIe Interface

2.13 Antenna Interface (AIL)

The AIL interface is responsible for transporting baseband antenna streams over two-lane SerDes-based Antenna Interface Link (AIL) between SoC and AMC edge connector. For more information, see the KeyStone II Architecture IQNet2 User Guide (literature number SPRUH06).

The two-lane SerDes-Baded AIL interface on EVM provides a connection between SoC and AMC edge connector through SerDes multiplexer. The AIL interface provides high-speed data transfer at the rate of 9.83 Gbps per lane on the serial links.

The figure 2.12 illustrates the AIL connections on the EVM.

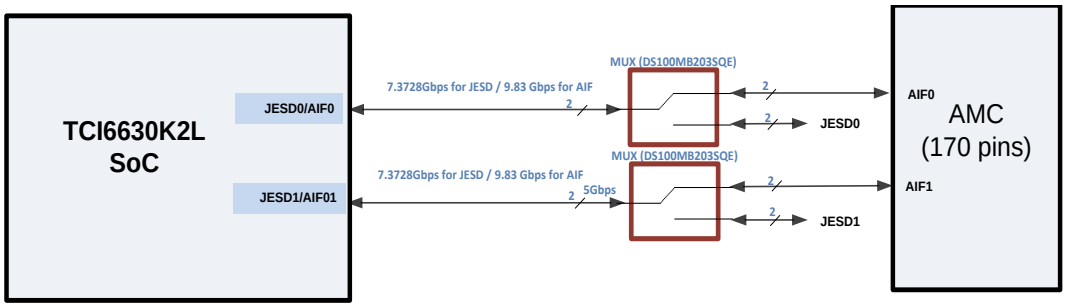


Figure 2.12: TCIEVMK2LX EVM AIL Interface

2.14 UART Interface

The TCI6630K2L supports two UART port. UART0 can be accessed either through mini USB connecter or 4-pin header. The selection is made through detect signal on 4-pin header. UART0 TX single line is also connected to RX line of BMC UART. UART1 port is connected to 120-pin Expansion connector and GPS module.

The LM3S2D93 BMC UART is connected to same mini USB connector and another 4-pin header. The selection is made through detect signal on 4-pin header.

Below figure shows the UART connection of TCIEVMK2LX Evaluation Module.

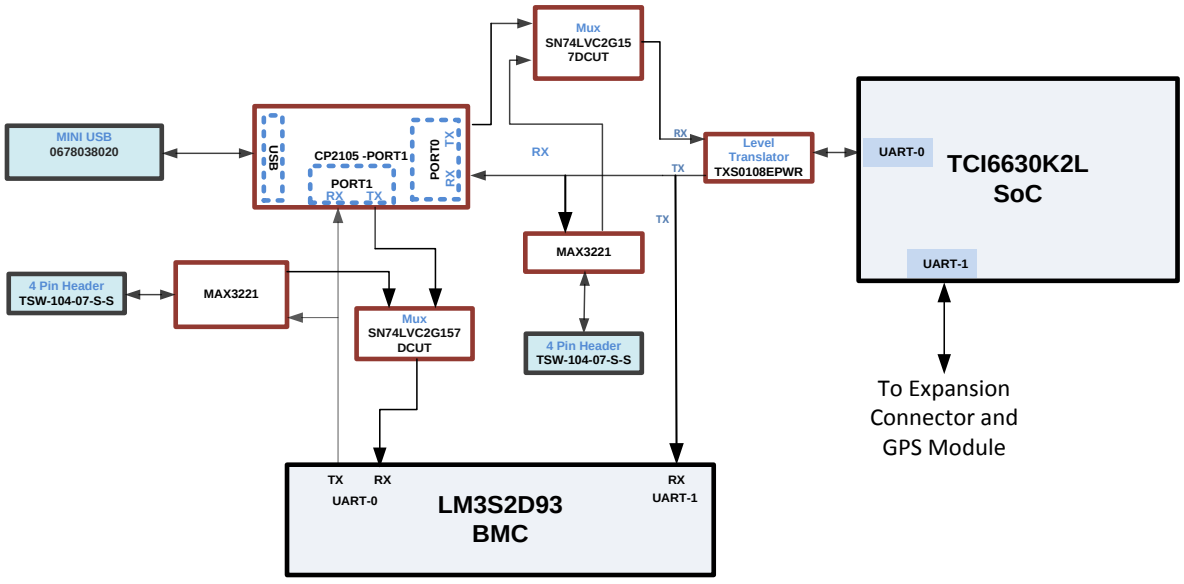


Figure 2.13: TCIEVMK2LX EVM UART Connections

2.15 Board Management Controller (BMC)

The MCU (TI's LMS2D93) controls reset mechanism of the SoC, initiates board power sequence through UCD9090, configures Clock chips (two CDCM6208) and provides boot mode & boot configuration data to the SoC through SW1. MCU also provides the transformation of TDM Frame Sync and Clock between AMC connector and the SoC. The MCU also supports 3 user LEDs and 1 user switch through control registers. All MCU registers are accessible over the SPI interface.

The EVM also supports a limited set of Intelligent Platform Management Interface (IPMI) commands using Microcontroller based on Texas Instruments LMS2D93.

The MCU will communicate with MicroTCA Carrier Hub (MCH) over IPMB (Intelligent Platform Management Bus) when inserted into an AMC slot of a PICMG® MTCA.0 R1.0 compliant chassis. The primary purpose of the MCU is to provide necessary information to MCH, to enable the payload power to EVM EVM when it is inserted into the MicroTCA chassis.

The EVM also supports a Blue LED (D5) and Red LED(D3) on the front panel as specified in PICMG® AMC.0 R2.0 AdvancedMC base specification. Both of these LEDs will blink as part of initialization process when the MCU will receive management power.

Blue LED (D5):

Blue LED will turn ON when MicroTCA chassis is powered ON and an EVM is inserted into it. The blue LED will turn OFF when payload power is enabled to the EVM by the MCH.

Red LED (D3):

Red colored D3 will normally be OFF. It will turn ON to provide basic feedback about failures and out of service.

The figure below shows the interface between SoC and MCU.

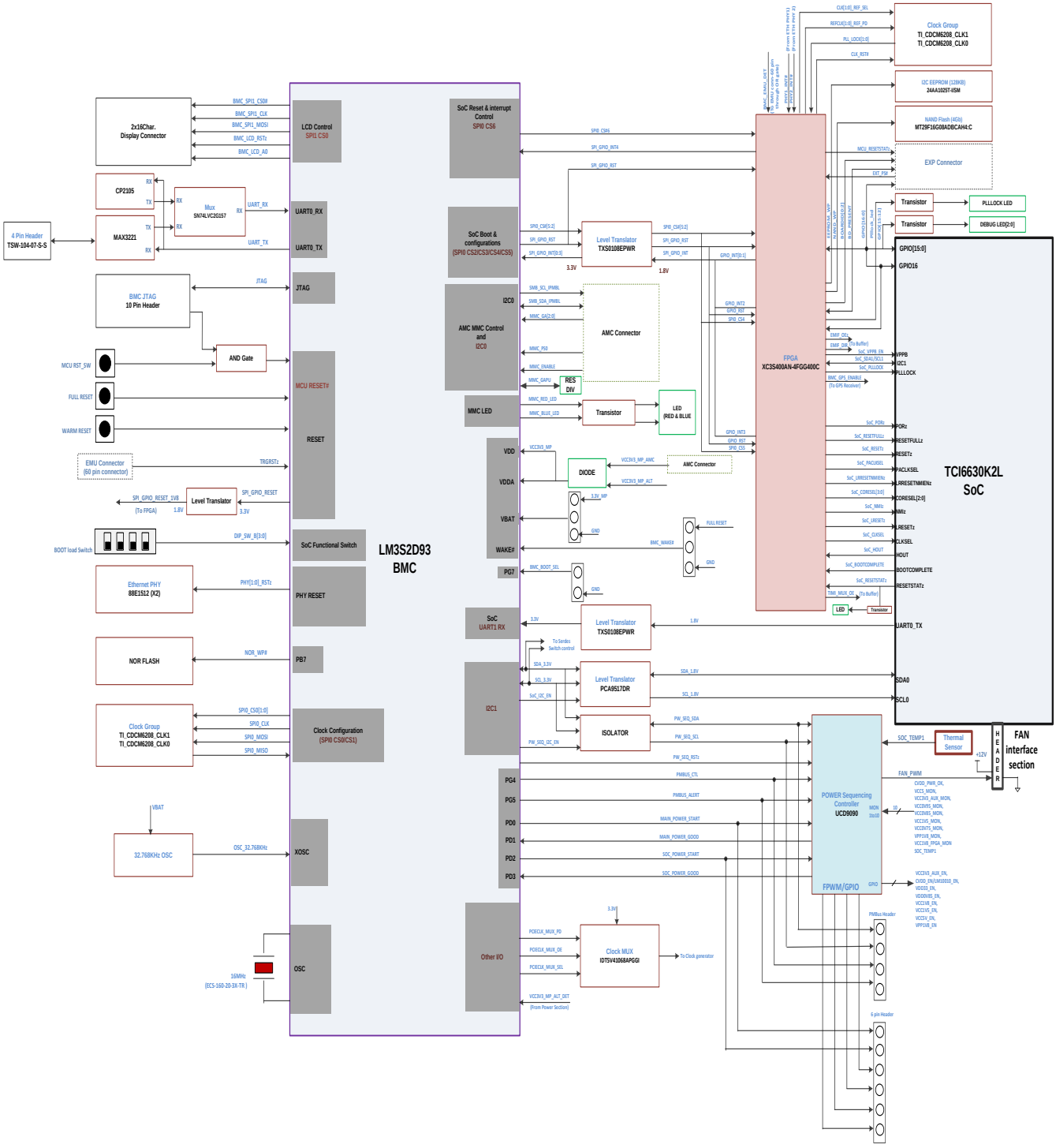


Figure 2.14: TCIEVMK2LX EVM BMC Connections Diagram

2.16 USB3.0 Interface

There is one host USB ports available in TCI6630K2L SoC . This USB port is routed to on board USB3.0 connector and supports data transfer at the rate of 5.0 Gbps on serial links. For more information, see the Universal Serial Bus 3 (USB3) for KeyStone II Devices User Guide (literature number SPRUHJ7).

Below figure shows USB connections between the SoC and USB3.0 connector.

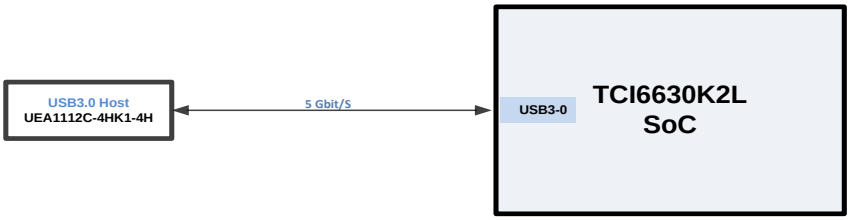


Figure 2.15: TCIEVMK2LX EVM USB3.0 Connection Diagram

2.17 Expansion Header

The TCIEVMK2LX contains 120-pin header (CN2) which has EMIF, I2C, TIMI[1:0], TIMO[0:1], SPI, GPIO[16:0] and UART signal connections. It should be noted that EMIF, I2C, TIMI[1:0], TIMO[0:1], and SPI, GPIO[16:0] connections to this header (CN3) are of 1.8V level whereas UART signals are of 3.3V level.

3. TCIEVMK2LX EVM Board Physical Specifications

This chapter describes the physical layout of the TCIEVMK2LX EVM board and its connectors, switches and test points. It contains:

3.1 Board Layout

The TCIEVMK2LX EVM board dimension is 7.11" x 5.84" (180.6mm x 148.5mm). It is a 12 layer board and powered through connector DC_IN1. Figure 3-1 and 3-2 shows assembly layout of the TCIEVMK2LX EVM Board.

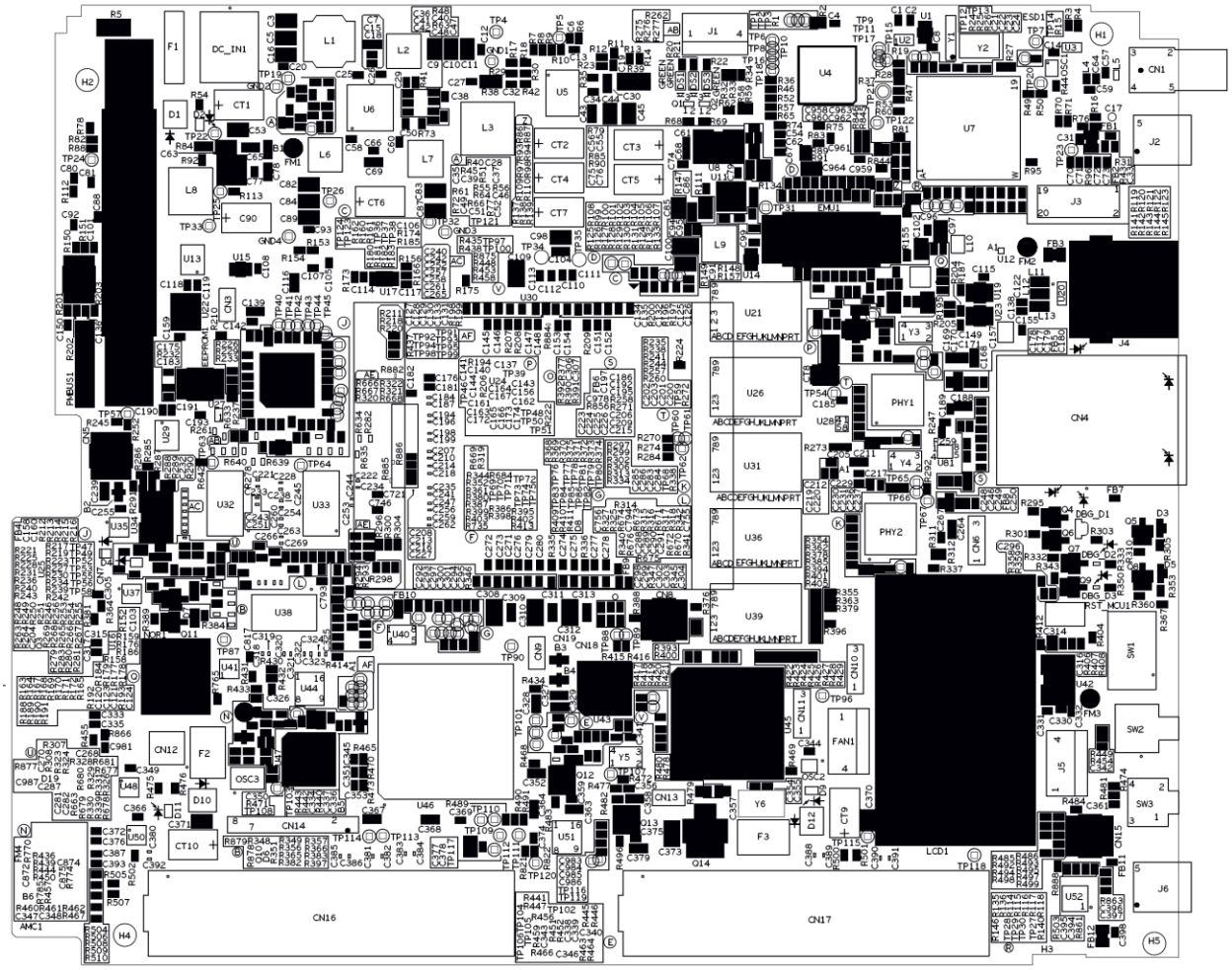


Figure 3.1: TCIEVMK2LX EVM Board Assembly Layout – TOP view

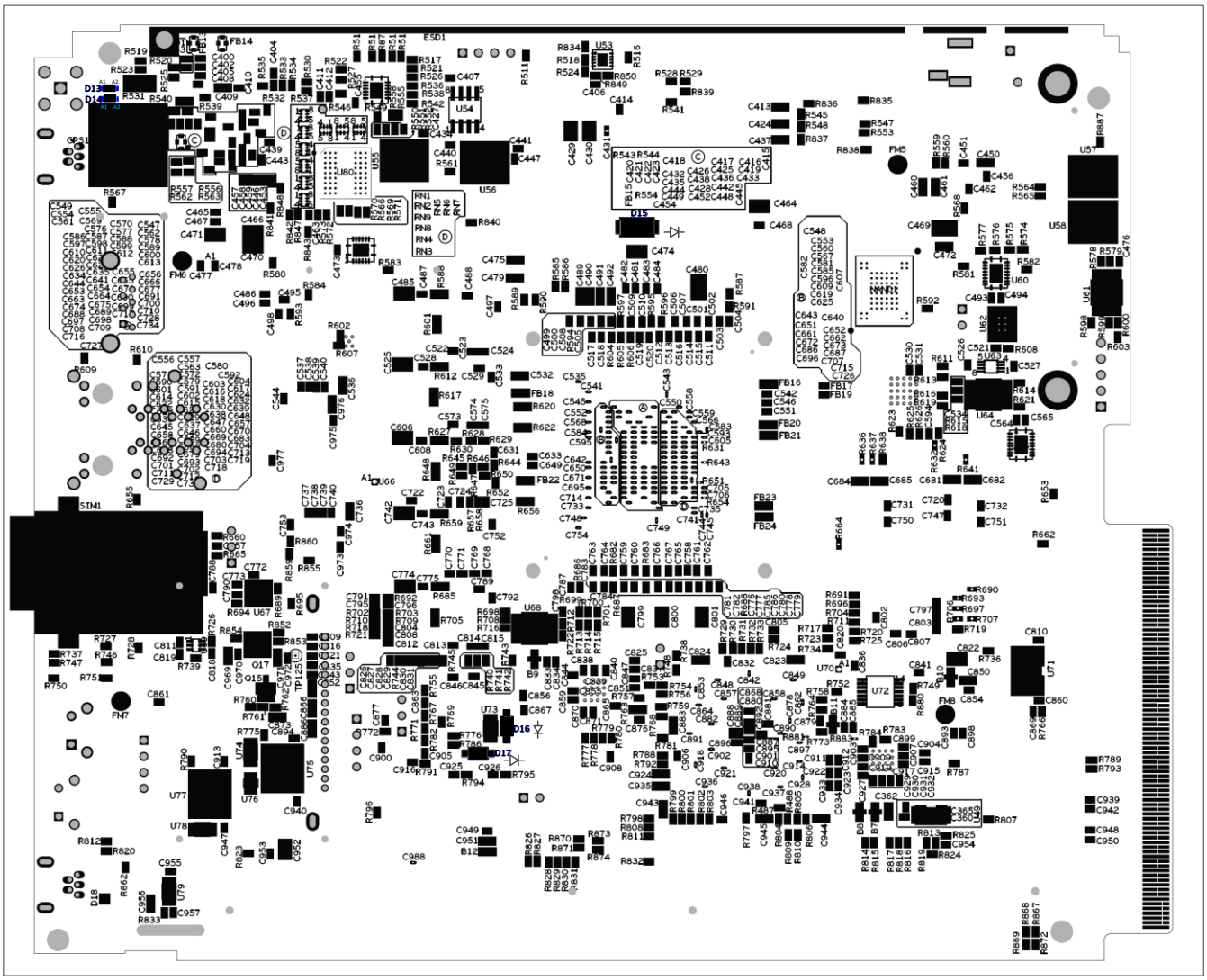


Figure 3.2: TCIEVMK2LX EVM Board layout – Bottom view

3.2 Connector Index

The TCIEVMK2LX EVM Board has several connectors which provide access to various interfaces on the board.

Table 3.1: TCIEVMK2LX EVM Board Connectors

Connector	Pins	Function
AMC1	170	AMC Edge Connector
CN1	5	GPS Input
CN2	120	EMIF, SPI, I2C, GPIO, TIMI[1:0], TIMO[1:0], and UART1 connections
CN3	2	JUMPER - VCC3V3_AUX_EN
CN4	24	Gigabit Ethernet RJ-45 Connector
CN5	10	Synchronization Event
CN6	3	SIM Power Value Select pin
CN7	3	10MHz input

CN8	10	FPGA Test Connector
CN9	2	JUMPER – FPGA Section 1
CN10	3	JUMPER – BMC Section 1
CN11	3	JUMPER – BMC Section 2
CN12	4	JUMPER – FPGA Section 2
CN13	2	JUMPER – BMC Section 3
CN14	8	FPGA JTAG Connector
CN15	10	MCU JTAG Connector
CN16	400	FMC1 Connector
CN17	400	FMC2 Connector
CN18	3	10MHz clock Positive output - U.FL connector
CN19	3	10MHz clock Negative output - U.FL connector
DC_IN1	3	DC Power Input Jack Connector
EMU1	60	TI 60-Pin SoC JTAG Connector
FAN1	4	FAN connector for +12V DC FAN
J1,J5	4	UART 4-Pin Connectors for SoC and BMC
J2	5	XDS200 USB mini connector
J3	20	XDS200 MCU JTAG
J4	9	USB3.0 TypeA
J6	5	Mini-USB Connector for UART console
PMBUS1	5	PMBUS for Smart-Reflex connected to UCD9090
SIM1	8	USIM Connector

3.2.1 AMC1, AMC Edge Connector

The AMC1 card edge connector plugs into an AMC compatible carrier board and provides a high speed AIL, PCIe, SGMII and IPMB-I2C interfaces to the carrier board. This connector is the 170 pin B+ style. The signals on this connector are shown in the table below:

Table 3.2: AMC Edge Connector

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground Signal	170	GND	Ground Signal
2	VCC12_AMC	+12V Power	169	AMC_JTAG_TDI	JTAG Data In
3	PS1#	Presence 1	168	AMC_JTAG_TDO	JTAG Data Out
4	VCC3V3_MP_AMC	Management Power	167	AMC_JTAG_RST#	JTAG Reset
5	MMC_GA0	Geographic Address 0	166	AMC_JTAG_TMS	JTAG TMS
6	NC	Reserved	165	AMC_JTAG_TCK	JTAG Clock
7	GND	Ground Signal	164	GND	Ground Signal
8	NC	Reserved	163	RP1_CLKP_AMC	RP Clock
9	VCC12_AMC	+12V Power	162	RP1_CLKN_AMC	RP Clock
10	GND	Ground Signal	161	GND	Ground Signal
11	AMC0_SGMII2_TX_DP	SGMII Port 0-TX	160	I2C_3V3_SCL	I2C Clock
12	AMC0_SGMII2_TX_DN	SGMII Port 0-TX	159	I2C_3V3_SDA	I2C Data
13	GND	Ground Signal	158	GND	Ground Signal
14	AMC0_SGMII2_RX_DP	SGMII Port 0-RX	157	RP1_FBP_AMC	RP Feedback
15	AMC0_SGMII2_RX_DN	SGMII Port 0-RX	156	RP1_FBN_AMC	RP Feedback
16	GND	Ground Signal	155	GND	Ground Signal
17	MMC_GA1	Geographic Address 1	154	PHYSYNC_AMC	PHYSYNC
18	VCC12_AMC	+12V Power	153	RADSYNC_AMC	RADSYNC
19	GND	Ground Signal	152	GND	Ground Signal
20	AMC1_SGMII3_TX_DP	SGMII Port 1-TX	151	AMC18_AIF1_TXP	AIL Port1-TX
21	AMC1_SGMII3_TX_DN	SGMII Port 1-TX	150	AMC18_AIF1_TXN	AIL Port1-TX
22	GND	Ground Signal	149	GND	Ground Signal
23	AMC1_SGMII3_RX_DP	SGMII Port 1-RX	148	AMC18_AIF1_RXP	AIL Port1-RX
24	AMC1_SGMII3_RX_DN	SGMII Port 1-RX	147	AMC18_AIF1_RXN	AIL Port1-RX
25	GND	Ground Signal	146	GND	Ground Signal
26	MMC_GA2	Geographic Address 2	145	AMC17_AIF0_TXP	AIL Port0-TX
27	VCC12_AMC	+12V Power	144	AMC17_AIF0_TXN	AIL Port0-TX
28	GND	Ground Signal	143	GND	Ground Signal

29	NC	Reserved	142	AMC17_AIF0_RXP	AIL Port0-RX
30	NC	Reserved	141	AMC17_AIF0_RXN	AIL Port0-RX
31	GND	Ground Signal	140	GND	Ground Signal
32	NC	Reserved	139	TCLKD_19.2MHz_P	Telecom Clock D
33	NC	Reserved	138	TCLKD_19.2MHz_N	Telecom Clock D
34	GND	Ground Signal	137	GND	Ground Signal
35	NC	Reserved	136	TIMER0IN1	Telecom Clock C
36	NC	Reserved	135	TIMER0OUT1	Telecom Clock C
37	GND	Ground Signal	134	GND	Ground Signal
38	NC	Reserved	133	NC	Reserved
39	NC	Reserved	132	NC	Reserved
40	GND	Ground Signal	131	GND	Ground Signal
41	MMC_ENABLE_N	Enable Signal	130	MDIO1	MDIO Data
42	VCC12_AMC	+12V Power	129	MDC1	MDIO Clock
43	GND	Ground Signal	128	GND	Ground Signal
44	AMC4_PCIe0_TX0P	PCIe Port 0-TX	127	NC	Reserved
45	AMC4_PCIe0_TX0N	PCIe Port 0-TX	126	NC	Reserved
46	GND	Ground Signal	125	GND	Ground Signal
47	AMC4_PCIe0_RX0P	PCIe Port 0-RX	124	NC	Reserved
48	AMC4_PCIe0_RX0N	PCIe Port 0-RX	123	NC	Reserved
49	GND	Ground Signal	122	GND	Ground Signal
50	NC	Reserved	121	NC	Reserved
51	NC	Reserved	120	NC	Reserved
52	GND	Ground Signal	119	GND	Ground Signal
53	NC	Reserved	118	NC	Reserved
54	NC	Reserved	117	NC	Reserved
55	GND	Ground Signal	116	GND	Ground Signal
56	SMB_SCL_IPMBL		115	NC	Reserved
57	VCC12_AMC	+12V Power	114	NC	Reserved
58	GND	Ground Signal	113	GND	Ground Signal
59	AMC6_PCIe1_TX0P	PCIe Port 1-TX	112	NC	Reserved
60	AMC6_PCIe1_TX0N	PCIe Port 1-TX	111	NC	Reserved
61	GND	Ground Signal	110	GND	Ground Signal
62	AMC6_PCIe1_RX0P	PCIe Port 1-RX	109	NC	Reserved
63	AMC6_PCIe1_RX0N	PCIe Port 1-RX	108	NC	Reserved
64	GND	Ground Signal	107	GND	Ground Signal
65	NC	Reserved	106	NC	Reserved
66	NC	Reserved	105	NC	Reserved
67	GND	Ground Signal	104	GND	Ground Signal
68	NC	Reserved	103	NC	Reserved
69	NC	Reserved	102	NC	Reserved

70	GND	Ground Signal	101	GND	Ground Signal
71	SMB_SDA_IPMBL		100	NC	Reserved
72	VCC12_AMC	+12V Power	99	NC	Reserved
73	GND	Ground Signal	98	GND	Ground Signal
74	NC	Reserved	97	NC	Reserved
75	NC	Reserved	96	NC	Reserved
76	GND	Ground Signal	95	GND	Ground Signal
77	TCLKB_25MHz_P	Telecom Clock B	94	NC	Reserved
78	TCLKB_25MHz_N	Telecom Clock B	93	NC	Reserved
79	GND	Ground Signal	92	GND	Ground Signal
80	PCIE_REF_CLK_P	FCLKA+	91	NC	Reserved
81	PCIE_REF_CLK_N	FCLKA-	90	NC	Reserved
82	GND	Ground Signal	89	GND	Ground Signal
83	PS0#	Presence 0	88	NC	Reserved
84	VCC12_AMC	+12V Power	87	NC	Reserved
85	GND	Ground Signal	86	GND	Ground Signal

3.2.2 CN1, GPS Input

CN1 is 5-pin SMA Jack for GPS input signal. The connections are shown in the table below:

Table 3.3: GPS Input Connectoe

Pin #	Signal Name
1	GPS_RF
2-5	Ground

3.2.3 CN2, Expansion Connector (EMIF, SPI, I2C, GPIO, TIMI[1:0], TIMO[1:0], UART1)

CN2 is an expansion header for several interfaces on the SoC. They are 16-bit EMIF, SPI, GPIO, Timer, I2C, and UART. The signal connections to the test header are as shown in a table below:

Table 3.4: Expansion Header pin out

Pin	Signal	Description	Pin	Signal	Description
1	VCC1V8	1.8V Supply	2	VCC1V8	1.8V Supply
3	GND	Ground	4	GND	Ground
5	EXP_SDA_3V3	SoC I2C data	6	SoC_EMIFA00	EMIF addr0
7	EXP_SCL_3V3	SoC I2C clock	8	SoC_EMIFA01	EMIF addr1
9	SoC_EMIFD0	EMIF data0	10	SoC_EMIFA02	EMIF addr2
11	SoC_EMIFD1	EMIF data1	12	SoC_EMIFA03	EMIF addr3
13	SoC_EMIFD2	EMIF data2	14	SoC_EMIFA04	EMIF addr4
15	SoC_EMIFD3	EMIF data3	16	SoC_EMIFA05	EMIF addr5
17	SoC_EMIFD4	EMIF data4	18	SoC_EMIFA06	EMIF addr6
19	SoC_EMIFD5	EMIF data5	20	SoC_EMIFA07	EMIF addr7
21	SoC_EMIFD6	EMIF data6	22	SoC_EMIFA08	EMIF addr8

23	SoC_EMIFD7	EMIF data7	24	SoC_EMIFA09	EMIF addr9
25	SoC_EMIFD8	EMIF data8	26	SoC_EMIFA10	EMIF addr10
27	SoC_EMIFD9	EMIF data9	28	SoC_EMIFA11	EMIF addr11
29	SoC_EMIFD10	EMIF data10	30	SoC_EMIFA12	EMIF addr12
31	SoC_EMIFD11	EMIF data11	32	SoC_EMIFA13	EMIF addr13
33	SoC_EMIFD12	EMIF data12	34	SoC_EMIFA14	EMIF addr14
35	SoC_EMIFD13	EMIF data13	36	SoC_EMIFA15	EMIF addr15
37	SoC_EMIFD14	EMIF data14	38	SoC_EMIFA16	EMIF addr16
39	SoC_EMIFD15	EMIF data15	40	SoC_EMIFA17	EMIF addr17
41	NC	Reserve	42	SoC_EMIFA18	EMIF addr18
43	SoC_EMIFCE1z	EMIF Space Enable1	44	SoC_EMIFA19	EMIF addr19
45	SoC_EMIFCE2z	EMIF Space Enable2	46	SoC_EMIFA20	EMIF addr20
47	SoC_EMIFCE3z	EMIF Space Enable3	48	SoC_EMIFA21	EMIF addr21
49	SoC_EMIFBE0z	EMIF Byte Enable0	50	SoC_EMIFA22	EMIF addr22
51	SoC_EMIFBE1z	EMIF Byte Enable1	52	SoC_EMIFA23	EMIF addr23
53	SoC_EMIFOEz	EMIF Output Enable	54	SoC_GPIO_00	SoC GPIO0
55	SoC_EMIFWEz	EMIF Write Enable	56	SoC_GPIO_01	SoC GPIO1
57	GND	Ground	58	GND	Ground
59	VCC5	5V Supply	60	VCC5	5V Supply
61	VCC3V3_AUX	3.3V Supply	62	VCC3V3_AUX	3.3V Supply
63	GND	Ground	64	GND	Ground
65	SoC_EMIFRNW	EMIF Read/Write	66	SoC_GPIO_02	SoC GPIO2
67	NC	Reserve	68	SoC_GPIO_03	SoC GPIO3
69	SoC_EMIFWAIT1	EMIF Wait	70	SoC_GPIO_04	SoC GPIO4
71	SoC_TIMO0	Timer input 0	72	SoC_GPIO_05	SoC GPIO5
73	EXP_TIMO0	Timer output 0	74	SoC_GPIO_06	SoC GPIO6
75	SoC_TIMO1	Timer input 1	76	SoC_GPIO_07	SoC GPIO7
77	EXP_TIMO1	Timer output 1	78	SoC_GPIO_08	SoC GPIO8
79	SoC_SSP2_MOSI	SPI data input	80	SoC_GPIO_09	SoC GPIO9
81	SoC_SSP2_MISO	SPI data output	82	SoC_GPIO_10	SoC GPIO10
83	SoC_SSP2_CS0	SPI chip select	84	SoC_GPIO_11	SoC GPIO11
85	SoC_SSP2_CS1	SPI chip select	86	SoC_GPIO_12	SoC GPIO12
87	SoC_SSP2_CS2	SPI chip select	88	SoC_GPIO_13	SoC GPIO13
89	SoC_SSP2_CS3	SPI chip select	90	SoC_GPIO_14	SoC GPIO14
91	SoC_SSP2_CLK	SPI clock	92	SoC_GPIO_15	SoC GPIO15
93	EXP_UART1_TXD_3V3	UART Serial Data Out (+3.3v)	94	SoC_GPIO_16	SoC GPIO16
95	EXP_UART1_RXD_3V3	UART Serial Data In (+3.3v)	96	EXP_TP0	Test point
97	SoC_UARTRTS	UART Request To (+3.3V)	98	EXP_TP1	MCU Resetstatz
99	SoC_UARTCTS	UART Cear To Send (+3.3v)	100	EXP_TP2	EXT_PS#
101	TSRX_CLK0N	SerDes recovered clock for SyncE	102	BD_PRESENT	Board Present
103	TSRX_CLK0P	SerDes recovered clock for SyncE	104	BD_ID0	Board ID
105	NC	Reserved	106	BD_ID1	Board ID

107	NC	Reserved	108	BD_ID2	Board ID
109	TSPUSHEVt0_E	PPS push event from GPS for IEEE1588	110	RSV_CLKN	Output Clock
111	TSPUSHEVt1_E	Push event from BCN for IEEE1588	112	RSV_CLKP	Output Clock
113	TSCOMPOUT_E	IEEE1588 compare output.	114	TSPUSHEVt0	PPS push event from GPS for IEEE1588
115	TSSYNCEVT_E	IEEE1588 sync event output.	116	TSCOMPOUT_E	IEEE1588 compare output.
117	GND	Ground	118	GND	Ground
119	VCC3V3_AUX	3.3V Supply	120	VCC3V3_AUX	3.3V Supply

3.2.4 CN3, Jumper for Enable Signal

This Jumper is used to select the enable signal for VCC3V3_AUX Power Supply Rail.

Table 3.5: Connector Pin Out

Pin #	Signal Name
1	VCC3V3_AUX_EN_R
2	VCC3V3_AUX_EN

3.2.5 CN4, Gigabit Ethernet Connector

CN4 is dual Gigabits RJ45 Ethernet connector with integrated magnetic. It is driven by Two Marvell Gigabit Ethernet transceiver 88E152. The connections are shown in the table below:

Table 3.6: Ethernet Connector Pin Out

Pin #	Signal Name	Pin #	Signal Name
A1	PHY1_MDI0_N	B1	PHY2_MDI0_N
A2	PHY1_MDI0_P	B2	PHY2_MDI0_P
A3	PHY1_MDI1_N	B3	PHY2_MDI1_N
A4	PHY1_MDI1_P	B4	PHY2_MDI1_P
A5	PHY1_MDI2_N	B5	PHY2_MDI2_N
A6	PHY1_MDI2_P	B6	PHY2_MDI2_P
A7	PHY1_MDI3_N	B7	PHY2_MDI3_N
A8	PHY1_MDI3_P	B8	PHY2_MDI3_P
A9	Center Tap	B9	Center Tap
A10	GND	B10	GND
A11	VCC2V5	B11	VCC2V5
A12	PHY1_LED_0	B12	PHY2_LED_0
A13	VCC2V5	B13	VCC2V5
A14	PHY1_LED_1	B14	PHY2_LED_1
SH1	Shield 1	SH3	Shield 3
SH2	Shield 2	SH4	Shield 4

3.2.6 CN5, Synchronization Event

CN5 is 10-pin male header for synchronization event signal. The connections are shown in the table below:

Table 3.7: Synchronization Event Connector Pin Out

Pin#	Signal Name	Pin#	Signal Name
1	GPS_PPS	2	GND
3	TSPUSHEVt0	4	SOC_TIMO1
5	TSCOMPOUT_E	6	RADSYNC
7	TSCOMPOUT_E	8	PHYSYNC
9	TSPUSHEVt1_E	10	Test Point

Default settings are showing in below figure:

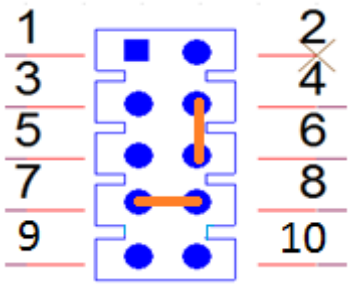


Figure 3.3: Sync Event Jumper Setting

3.2.7 CN6, SIM Power Value select header

CN6 is 3-pin header for program VSIM value. The selection has two output voltages as follows:

- VCC_SIM Value = 2.95V: installed over CN6 (1-2)
- VCC_SIM Value = 1.8V (Default): installed over CN6 (2-3)

The connections are shown in the table below:

Table 3.8: USIM Header Pin Out

Pin#	Signal Name
1	VCC1V8
2	SIM_SEL
3	GND

3.2.8 CN7, 10MHz Clock input

CN7 provides single ended 10MHz clock input. The pin out of is shown in below table:

Table 3.9: 10MHz Clock input Connector Pin Out

Pin#	Signal Name
1	GND
2	EXT_10MHz
3	GND

3.2.9 CN8, FPGA Test Connector

CN8 provides test signals from/to FPGA for testing purpose. The pin out of CN8 is shown below,

Table 3.10: FPGA Test Connector Pin Out

Pin#	Signal Name	Pin#	Signal Name
1	GPIO_0_TCON_FPGA_3V3	6	GPIO_3_TCON_FPGA_1V8
2	GPIO_5_TCON_FPGA_1V8	7	SYSREFREQ_TCON_FPGA_3V3
3	GPIO_1_TCON_FPGA_3V3	8	DLSYNC_3V3_TIMINGCON
4	GPIO_4_TCON_FPGA_1V8	9	TDD_TIME_SYNC_3V3_TIMINGCON
5	GPIO_2_TCON_FPGA_3V3	10	GND

3.2.10 CN9, JUMPER – FPGA Section 1

Table 3.11: Connector Pin Out

Pin #	Signal Name
1	EXT_TIMO1
2	EVM_TS_EXTFRAMEEVT_FPGA_1V8

3.2.11 CN10, JUMPER – BMC Section 1

Table 3.12: Connector Pin Out

Pin #	Signal Name
1	FULL_RESETz
2	MCU_WAKEz
3	GND

3.2.12 CN11, JUMPER – BMC Section 2

Table 3.13: Connector Pin Out

Pin #	Signal Name
1	VCC3V3_MP
2	VBAT
3	GND

3.2.13 CN12, FPGA Section 2

Table 3.14: Connector Pin Out

Pin #	Signal Name
A1	EXT_SWITCH_IN1_1V8
A2	EXT_SWITCH_IN2_1V8
B1	GND
B2	GND

3.2.14 CN13, JUMPER – BMC Section 3

Table 3.15: Connector Pin Out

Pin #	Signal Name
1	MCU_BOOTSELECT
2	GND

3.2.15 CN14, FPGA JTAG Connector (For Factory Use Only)

CN14 is an 8-pin JTAG connector for the FPGA programming. The pin out for the connector is shown in the table below:

Table 3.16: FPGA JTAG Header Pin Out

Pin #	Signal Name
1	VCC3V3_AUX
2	GND
3	FPGA_JTAG_TCK
4	FPGA_JTAG_TDI
5	FPGA_JTAG_TDO
6	FPGA_JTAG_TMS
7	FPGA_JTAG_RST#
8	VCC_1V8_FPGA

3.2.16 CN15, MCU JTAG Connector

CN15 is a 10-pin JTAG connector for ICDI (In Circuit Debug Interface) of MCU emulation, whenever an external emulator is plugged into CN22. The pin out for the connector is shown in table below:

Table 3.17: MCU JTAG Header Pin Out

Pin#	Signal Name	Pin#	Signal Name
1	VCC3V3_MP	2	BSC_JTAG_TMS
3	Ground	4	BSC_JTAG_TCK
5	Ground	6	BSC_JTAG_TDO
7	NC	8	BSC_JTAG_TDI
9	Ground	10	BSC_JTAG_SRSTN

3.2.17 CN16, FMC1 (AFE7500EVM Card) Interface

CN16 is a 400 pin connector where AFE7500EVM Card is connected. The pin out details is shown in below table.

Table 3.18: FMC1 Connector Pin Out

Pin	Signal	Description	Pin	Signal	Description
A1	GND	Ground Signal	H7	SPI_CLK_FMC1_FPGA_1V8	SPI Clock
A2	JESD1_RXP_FMC1	JESD Port1 RX	H8	SPI_CS0_FMC1_FPGA_1V8	SPI Chip Select
A3	JESD1_RXN_FMC1	JESD Port1 RX	H9	GND	Ground Signal
A4	GND	Ground Signal	H12	GND	Ground Signal
A5	GND	Ground Signal	H13	STATUS_0_FMC1_FPGA_1V8	Status 0 signal
A6	JESD2_RXP_FMC1	JESD Port2 RX	H14	STATUS_1_FMC1_FPGA_1V8	Status 1 signal
A7	JESD2_RXN_FMC1	JESD Port2 RX	H15	GND	Ground Signal
A8	GND	Ground Signal	H18	GND	Ground Signal
A9	GND	Ground Signal	H21	GND	Ground Signal
A10	JESD3_RXP_FMC1	JESD Port3 RX	H24	GND	Ground Signal
A11	JESD3_RXN_FMC1	JESD Port3 RX	H27	GND	Ground Signal
A12	GND	Ground Signal	H30	GND	Ground Signal
A13	GND	Ground Signal	H33	GND	Ground Signal
A16	GND	Ground Signal	H36	GND	Ground Signal
A17	GND	Ground Signal	H39	GND	Ground Signal
A20	GND	Ground Signal	A31	JESD3_TXN_FMC1	JESD Port3 TX
A21	GND	Ground Signal	A30	JESD3_TXP_FMC1	JESD Port3 TX
A24	GND	Ground Signal	A23	JESD1_TXN_FMC1	JESD Port1 TX
A25	GND	Ground Signal	A22	JESD1_TXP_FMC1	JESD Port1 TX

A28	GND	Ground Signal	A27	JESD2_TXN_FMC1	JESD Port2 TX
A29	GND	Ground Signal	A26	JESD2_TXP_FMC1	JESD Port2 TX
A32	GND	Ground Signal	C3	JESD0_TXN_FMC1	JESD Port0 TX
A33	GND	Ground Signal	C2	JESD0_TXP_FMC1	JESD Port0 TX
A36	GND	Ground Signal	J15	NC	
A37	GND	Ground Signal	J16	NC	
A40	GND	Ground Signal	J18	NC	
B2	GND	Ground Signal	J19	NC	
B3	GND	Ground Signal	J21	NC	
B6	GND	Ground Signal	J22	NC	
B7	GND	Ground Signal	A14	NC	
B10	GND	Ground Signal	A15	NC	
B11	GND	Ground Signal	A18	NC	
B14	GND	Ground Signal	A19	NC	
B15	GND	Ground Signal	A34	NC	
B18	GND	Ground Signal	A35	NC	
B19	GND	Ground Signal	A38	NC	
B22	GND	Ground Signal	A39	NC	
B23	GND	Ground Signal	B1	NC	
B26	GND	Ground Signal	B4	NC	
B27	GND	Ground Signal	B5	NC	
B30	GND	Ground Signal	B8	NC	
B31	GND	Ground Signal	B9	NC	
B34	GND	Ground Signal	B12	NC	
B35	GND	Ground Signal	B13	NC	
B38	GND	Ground Signal	B16	NC	
B39	GND	Ground Signal	B17	NC	
C1	GND	Ground Signal	B20	NC	
C4	GND	Ground Signal	B21	NC	
C5	GND	Ground Signal	B24	NC	
C6	JESD0_RXP_FMC1	JESD Port0 RX	B25	NC	
C7	JESD0_RXN_FMC1	JESD Port0 RX	B28	NC	
C8	GND	Ground Signal	B29	NC	
C9	GND	Ground Signal	B32	NC	
C10	GPIO1_5_FMC1_FPGA_3V3	GPIO signal-port1	B33	NC	
C11	GPIO1_6_FMC1_FPGA_3V3	GPIO signal-port1	B36	NC	
C12	GND	Ground Signal	B37	NC	
C13	GND	Ground Signal	B40	NC	
C16	GND	Ground Signal	C14	NC	
C17	GND	Ground Signal	C15	NC	
C20	GND	Ground Signal	C18	NC	
C21	GND	Ground Signal	C19	NC	
C24	GND	Ground Signal	C22	NC	

C25	GND	Ground Signal	C23	NC	
C28	GND	Ground Signal	C26	NC	
C29	GND	Ground Signal	C27	NC	
C32	GND	Ground Signal	C30	NC	
C33	GND	Ground Signal	C31	NC	
C35	12VIN_FMC1	12V DC Power	C34	NC	
C36	GND	Ground Signal	D1	NC	
C37	12VIN_FMC1	12V DC Power	D4	NC	
C38	GND	Ground Signal	D5	NC	
C39	3V3_IN_FMC1	3.3V DC Power	D8	NC	
C40	GND	Ground Signal	D9	NC	
D2	GND	Ground Signal	D12	NC	
D3	GND	Ground Signal	D14	NC	
D6	GND	Ground Signal	D15	NC	
D7	GND	Ground Signal	D17	NC	
D10	GND	Ground Signal	D18	NC	
D11	GPIO1_7_FMC1_FPGA_3V3	GPIO signal-port1	D20	NC	
D13	GND	Ground Signal	D21	NC	
D16	GND	Ground Signal	D23	NC	
D19	GND	Ground Signal	D24	NC	
D22	GND	Ground Signal	D26	NC	
D25	GND	Ground Signal	D27	NC	
D28	GND	Ground Signal	D29	NC	
D37	GND	Ground Signal	D30	NC	
D39	GND	Ground Signal	D31	NC	
J1	GND	Ground Signal	D32	NC	
J2	SYSREF_P_FMC1	SYSREF clock	D33	NC	
J3	SYSREF_N_FMC1	SYSREF clock	D34	NC	
J4	GND	Ground Signal	D35	NC	
J5	GND	Ground Signal	D36	NC	
J6	SPI_MOSI_FMC1_FPGA_1V8	SPI MOSI	D38	NC	
J7	SPI_MISO_FMC1_FPGA_1V8	SPI MISO	D40	NC	
J8	GND	Ground Signal	J12	NC	
J9	BUSY#_FMC1_FPGA_1V8	Busy signal	J13	NC	
J10	RST#_FMC1_FPGA_1V8	Reset signal	J30	NC	
J11	GND	Ground Signal	J39	NC	
J14	GND	Ground Signal	K1	NC	
J17	GND	Ground Signal	K7	NC	
J20	GND	Ground Signal	K8	NC	
J23	GND	Ground Signal	K10	NC	
J24	GPDAC1_FMC1_FPGA_1V8	GPIO signal-port2	K11	NC	
J25	GPDAC2_FMC1_FPGA_1V8	GPIO signal-port2	K13	NC	
J26	GND	Ground Signal	K14	NC	
J27	GPDAC3_FMC1_FPGA_1V8	GPIO signal-	K16	NC	

		port2			
J28	GPDAC4_FMC1_FPGA_1V8	GPIO signal-port2	K17	NC	
J29	GND	Ground Signal	K19	NC	
J31	GPIO0_0/ GPTEST_FMC1_FPGA_1V8	GPIO signal-port0	K20	NC	
J32	GND	Ground Signal	K22	NC	
J33	GPDAC5_FMC1_FPGA_1V8	GPIO signal-port2	K23	NC	
J34	GPDAC6_FMC1_FPGA_1V8	GPIO signal-port2	K25	NC	
J35	GND	Ground Signal	K26	NC	
J36	GPDAC7_FMC1_FPGA_1V8	GPIO signal-port2	K28	NC	
J37	GPDAC8_FMC1_FPGA_1V8	GPIO signal-port2	K29	NC	
J38	GND	Ground Signal	K31	NC	
J40	GND	Ground Signal	K32	NC	
K2	GND	Ground Signal	K34	NC	
K3	GND	Ground Signal	K35	NC	
K4	SYS_CLKP_FMC1	System clock	K37	NC	
K5	SYS_CLKN_FMC1	System clock	K38	NC	
K6	GND	Ground Signal	K40	NC	
K9	GND	Ground Signal	E2	NC	
K12	GND	Ground Signal	E3	NC	
K15	GND	Ground Signal	E6	NC	
K18	GND	Ground Signal	E7	NC	
K21	GND	Ground Signal	E9	NC	
K24	GND	Ground Signal	E10	NC	
K27	GND	Ground Signal	E13	NC	
K30	GND	Ground Signal	E21	NC	
K33	GND	Ground Signal	E22	NC	
K36	GND	Ground Signal	E24	NC	
K39	GND	Ground Signal	E25	NC	
E1	GND	Ground Signal	E27	NC	
E4	GND	Ground Signal	E28	NC	
E5	GND	Ground Signal	E36	NC	
E8	GND	Ground Signal	E37	NC	
E11	GND	Ground Signal	E39	NC	
E12	IRQ_FMC1_FPGA_3V3	Interrupt Request signal	F1	NC	
E14	GND	Ground Signal	F4	NC	
E15	GPIO0_1_FMC1_FPGA_3V3	GPIO signal-port0	F5	NC	
E16	GPIO0_2_FMC1_FPGA_3V3	GPIO signal-port0	F7	NC	
E17	GND	Ground Signal	F8	NC	
E18	GPIO1_3_FMC1_FPGA_1V8	GPIO signal-port1	F13	NC	
E19	GPIO1_4_FMC1_FPGA_1V8	GPIO signal-	F14	NC	

		port1			
E20	GND	Ground Signal	F19	NC	
E23	GND	Ground Signal	F20	NC	
E26	GND	Ground Signal	F22	NC	
E29	GND	Ground Signal	F23	NC	
E30	SPI_CLK_LMK_FMC1_ FPGA_1V8	LMK SPI Clock	F25	NC	
E31	SPI_CS1_LMK_FMC1_ FPGA_1V8	LMK SPI Chip Select	F26	NC	
E32	GND	Ground Signal	F28	NC	
E33	SPI_MOSI_LMK_FMC1_ FPGA_1V8	LMK SPI MOSI	F29	NC	
E34	SPI_MISO/ RST_LMK_FMC1_FPGA_1V8	LMK SPI MISO/Reset	F31	NC	
E35	GND	Ground Signal	F32	NC	
E38	GND	Ground Signal	F34	NC	
E40	GND	Ground Signal	F35	NC	
F2	GND	Ground Signal	F37	NC	
F3	GND	Ground Signal	F38	NC	
F6	GND	Ground Signal	F40	NC	
F9	GND	Ground Signal	G2	NC	
F10	SOC_JESD_SYNCIN0_P_ FMC1	JESD SYNC In0	G3	NC	
F11	SOC_JESD_SYNCIN0_N_ FMC1	JESD SYNC In0	G6	NC	
F12	GND	Ground Signal	G7	NC	
F15	GND	Ground Signal	G9	NC	
F16	GPIO0_5_FMC1_FPGA_1V8	GPIO signal-port0	G10	NC	
F17	GPIO0_4_FMC1_FPGA_1V8	GPIO signal-port0	G24	NC	
F18	GND	Ground Signal	G25	NC	
F21	GND	Ground Signal	G27	NC	
F24	GND	Ground Signal	G28	NC	
F27	GND	Ground Signal	G30	NC	
F30	GND	Ground Signal	G31	NC	
F33	GND	Ground Signal	G33	NC	
F36	GND	Ground Signal	G34	NC	
F39	GND	Ground Signal	G36	NC	
G1	GND	Ground Signal	G37	NC	
G4	GND	Ground Signal	G39	NC	
G5	GND	Ground Signal	H1	NC	
G8	GND	Ground Signal	H2	NC	
G11	GND	Ground Signal	H4	NC	
G12	SOC_JESD_SYNCOUT0_P_ FMC1	JESD SYNC Out0	H5	NC	
G13	SOC_JESD_SYNCOUT0_N_ FMC1	JESD SYNC Out0	H10	NC	
G14	GND	Ground Signal	H11	NC	
G15	GPIO1_0_FMC1_FPGA_1V8	GPIO signal-	H16	NC	

		port1			
G16	GPIO1_2_FMC1_FPGA_1V8	GPIO signal-port1	H17	NC	
G17	GND	Ground Signal	H19	NC	
G18	GPIO1_1_FMC1_FPGA_1V8	GPIO signal-port1	H20	NC	
G19	GPIO0_3_FMC1_FPGA_1V8	GPIO signal-port0	H22	NC	
G20	GND	Ground Signal	H23	NC	
G21	GPIO0_6_FMC1_FPGA_1V8	GPIO signal-port0	H25	NC	
G22	GPIO0_7_FMC1_FPGA_1V8	GPIO signal-port0	H26	NC	
G23	GND	Ground Signal	H28	NC	
G26	GND	Ground Signal	H29	NC	
G29	GND	Ground Signal	H31	NC	
G32	GND	Ground Signal	H32	NC	
G35	GND	Ground Signal	H34	NC	
G38	GND	Ground Signal	H35	NC	
G40	GND	Ground Signal	H37	NC	
H3	GND	Ground Signal	H38	NC	
H6	GND	Ground Signal	H40	NC	

3.2.18 CN17, FMC2 (AFE7500EVM Card) Interface

CN17 is a 400 pin connector where AFE7500EVM Card is connected. The pin out details is shown in below table.

Table 3.19: FMC2 Connector Pin Out

Pin	Signal	Description	Pin	Signal	Description
A1	GND	Ground Signal	H13	STATUS_0_FMC2_FPGA_1V8	Status 0 signal
A4	GND	Ground Signal	H14	STATUS_1_FMC2_FPGA_1V8	Status 1 signal
A5	GND	Ground Signal	H15	GND	Ground Signal
A6	JESD2_RXP_FMC2	JESD Port2 RX	H18	GND	Ground Signal
A7	JESD2_RXN_FMC2	JESD Port2 RX	H21	GND	Ground Signal
A8	GND	Ground Signal	H24	GND	Ground Signal
A9	GND	Ground Signal	H27	GND	Ground Signal
A10	JESD3_RXP_FMC2	JESD Port3 RX	H30	GND	Ground Signal
A11	JESD3_RXN_FMC2	JESD Port3 RX	H33	GND	Ground Signal
A12	GND	Ground Signal	H36	GND	Ground Signal
A13	GND	Ground Signal	H39	GND	Ground Signal
A16	GND	Ground Signal	A31	JESD3_TXN_FMC2	JESD Port3 TX
A17	GND	Ground Signal	A30	JESD3_TXP_FMC2	JESD Port3 TX
A20	GND	Ground Signal	A23	Terminated	Terminated to GND with 49.9E
A21	GND	Ground Signal	A22	Terminated	Terminated to GND with 49.9E
A24	GND	Ground Signal	A27	JESD2_TXN_FMC2	JESD Port2 TX
A25	GND	Ground Signal	A26	JESD2_TXP_FMC2	JESD Port2 TX

A28	GND	Ground Signal	A3	Terminated	Terminated to GND with 49.9E
A29	GND	Ground Signal	A2	Terminated	Terminated to GND with 49.9E
A32	GND	Ground Signal	C7	Terminated	Terminated to GND with 49.9E
A33	GND	Ground Signal	C6	Terminated	Terminated to GND with 49.9E
A36	GND	Ground Signal	J15	NC	
A37	GND	Ground Signal	J16	NC	
A40	GND	Ground Signal	J18	NC	
B2	GND	Ground Signal	J19	NC	
B3	GND	Ground Signal	J21	NC	
B6	GND	Ground Signal	J22	NC	
B7	GND	Ground Signal	C3	Terminated	Terminated to GND with 49.9E
B10	GND	Ground Signal	C2	Terminated	Terminated to GND with 49.9E
B11	GND	Ground Signal	A14	NC	
B14	GND	Ground Signal	A15	NC	
B15	GND	Ground Signal	A18	NC	
B18	GND	Ground Signal	A19	NC	
B19	GND	Ground Signal	A34	NC	
B22	GND	Ground Signal	A35	NC	
B23	GND	Ground Signal	A38	NC	
B26	GND	Ground Signal	A39	NC	
B27	GND	Ground Signal	B1	NC	
B30	GND	Ground Signal	B4	NC	
B31	GND	Ground Signal	B5	NC	
B34	GND	Ground Signal	B8	NC	
B35	GND	Ground Signal	B9	NC	
B38	GND	Ground Signal	B12	NC	
B39	GND	Ground Signal	B13	NC	
C1	GND	Ground Signal	B16	NC	
C4	GND	Ground Signal	B17	NC	
C5	GND	Ground Signal	B20	NC	
C8	GND	Ground Signal	B21	NC	
C9	GND	Ground Signal	B24	NC	
C10	GPIO1_5_FMC2_FPGA_3V3	GPIO signal-port1	B25	NC	
C11	GPIO1_6_FMC2_FPGA_3V3	GPIO signal-port1	B28	NC	
C12	GND	Ground Signal	B29	NC	
C13	GND	Ground Signal	B32	NC	
C16	GND	Ground Signal	B33	NC	
C17	GND	Ground Signal	B36	NC	
C20	GND	Ground Signal	B37	NC	
C21	GND	Ground Signal	B40	NC	
C24	GND	Ground Signal	C14	NC	

C25	GND	Ground Signal	C15	NC	
C28	GND	Ground Signal	C18	NC	
C29	GND	Ground Signal	C19	NC	
C32	GND	Ground Signal	C22	NC	
C33	GND	Ground Signal	C23	NC	
C35	12VIN_FMC2	12V DC Power	C26	NC	
C36	GND	Ground Signal	C27	NC	
C37	12VIN_FMC2	12V DC Power	C30	NC	
C38	GND	Ground Signal	C31	NC	
C39	3V3_IN_FMC2	3.3V DC Power	C34	NC	
C40	GND	Ground Signal	D1	NC	
D2	GND	Ground Signal	D4	NC	
D3	GND	Ground Signal	D5	NC	
D6	GND	Ground Signal	D8	NC	
D7	GND	Ground Signal	D9	NC	
D10	GND	Ground Signal	D12	NC	
D11	GPIO1_7_FMC2_FPGA_3V3	GPIO signal-port1	D14	NC	
D13	GND	Ground Signal	D15	NC	
D16	GND	Ground Signal	D17	NC	
D19	GND	Ground Signal	D18	NC	
D22	GND	Ground Signal	D20	NC	
D25	GND	Ground Signal	D21	NC	
D28	GND	Ground Signal	D23	NC	
D37	GND	Ground Signal	D24	NC	
D39	GND	Ground Signal	D26	NC	
J1	GND	Ground Signal	D27	NC	
J2	SYSREF_P_FMC2	SYSREF clock	D29	NC	
J3	SYSREF_N_FMC2	SYSREF clock	D30	NC	
J4	GND	Ground Signal	D31	NC	
J5	GND	Ground Signal	D32	NC	
J6	SPI_MOSI_FMC2_FPGA_1V8	SPI MOSI	D33	NC	
J7	SPI_MISO_FMC2_FPGA_1V8	SPI MISO	D34	NC	
J8	GND	Ground Signal	D35	NC	
J9	BUSY#_FMC2_FPGA_1V8	Busy signal	D36	NC	
J10	RST#_FMC2_FPGA_1V8	Reset signal	D38	NC	
J11	GND	Ground Signal	D40	NC	
J14	GND	Ground Signal	J12	NC	
J17	GND	Ground Signal	J13	NC	
J20	GND	Ground Signal	J30	NC	
J23	GND	Ground Signal	J39	NC	
J24	GPDAC1_FMC2_FPGA_1V8	GPIO signal-port2	K1	NC	
J25	GPDAC2_FMC2_FPGA_1V8	GPIO signal-port2	K7	NC	
J26	GND	Ground Signal	K8	NC	
J27	GPDAC3_FMC2_FPGA_1V8	GPIO signal-port2	K10	NC	

J28	GPDAC4_FMC2_FPGA_1V8	GPIO signal-port2	K11	NC	
J29	GND	Ground Signal	K13	NC	
J31	GPIO0_0/GPTEST_FMC2_FPGA_1V8	GPIO signal-port2	K14	NC	
J32	GND	Ground Signal	K16	NC	
J33	GPDAC5_FMC2_FPGA_1V8	GPIO signal-port2	K17	NC	
J34	GPDAC6_FMC2_FPGA_1V8	GPIO signal-port2	K19	NC	
J35	GND	Ground Signal	K20	NC	
J36	GPDAC7_FMC2_FPGA_1V8	GPIO signal-port2	K22	NC	
J37	GPDAC8_FMC2_FPGA_1V8	GPIO signal-port2	K23	NC	
J38	GND	Ground Signal	K25	NC	
J40	GND	Ground Signal	K26	NC	
K2	GND	Ground Signal	K28	NC	
K3	GND	Ground Signal	K29	NC	
K4	SYS_CLKP_FMC2	System clock	K31	NC	
K5	SYS_CLKN_FMC2	System clock	K32	NC	
K6	GND	Ground Signal	K34	NC	
K9	GND	Ground Signal	K35	NC	
K12	GND	Ground Signal	K37	NC	
K15	GND	Ground Signal	K38	NC	
K18	GND	Ground Signal	K40	NC	
K21	GND	Ground Signal	E2	NC	
K24	GND	Ground Signal	E3	NC	
K27	GND	Ground Signal	E6	NC	
K30	GND	Ground Signal	E7	NC	
K33	GND	Ground Signal	E9	NC	
K36	GND	Ground Signal	E10	NC	
K39	GND	Ground Signal	E13	NC	
E1	GND	Ground Signal	E21	NC	
E4	GND	Ground Signal	E22	NC	
E5	GND	Ground Signal	E24	NC	
E8	GND	Ground Signal	E25	NC	
E11	GND	Ground Signal	E27	NC	
E12	IRQ_FMC2_FPGA_3V3	Interrupt Request signal	E28	NC	
E14	GND	Ground Signal	E36	NC	
E15	GPIO0_1_FMC2_FPGA_3V3	GPIO signal-port0	E37	NC	
E16	GPIO0_2_FMC2_FPGA_3V3	GPIO signal-port0	E39	NC	
E17	GND	Ground Signal	F1	NC	
E18	GPIO1_3_FMC2_FPGA_1V8	GPIO signal-port1	F4	NC	
E19	GPIO1_4_FMC2_FPGA_1V8	GPIO signal-port1	F5	NC	

E20	GND	Ground Signal	F7	NC	
E23	GND	Ground Signal	F8	NC	
E26	GND	Ground Signal	F13	NC	
E29	GND	Ground Signal	F14	NC	
E30	SPI_CLK_LMK_FMC2_FPGA _1V8	LMK SPI Clock	F19	NC	
E31	SPI_CS3_LMK_FMC2_FPGA _1V8	LMK SPI Chip Select	F20	NC	
E32	GND	Ground Signal	F22	NC	
E33	SPI_MOSI_LMK_FMC2_ FPGA _1V8	LMK SPI MOSI	F23	NC	
E34	SPI_MISO/RST_LMK_FMC2_ FPGA_1V8	LMK SPI MISO/Reset	F25	NC	
E35	GND	Ground Signal	F26	NC	
E38	GND	Ground Signal	F28	NC	
E40	GND	Ground Signal	F29	NC	
F2	GND	Ground Signal	F31	NC	
F3	GND	Ground Signal	F32	NC	
F6	GND	Ground Signal	F34	NC	
F9	GND	Ground Signal	F35	NC	
F10	SOC_JESD_SYNCIN1_P_ FMC2	JESD SYNC In0	F37	NC	
F11	SOC_JESD_SYNCIN1_N_ FMC2	JESD SYNC In0	F38	NC	
F12	GND	Ground Signal	F40	NC	
F15	GND	Ground Signal	G2	NC	
F16	GPIO0_5_FMC2_FPGA_1V8	GPIO signal-port0	G3	NC	
F17	GPIO0_4_FMC2_FPGA_1V8	GPIO signal-port0	G6	NC	
F18	GND	Ground Signal	G7	NC	
F21	GND	Ground Signal	G9	NC	
F24	GND	Ground Signal	G10	NC	
F27	GND	Ground Signal	G24	NC	
F30	GND	Ground Signal	G25	NC	
F33	GND	Ground Signal	G27	NC	
F36	GND	Ground Signal	G28	NC	
F39	GND	Ground Signal	G30	NC	
G1	GND	Ground Signal	G31	NC	
G4	GND	Ground Signal	G33	NC	
G5	GND	Ground Signal	G34	NC	
G8	GND	Ground Signal	G36	NC	
G11	GND	Ground Signal	G37	NC	
G12	SOC_JESD_SYNCOUT1_P_ FMC2	JESD SYNC Out0	G39	NC	
G13	SOC_JESD_SYNCOUT1_N_ FMC2	JESD SYNC Out0	H1	NC	
G14	GND	Ground Signal	H2	NC	
G15	GPIO1_0_FMC2_FPGA_1V8	GPIO signal-port1	H4	NC	

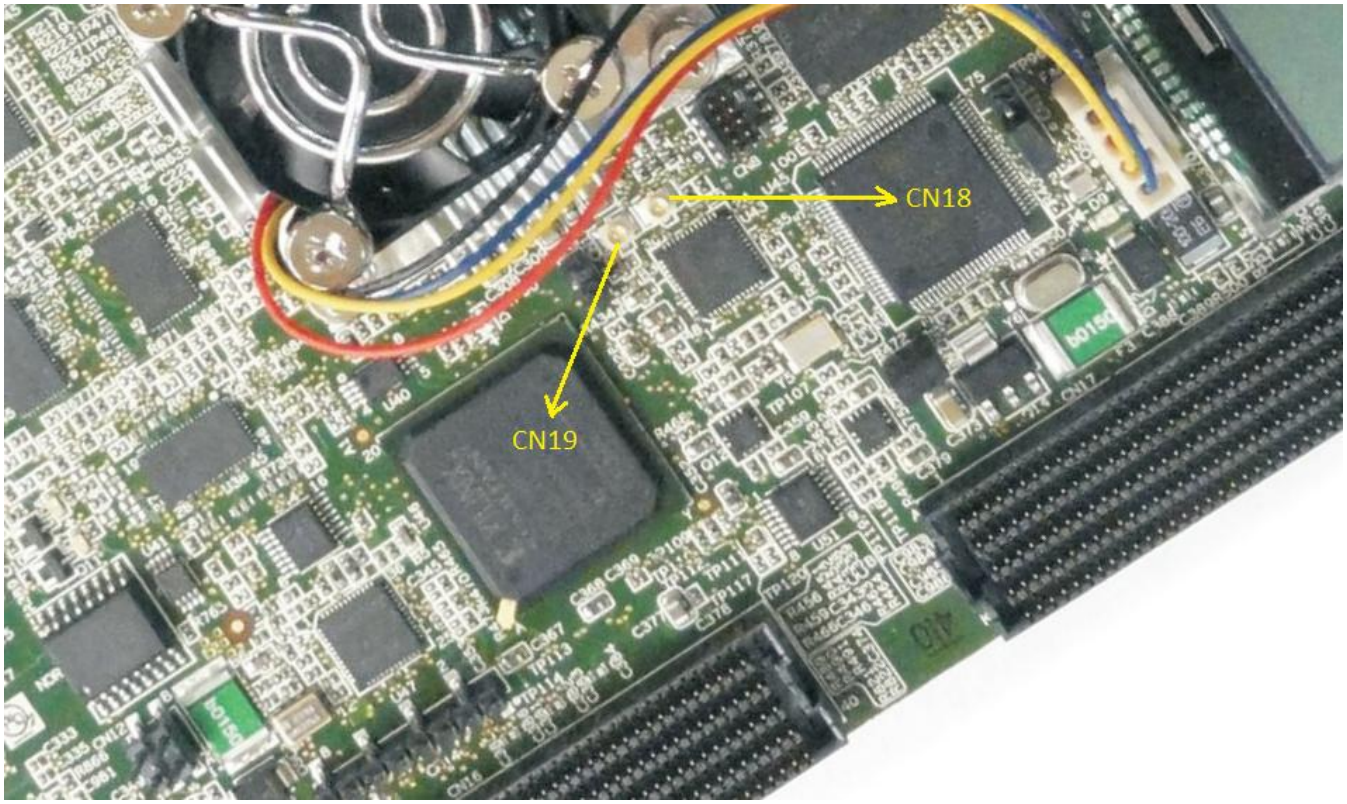
G16	GPIO1_2_FMC2_FPGA_1V8	GPIO signal-port1	H5	NC	
G17	GND	Ground Signal	H10	NC	
G18	GPIO1_1_FMC2_FPGA_1V8	GPIO signal-port1	H11	NC	
G19	GPIO0_3_FMC2_FPGA_1V8	GPIO signal-port0	H16	NC	
G20	GND	Ground Signal	H17	NC	
G21	GPIO0_6_FMC2_FPGA_1V8	GPIO signal-port0	H19	NC	
G22	GPIO0_7_FMC2_FPGA_1V8	GPIO signal-port0	H20	NC	
G23	GND	Ground Signal	H22	NC	
G26	GND	Ground Signal	H23	NC	
G29	GND	Ground Signal	H25	NC	
G32	GND	Ground Signal	H26	NC	
G35	GND	Ground Signal	H28	NC	
G38	GND	Ground Signal	H29	NC	
G40	GND	Ground Signal	H31	NC	
H3	GND	Ground Signal	H32	NC	
H6	GND	Ground Signal	H34	NC	
H7	SPI_CLK_FMC2_FPGA_1V8	SPI Clock	H35	NC	
H8	SPI_CS2_FMC2_FPGA_1V8	SPI Chip Select	H37	NC	
H9	GND	Ground Signal	H38	NC	
H12	GND	Ground Signal	H40	NC	

3.2.19 CN18, 10MHz Clock Positive Output – U.FL connector

Table 3.20: 10MHz Clock Output Connector Pin Out

Pin#	Signal Name
1	GND
2	10M_TESTP
3	GND

Refer below picture to identify CN18 and CN19.



3.2.20 CN19, 10MHz Clock Negative Output – U.FL connector

Table 3.21: 10MHz Clock Output Connector Pin Out

Pin#	Signal Name
1	GND
2	10M_TESTN
3	GND

3.2.21 DC_IN1, 12V DC Input Jack

DC_IN1 is a DC Power-in Jack Connector for the stand-alone application of EVM. It is a 2.5mm power jack with positive center tap polarity. Do not use this connector if EVM is inserted into MicroTCA chassis or AMC carrier backplane.

3.2.22 EMU1, TI MIPI 60-Pin SoC JTAG Connector

EMU1 is a high speed system trace capable TI 60 pin JTAG connector for XDSxxx type of SoC/DSP emulation. The onboard switch multiplexes this interface with the on-board XDS200 type emulator. Whenever an external emulator is plugged into EMU1, the on board XDS200 emulator disconnects from SoC and external emulator connects to SoC automatically. The I/O voltage level on these pins is 1.8V. So any 1.8V level compatible emulator can be used to interface with the TCI6630K2L. The pin out for the connector is shown in figure below:

Table 3.22: MIPI 60 Connector Pin Out

Pin#	Signal Name	Pin#	Signal Name
1	TVD (+1.8V)	2	TMS
3	TCLK	4	TDO
5	TDI	6	TRGRST#
7	TCLKRTN	8	EMU_TRST#
9	nTRST(NC)	10	NC
11	NC	12	TVD
13	EMU2	14	TRC_CLK1(NC)
15	TDIS	16	Ground
17	EMU3	18	EMU21
19	EMU0	20	EMU22
21	EMU1	22	EMU23
23	EMU4	24	EMU24
25	EMU5	26	EMU25
27	EMU6	28	EMU26
29	EMU7	30	EMU27
31	EMU8	32	EMU28
33	EMU9	34	EMU29
35	EMU10	36	EMU30
37	EMU11	38	EMU31
39	EMU12	40	EMU32
41	EMU13	42	EMU33
43	EMU14	44	NC
45	EMU15	46	NC
47	EMU16	48	NC
49	EMU17	50	NC
51	EMU18	52	NC
53	EMU19	54	NC
55	EMU20	56	NC
57	Ground	58	EXT_EMU_DET
59	TRC_CLK(NC)	60	NC

3.2.23 FAN1, FAN Connector

The EVM incorporates a dedicated cooling fan. This fan has the capability of easily being removed when the EVM is inserted into an AMC backplane which uses forced air cooling. The fan selected provides maximum cooling (CFM) and operates on 12Vdc provided by EVM. It should be noted that the adjustment of the fan speed is supported by UCD9090 through FAN Duty cycle control.

Table 3.23: FAN1 Connector Pin Out

Pin#	Signal Name
1	GNG
2	+12Vdc
3	NC
4	FAN_PWM

3.2.24 J1 and J5, UART 4-pin connectors for SoC and BMC

There are two 4-pin male connectors for RS232 serial interface with EVM. One is for SoC UART and other is for BMC UART. A 4-Pin female to 9-Pin DTE female cable is supplied with EVM to connect with the PC.

Table 3.24: UART Connectors Pin Out

Pin#	Signal Name
1	Detect
2	Ground
3	Transmit
4	Receive

3.2.25 J2, XDS200 mini USB connector

J2 is a 5-pin Mini-USB connector to connect Code Composer Studio with SoC through on board XDS200 circuitry. Below table shows the pin outs of the Mini-USB connector.

Table 3.25: XDS200 mini USB Connector Pin Out

Pin#	Signal Name
1	XDS_USB_VBUS_IN
2	XDS_USB_DM
3	XDS_USB_DP
4	Ground
5	Ground

3.2.26 J3, XDS200 MCU JTAG Connector

J3 is the 20-pin JTAG connector for debugging of XDS200 processor (AM1802BZWTD3). The pin outs for this connector is shown in below table:

Table 3.26: XDS200 MCU JTAG Connector Pin Out

Pin#	Signal Name	Pin#	Signal Name
1	DBG_TMS	2	DBG_TRSTn
3	DBG_TDI	4	Ground
5	EMU_TVD	6	NC
7	DBG_TDO	8	Ground
9	DBG_RTCK	10	Ground
11	DBG_TCK	12	Ground
13	NC	14	NC

15	DBG_SRST	16	NC
17	NC	18	NC
19	NC	20	NC

3.2.27 J4, USB3.0 TypeA Connector

J4 is 9-pin USB3.0 typeA connector for the USB host interface. Pin out for this connector is shown in the table below:

Table 3.27: USB3.0 Connector Pin Out

Pin#	Signal Name
1	VBUS
2	D-
3	D+
4	GND
5	SSRX-
6	SSRX+
7	GND
8	SSTX-
9	SSTX+

3.2.28 J6, Mini-USB Connector for UART Console

J6 is a 5-pin Mini-USB connector to connect Code Composer Studio with SoC/BMC using UART Console type on-board emulation circuitry. Below table shows the pin outs of this Mini-USB connector.

Table 3.28: Mini USB Connector Pin Out

Pin#	Signal Name
1	USB_VBUS_IN
2	D-
3	D+
4	NC
5	Ground

3.2.29 PMBUS1, PMBUS for Smart-Reflex connected to UCD9090

PMBUS is programming connector for configuring the power sequence controller chip UCD9090 which controls power sequence of all on board supplies.

Table 3.29: PMBUS Connector Pin Out

Pin#	Signal Name
1	PMBUS_CLK
2	PMBUS_DAT
3	PMBUS_ALT
4	PMBUS_CTL
5	GND

3.2.30 SIM1, USIM Connector

SIM1 is a 8-pin SIM Card connector for Universal Subscriber Identity Module (USIM) interface. The USIM is compatible with ISO, ETSI/GSM, and 3GPP standards. The pin out for the connector is shown in the table below:

Table 3.30: USIM Connector Pin Out

Pin#	Signal Name
C1	SIM_VCC
C2	SIM_RST
C3	SIM_CLK
C5	GND
C6	NC
C7	SIM_IO
SW1	VCC1V8
SW2	SIM_EN

3.3 DIP and Push Button Switches

The TCIEVMK2LX EVM has 3 push button switches, one Jumper header and one sliding actuator DIP switches. The PRW, ATT and MCU_RESET are push button switches; CN8 is Jumper header while SW1is DIP switch. The function of each of the switches is listed in the table below:

The function of each of the switches is listed in the table below:

Table 3.31: TCIEVMK2LX EVM Board Switches

Switch	Function
PWR	Full Reset Event
MCU_RESET	MCU Reset Event
ATT	Warm Reset Event
CN8	MCU Wake Event
SW1	SoC Boot mode Configuration

3.3.1 PWR, Full Reset Event

Pressing the PWR button performs different functions based on how many times the button is pressed. The button must be pressed again within 0.5 seconds for it to register as a sequential click:

1 press: Graceful Shutdown

2 presses: Warm Reset

3 presses: Full Reset

4 presses: Cancel action

If the button is pressed and held for longer than 3 seconds, the board will be forcefully shutdown.

3.3.2 MCU_RST, MCU Reset Event

Pressing the MCU_RESET button switch will issue a RST# to the BMC. It'll reset BMC and other peripherals.

3.3.3 ATT, Warm Reset

Not currently implemented.

3.3.4 CN10, Wake

The button is reserved for future use.

3.3.5 SW1, SoC Boot mode Configurations

SW1 are 4 position DIP switches, which is used for DSP Boot Device, Boot Configuration,

For the details about the SoC Boot modes and their configuration, please refer to the SoC Data Manual.

The diagram for the DSP no-boot setting on these switches shown below:

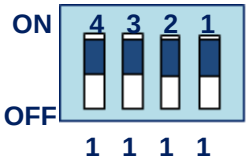


Figure 3.4: SW1 DSP No-Boot Setting

The following table describes the position and corresponding functions on SW1.

Table 3.32: SW1, Boot mode configuration Switch

DIP Switch (p4, p3, p2, p1)	Boot mode Selected
0000	ARM NAND
0001	DSP No Boot
0010	ARM SPI
0011	ARM I2C
0100	ARM UART
0101	ARM RBL ETHERNET
0110	SLEEP WITH MAX PLL & ARM BYPASS
0111	SLEEP WITH MAX PLL
1000	DSP NAND
1001	SLEEP W/ SLOW PLL & ARM BYPASS
1010	DSP SPI
1011	DSP I2C
1100	DSP UART
1101	DSP RBL ETHERNET
1110	SLEEP WITH SLOW PLL & SLOW ARM PLL
1111	DSP No Boot

For more information and options on boot modes please visit:
http://processors.wiki.ti.com/index.php/EVMK2L_Hardware_Setup

3.4 Test Points

The TCIEVMK2LX EVM Board has 81 test points. The position of each test point is shown in the figure below:

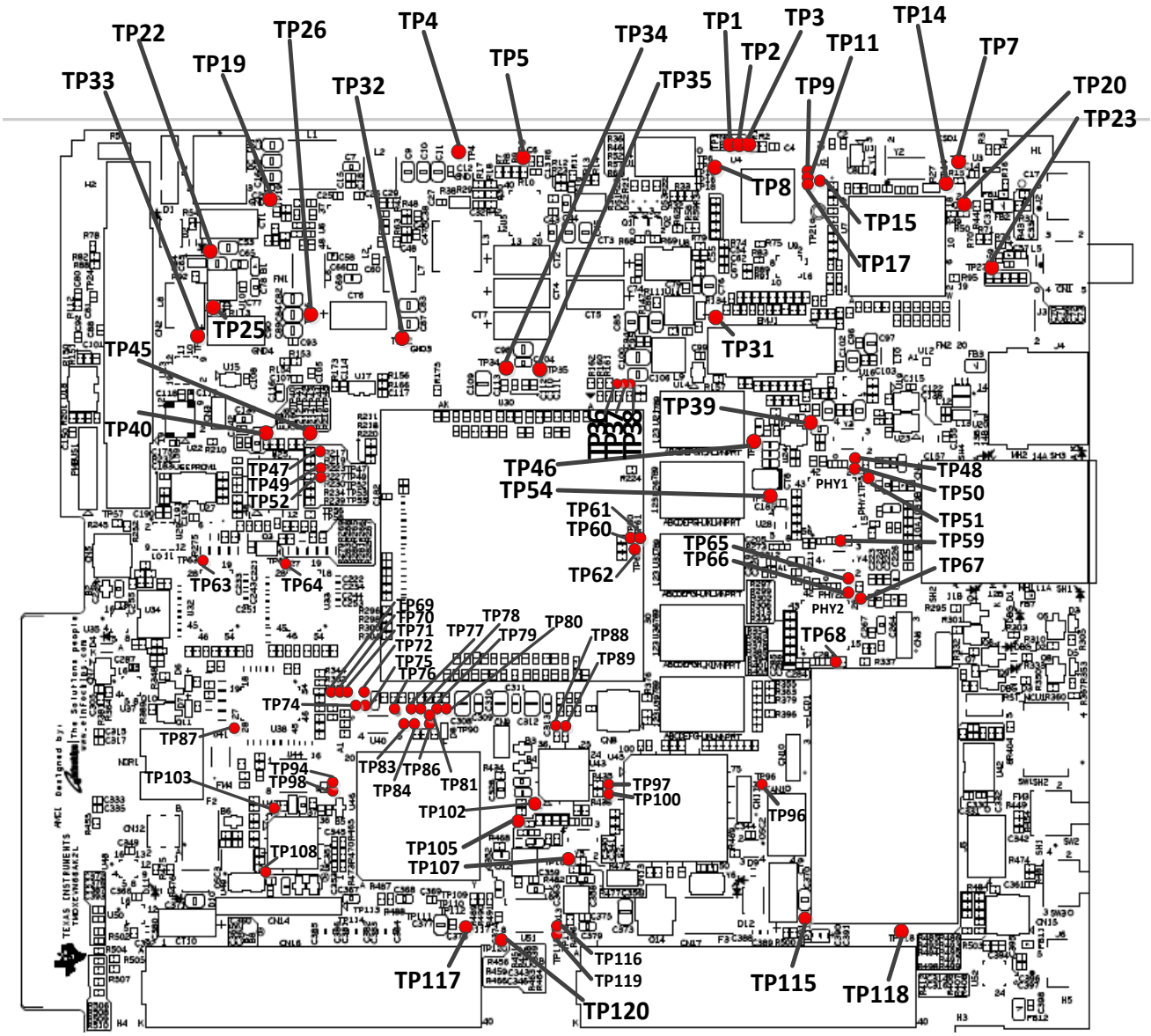


Figure 3.5: Board Test Points (Top)

Table 3.33: TCIEVMK2LX EVM Board Test Points

Test Points	Signal
TP1	XDS_SPARE0
TP2	XDS_SPARE1
TP3	XDS_T_TDIS
TP4	VCC0V85
TP5	TA_PGOOD
TP7	XDS_CLK_OUT
TP8	XDS_CPLD_TDO
TP9	XDS_CPLD_TCK
TP11	XDS_CPLD_TMS
TP14	XDS_VPP
TP15	XDS_VCC3V3
TP17	XDS_CPLD_TDI
TP19	VCC5
TP20	XDS_VCC3V3
TP22	VCC12
TP23	GPS_TCXO_CLK
TP25	VCC3_AUX_PGOOD
TP26	CVDD1
TP31	VDD_DDR_PGOOD
TP32	VCC1V8
TP33	VCC3V3_AUX
TP34	CVDD
TP35	Ground
TP36	SOC_THERMDIODE_A1
TP37	SOC_THERMDIODE_C1
TP38	SOC_PMCSENSE0
TP39	VCC0V75_PGOOD
TP40	UCD_TRST#
TP45	SOC_POWER_GOOD
TP46	VDD_DDR
TP47	MAIN_POWER_GOOD
TP48	PHY1_HSDAC_P
TP49	SOC_POWER_START_R
TP50	PHY1_HSDAC_N
TP51	PHY1_TSTPT
TP52	MAIN_POWER_START_R
TP54	VTT_DDR3A

TP59	PHY1_CLK125
TP60	SOC_DDR3ADTO0
TP61	SOC_DDR3AATO
TP62	SOC_DDR3ADTO1
TP63	ALL_DONE#_SW1
TP64	ALL_DONE#_SW3
TP65	PHY2_HSDAC_P
TP66	PHY2_HSDAC_N
TP67	PHY2_TSTPT
TP68	PHY2_CLK125
TP69	SYSCLKOUT_SOC
TP70	DDR3APLLOBSCLKN
TP71	DDR3APLLOBSCLKP
TP72	SOC_SPI0SCS3
TP74	SOC_SPI0SCS4
TP75	SOC_SPI0SCS2
TP76	SOC_VSSTMON
TP77	SOC_SPI0SCS1
TP78	SOC_VDDTMON
TP79	SOC_THERMDIODE_A2
TP80	SOC_THERMDIODE_C2
TP81	FPGA_DIFF_TP1_P
TP83	FPGA_TP1
TP84	FPGA_TP2
TP86	FPGA_DIFF_TP1_N
TP87	ALL_DONE#_SW2
TP88	CDCM2_Y6_N
TP89	CDCM2_Y6_P
TP94	LVDS_BUFF_4Y
TP96	MCU_U1TX
TP97	CDCM2_Y0_N
TP98	LVDS_BUFF_4Z
TP100	CDCM2_Y0_P
TP102	CDCM2_STATUS1
TP103	CDCM1_STATUS1
TP105	VCC_1V8_FPGA
TP107	VCC_1V2_FPGA
TP108	DAC_VOUT
TP115	12VIN_FMC2
TP116	LVDS_BUFF2_4Y
TP117	12VIN_FMC1

TP118	3V3_IN_FMC2
TP119	LVDS_BUFF2_4Z
TP120	3V3_IN_FMC1

3.5 System LEDs

The TCIEVMK2LX EVM board has ten LEDs. Their positions on the board are indicated in figure below. The description of each LED is listed in table below:

Table 3.34: TCIEVMK2LX EVM Board LEDs

LED#	Color	Description
D2	Green	12V DC adaptor input indication
D3	Red	Failure and Out of service status in AMC chassis
D6	Green	PLLLOCK LED
D5	Blue	Hot Swap status in AMC chassis
D7	Red	SoC RESETSTATZ
D9	Green	12V FMC2 Indication
D11	Green	12V FMC1 Indication
Dbg_D1	Red Green	SoC Debug LEDs
Dbg_D2	Blue	SoC Debug LEDs
DBG_D3	Blue	SoC Debug LEDs

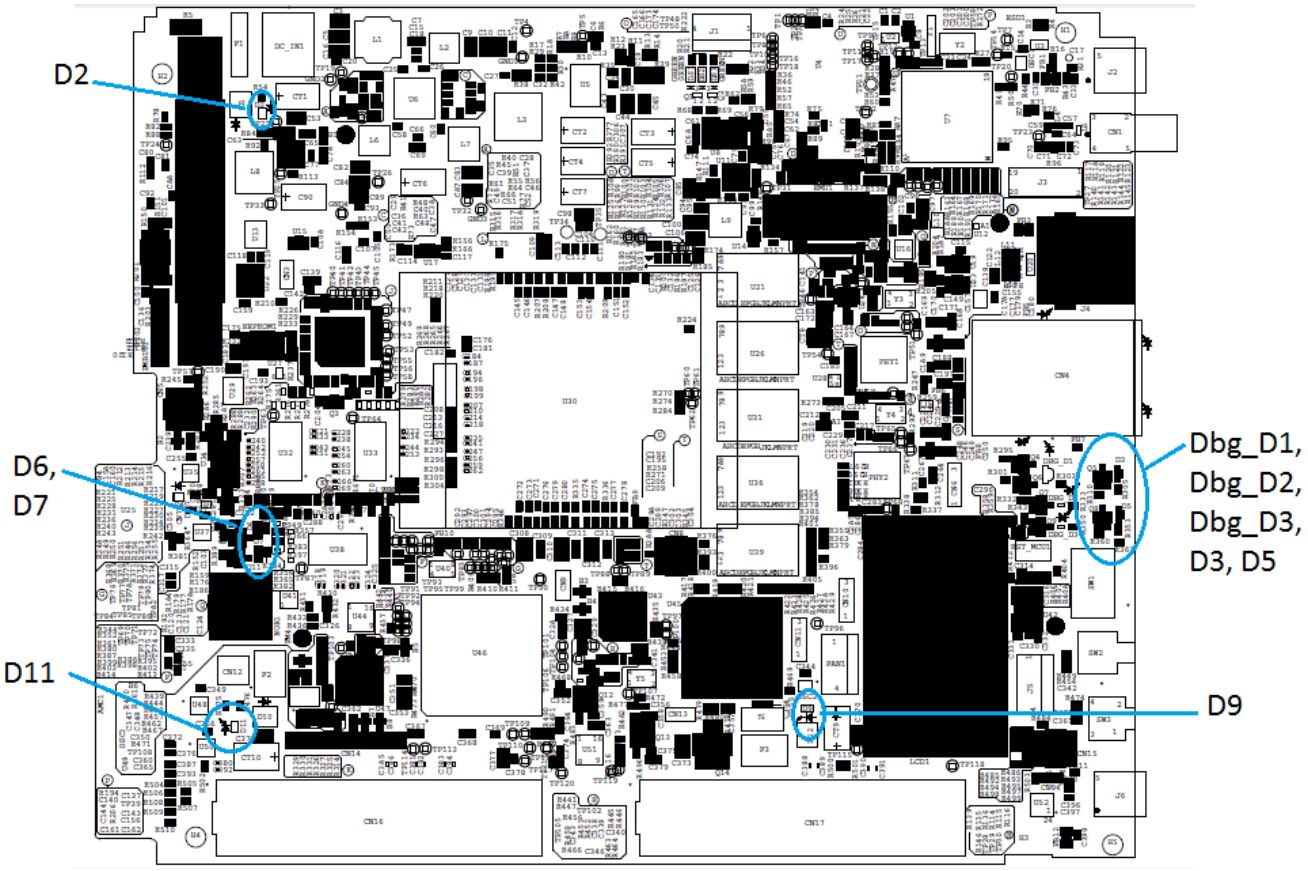


Figure 3.6: Board LEDs

4. TCIEVMK2LX EVM System Power Requirements

This chapter describes the power design of TCIEVMK2LX EVM board. It contains:

4.1 Power Requirements

Note that the power estimates stated in this section are maximum limits used in the design of the EVM. They have margin added to allow the EVM to support early silicon samples that normally have higher power consumption than eventual production units.

The maximum EVM power requirements are estimated to be:

- TCI6630K2L – 25.912W
- Two FMC Connector – 18W
- MT41K256M16HA125:E (DDR3) – 5.250W
- LM3S2D93 (BMC) – 0.445W
- Ethernet – 1.065W
- NAND Flash – 0.072W
- NOR Flash – 0.036W
- LCD – 0.135W
- Clock Generator – 2.098W
- XDS200 circuitry – 0.680W
- SIM translator – 0.174W
- UART to USB Converter – 0.148W
- FPGA – 1.952W
- GPS – 0.149W
- USB3.0 connector – 4.500W
- SERDES Switches – 2.732W
- FAN – 1.200W
- Power Sequence Circuit – 0.198W
- Others – 2.070W

Total EVM Board Consumption is 83.81W approx. Hence, the selected AC/DC 12V adapter should be rated for a minimum of 84 Watts.

Table 4.1: Current Consumption on Each Voltage Rail

Device	Net Name	Voltage Rail	Current	Qty	Power Usage		Description
Input	VCC3V3_MP	+3.3V					BMC Management Power
	VCC12	+12V					Payload Power to AMC
TCI6630K2L	CVDD	+1.0V	18.8A	1	18.8W	25.912	SoC Core variable Power
	CVDD1	+0.95V	2.9A		2.755 W		Core fixed Power

	VCC0V85	+0.85V	1.5A		1.275 W		USB LV and SERDES analog Power
	VDD_DDR	+1.5V	0.8A		1.2W		DDR3 I/O of SoC and DDR3 Power
	VCC1V8	+1.8V	1A		1.8W		SerDes I/O, Core PLL, DDR3 DLL Power
	VCC3V3_AUX	+3.3V	0.025A		0.082 5W		FPGA I/O and other on board circuit Power
AFE7500EVM Card	VCC12	+12V	1.5A	2	18W	18W	AFE7500EVM Power
DDR3 Memory	VDD_DDR	+1.5V	3A	5	4.5W	5.25W	DDR3 RAM Power
	VCCA0V75REF	0.75V	1A		0.75W		DDR3 Termination Power
BMC Microcontroller	VCC3V3_MP	+3.3V	0.135A	1	0.445 W	0.445 W	BMC Power
Ethernet Devices	VCC2V5	+2.5V	0.426A	2	1.065 W	1.065 W	Ethernet Power
NAND Flash	VCC1V8	+1.8V	0.04A	1	0.072 W	0.072 W	NAND Flash Power
NOR Flash	VCC1V8	+1.8V	0.02A	1	0.036 W	0.036 W	NOR Flash Power
LCD Display	VCC3_LCD	+3V	0.045A	1	0.135 W	0.135 W	LCD Power
Clock Generator	VCC3V3_MP	+3.3V	0.636A	2	2.098 W	2.098 W	Clock Gen Power
XDS200 Circuit	VCC5	+5V	0.136A	1	0.68W	0.68W	XDS Power
SIM Translator	VCC1V8	+1.8V	0.005A	1	0.009 W	0.174 W	USIM Power
	VCC3V3_AUX	+3.3V	0.05A		0.165 W		USIM Power
USB to Dual UART	VCC3V3_AUX	+3.3V	0.045A	1	0.148 W	0.148 W	USB to UART Power
FPGA	VCC_1V2_FPGA	+1.2V	0.09A	1	0.108 W	1.952 W	Core Power
	VCC_1V8_FPGA	+1.8V	0.275A		0.495 W		I/O Power
	VCC3V3_AUX	+3.3V	0.409A		1.349 W		I/O Power
GPS Receiver	VCC1V8	+1.8V	0.083A	1	0.149 W	0.149 W	GPS Power
USB3.0	VCC5	+5V	0.9A	1	4.5W	4.5W	USB3.0 Power
SERDES Switches	VCC3V3_AUX	+3.3V	0.621A	3	2.049 W	2.049 W	SERDES Switch Power
FAN	VCC12	+12V	0.1A	1	1.2W	1.2W	FAN Power
Power Sequence Controller	VCC3V3_MP	+3.3V	0.06A	1	0.198 W	0.198 W	UCD9090 Power
Others	VCC3V3_AUX	+3.3V	0.3A		2.07W	2.07W	Misc Power

Approx Power Consumption for TI_EVM -Lamarr

Components Part No.	Description	Quantity Per Board	Current Consumed by corresponding device on power supply (mA)													Total Power (mW)
			0.75	0.85 Analog	0.85 USB	0.95 Fixed DSP+ARM	1 AVS(DSP+ARM)	1.2	1.5	1.8 Digital	1.8 Analog	3	3.3	5	12	
Marconi Connector	2 Nos of Marconi EVM	2													1500	18000
Lammar (K2L) Part	TI- Multicore DSP with ARM Core	1		700	800	2900	18800		800	400	600		25			25912.5
MT41K256M16HA125:E	IC. DDR3. 4Gb (256Mx16)	5	1000						3000							5250
LM3S2D93	Microcontroller	1											135			445.5
88E1512	Gigabit ethernet phy	2											426			1405.8
MT29F16G16ADBCA	Nand Flash	1								40						72
N25Q128A11ESF40F	SPI NOR	1								20						36
LCD	LCD display	1										45				135
CDCM6208	Reference Clock generator	2											636			2098.8
MCP23S17T-E/SS	IC I/O EXPANDER SPI 16B 28SSOP	5								16			4			42
XDS200 circuitry (referred from K@E)	XDS200 circuitry	1												136		680
TXS4555RGTR	SIM translaor	1								5			50			174
CP2105	IC USB to DUAL UART	1											45			148.5
XC3S400AN-4FGG400C	IC SPARTAN 3AN FGG400 FPGA	1						90		275			409			1952.7
TC6000G	GPS Receiver	1								83						149.4
USB3.0 connector	USB 3.0	1												900		4500
DS100MB203SQE/NOPB	JESD and PCIe switch	4											828			2732.4
FAN		1													100	1200
UCD9090		1											60			198
Others	Other Ics	1								600			300			2070
Total Current on individual power supply (mA)			1000	700	800	2900	18800	90	3800	1439	600	45	2918	1036	1600	
6.5% margin added over design (mA)			1065	745.5	852	3088.5	20022	95.85	4047	1532.535	639	47.925	3107.67	1103.34	1704	
Power Consumption in (mW)			798.75	633.675	724.2	2934.075	20022	115.02	6070.5	2758.563	1150.2	143.775	10255.311	5516.7	20448	

TPS544C24 -- 12V to 1V regulation	1962.94
LM26430-1(SW1) -- 12V to 0.95V regulation	287.65
TLV1117-33CDCY -- 12V to 3.3V BMC (LDO) regulation	148.50
TPS54620 -- 12V to 1.5V regulation	751.76
LM26430-1(SW3) -- 12V to 0.85V Analog SoC regulation	62.13
TPS54620 -- 12V to 1.8V Analog regulation	112.76
TPS51200 -- 1.5 to 0.75V DDR regulation	1065.00
LM26430-1(SW4) -- 12V to 0.85V USB SoC regulation	71.00
LM26430-1(SW2) -- 12V to 1.8V Digital regulation	240.79
TPS54620 -- 12V to 3.3V Others regulation	1101.76
TPS54620 -- 12V to 5V regulation	540.85
APL431LBAI-TRG -- 3.3V to 3V regulation	47.93
LDO -- 3.3V OTH to 1.2V FPGA (LDO) - regulation	95.85
LDO -- 3.3V OTH to 1.8V FPGA (LDO) - regulation	302.50
Total Current @ 12V	6.98A
Total Power :	83.81W
Total Current @5V	1103.34
Total Current @3.3V	3155.60
Total Current @1.5V	5112.00

Note :
1) Above power consumption considers major block of design and provides indicative figure only.
2) Power rail assignment to different regulator is tentative based on power consumption, this can be changed based on sequence requirement.
3) Total power consumption is system is higher than AMC power(80W), we assume that marconi EVM will be connected only when board is running on external power supply.

Figure 4.1: TCIEVMK2LX EVM Power Consumption

Note: The power budget value used for this EVM is an early estimation and users should reference the power estimation tool for power budgeting specific to their application.

4.2 Power Supply Distribution

A high-level block diagram of the power supplies is shown in Figure 4.1. It is also shown in the schematic.

In Figure 4.1, the Auxiliary power rails are always on after payload power is supplied. These regulators support all control, sequencing, and boot logic. The Auxiliary Power rails contain:

- VCC3V3_AUX
- VCC_1V2_FPGA
- VCC_1V8_FPGA

The maximum allowable power is 83.81W from the external AC brick supply or from the 8 AMC header pins.

Individual control for each (remaining) voltage regulator is provided to allow flexibility in how the power planes are sequenced (Refer to section 4.3 for specific details). The goal of all power supply designs is to support the ambient temperature range of 0°C to 45°C.

The TCI6630K2L core power is supplied using dedicated high current switching regulator i.e. Top Avatar TPS544C24. This regulator can supply up to 30A load. The output voltage is controlled by point of load controller, smart reflex enabled, VID supported regulator LM10011. The TCI6630K2L supports a VID interface to enable

Smart-Reflex® power supply control for its primary core logic supply. Other SoC supply voltages are provided through other TI switching regulators.

The VCC3V3_AUX power rails are regulated by TI 6A Synchronous Step Down SWIFT™ Converters, TPS54620, to supply the peripherals and other power sources.

The EVM power topology is a combination of switching supplies and linear supplies. The linear supplies are used to save space for small loads. The switching supplies are implemented for larger loads. The switching supplies are listed below followed by explanations of critical component selection:

- CVDD (AVS core power for TCI6630K2L)
- CVDD1 (0.95V fixed core power for TCI6630K2L)
- VCC3V3_AUX (3.3V power for peripherals)
- VCC1V5 (1.5V DDR3 power for TCI6630K2L and DDR3 memories)
- VCC2V5 (2.5V Ethernet Power)
- VCC1V8 (1.8V for TCI6630K2L and other power)
- VCC0V85 (0.85V for TCI6630K2L)
- VCC5 (5.0V power for USB and XDS200)

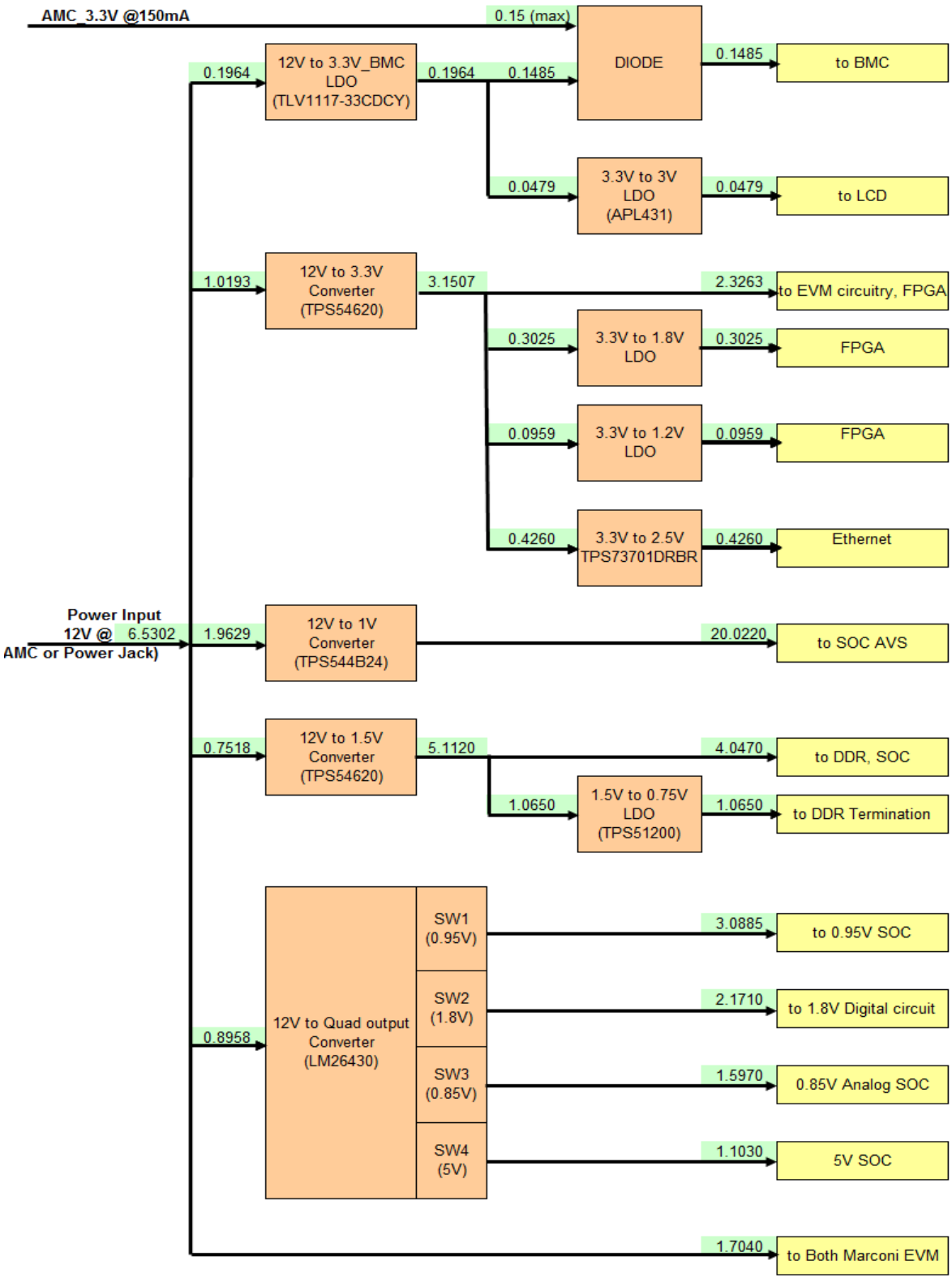


Figure 4.2: TCIEVMK2LX EVM Power Generation Topology

4.2.1 CVDD (1V) Design

The variable core power supply rail "**CVDD"** is regulated by "point of load controller" LM10011. The LM10011 is connected with TCI6630K2L's VID interface through which voltage can be controlled by SoC.

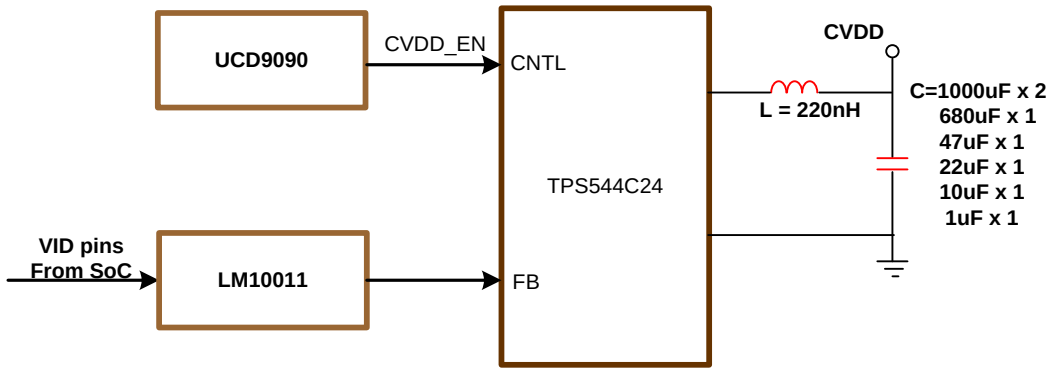
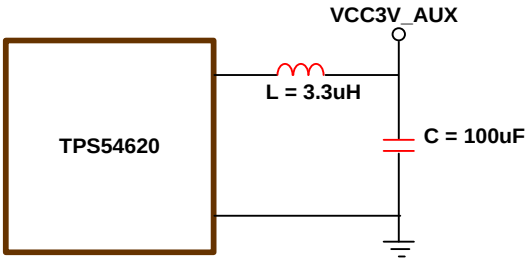


Figure 4.3: CVDD Design on TCIEVMK2LX EVM

CVDD Inductor Calculation	**CVDD Capacitor Calculation**
$L = ((V_{in(max)} - V_{out})/\Delta I_{out}) * V_{out}/(V_{in(max)} * F_{sw})$ = ((12.5 - 1/8) * (1 / (12.5 * 1MHz)) = (11.5/8) * (1/(12.5M)) = 1.4375 * 0.08u ≈ 115nH Reference Inductor = 220nH	$C = (\Delta I_{out}\text{^}2 * L) / (V_{out} * \Delta V_{out})$ = (10^2 * 220nH) / (1*10m) = 22000n / 10m = 2200 uF Total Caps connected = 2760uF

4.2.2 VCC3V3_AUX and VCC1V5 Design

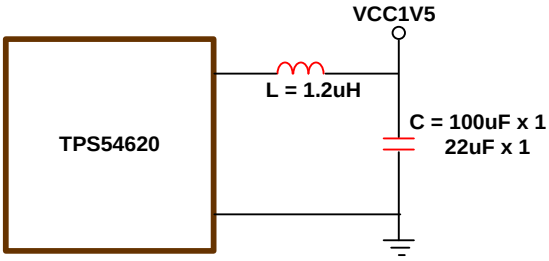
The **VCC3V3_AUX** and **VCC1V5** power rails are regulated by two TI 6A Synchronous Step Down SWIFT™ Converters, TPS54620, to supply the peripherals and other power sources and the SoC DDR3 EMIF and DDR3 memory chips respectively.



Over all tolerance 5%,
DC tolerance is 2.5%
K_{IND} = 0.3

Figure 4.4: VCC3V3_AUX Design on TCIEVMK2LX EVM

Output Capacitor Calculation	**Inductor Calculation**
$C_{out(min1)} = (2*\Delta I_{out}) / (F_{sw}*\Delta V_{out})$ $= (2*3.5) / (840kHz*0.0825)$ $\approx 110.58uF$ Reference Capacitor = 100uF	$L = ((V_{in(max)} - V_{out})/(I_{out} * K_{ind})) * (V_{out}/(V_{in(max)} * F_{sw}))$ $= ((12.5 - 3.3)/(3.5 * 0.3) * (3.3 / (12.5 * 840kHz))$ $= ((9.2/(3.5 * 0.3) * (3.3 / (10.5M))$ $= (8.76) * (0.31u)$ $\approx 2.75uH$ Reference Inductor = 3.3uH



Over all tolerance 5%,
DC tolerance is 2.5%
K_{IND} = 0.3

Figure 4.5: VCC1V5 Power Design on TCIEVMK2LX EVM

Output Capacitor Calculation	**Inductor Calculation**
$C_{out(min)} = (2*\Delta I_{out}) / (F_{sw}*\Delta V_{out})$ $= (2*1)/(700kHz*0.125)$ $\approx 22.8uF$ Reference Capacitor = 22uF	$L = ((V_{in(max)} - V_{out})/(I_{out} * K_{ind})) * (V_{out}/(V_{in(max)} * F_{sw}))$ $= ((12.5 - 1.5)/(4.5 * 0.3)) * (1.5 / (12.5*700kHz))$ $= (11/1.35) * (1.5 / (8.75M))$ $= (8.14) * (0.171u)$ $\approx 1.39uH$ Reference Inductor = 1.2uH

4.3 Power Supply Boot Sequence

Specific power supply and clock timing sequences are identified below. The TCI6630K2L SoC requires specific power up and power down sequencing. Figure 4.2 and Figure 4.3 illustrate the proper boot up and down sequence. Table 4.3 provides specific timing details for Figure 4.6 and Figure 4.7.

Refer to the Keystone 2 SoC Data Manual for confirmation of specific sequencing and timing requirements.

Table 4.2: Power-up and down timing on TCIEVMK2LX EVM

Step	Power Rails	Timing	Description
	Power-Up		
1	VCC12 (AMC Payload power), VCC3V3_MP_ALT, VCC3_LCD,	Auto	When the 12V power is supplied to the EVM, the VCC3V3_MP supplies to the MCU and UCD9090 power will turn on. The 3V supplies to the LCD power will turn on.
2	VCC3V3_AUX, VCC_1V2_FPGA VCC_1V8_FPGA	0ms	VCC3V3_AUX would be turned on first and 1.8V and 1.2V supplies to FPGA will turn on. FPGA outputs to DSP will be locked (held at ground).
3	CVDD (SoC AVS core power)	15ms	Enable CVDD (UCD9090 power rail#1) after 3.3V AUX is stable for 15ms.
4	CVDD1 (SoC CVDD1 fixed core power)	5ms	Enable CVDD1 (UCD9090 power rail#5) 5ms after CVDD has stabilized.
5	VCC0V85	5ms	Turn on VCC0V85 (UCD9090 power rail#2) after CVDD1 is stable for 5ms.
6	VCC1V8	5ms	Turn on VCC1V8 (UCD9090 power rail#6) after VCC0V85 is stable for 5ms.
7	VCC1V5 (DDR3 power)	5ms	Turn on VCC1V5 (UCD9090 power rail#11) after VCC1V8 is stable for 5ms.
8	VCC0V75	5ms	Turn on VCC0V75 (UCD9090 power rail#9) after VCC1V5 is stable for 5ms.
9	VDD3V3	5ms	Turn on VDD3V3 (UCD9090 power rail#12) after VCC0V75 is stable for 5ms.
10	VCC5V	5ms	Turn on VCC5V (UCD9090 power rail#3) after VDD3V3 is stable for 5ms.
11	CDCM6208#1/#2 Initialization BMC Output	5ms	Initialize the CDCE6208s after VCC5 stable for 5mS. De-assert CDCM6208 power down pins (PD#), initialize the CDCM6208s.
12	RESETz Other reset and NMI pins	18ms	De-asserted RESETz and unlock other reset and NMI pins for the SoC after SOC_Power_GOOD stable and CDCE6208s PLLs locked for 5mS. In the meanwhile, the MCU will driving the boot configurations to the SoC GPIO pins.
13	PORz	5ms	De-asserts PORz after RESETz is de-asserted for 5ms.
14	RESETFULLz	5ms	De-asserts RESETFULLz after PORz is de-asserted for 5ms.
15	SoC GPIO pins for boot configurations	1ms	Releases SoC GPIO pins after RESETFULLz is de-asserted for 1ms
	Power-Down		
13	RESETFULLz	0ms	If there is a power failure or AMC payload

	PORz		is powered off, BMC will assert RESETFULLz and PORz signals to SoC.
14	BMC 3.3V outputs CDCM6208 PD# pins	5ms	Locked 3.3V output pins on the BMC and pull the CDCM6208 PD# pins to low to disable SoC clocks.
15	VCC3V3_AUX VCC_1V2_FPGA VCC_1V8_FPGA VCC2V5 CVDD CVDD1 VCC0V85 VDD3V3 VCC1V8 VCC1V5 VCC0V75 VCC5	0ms	Turns off all main power rails.

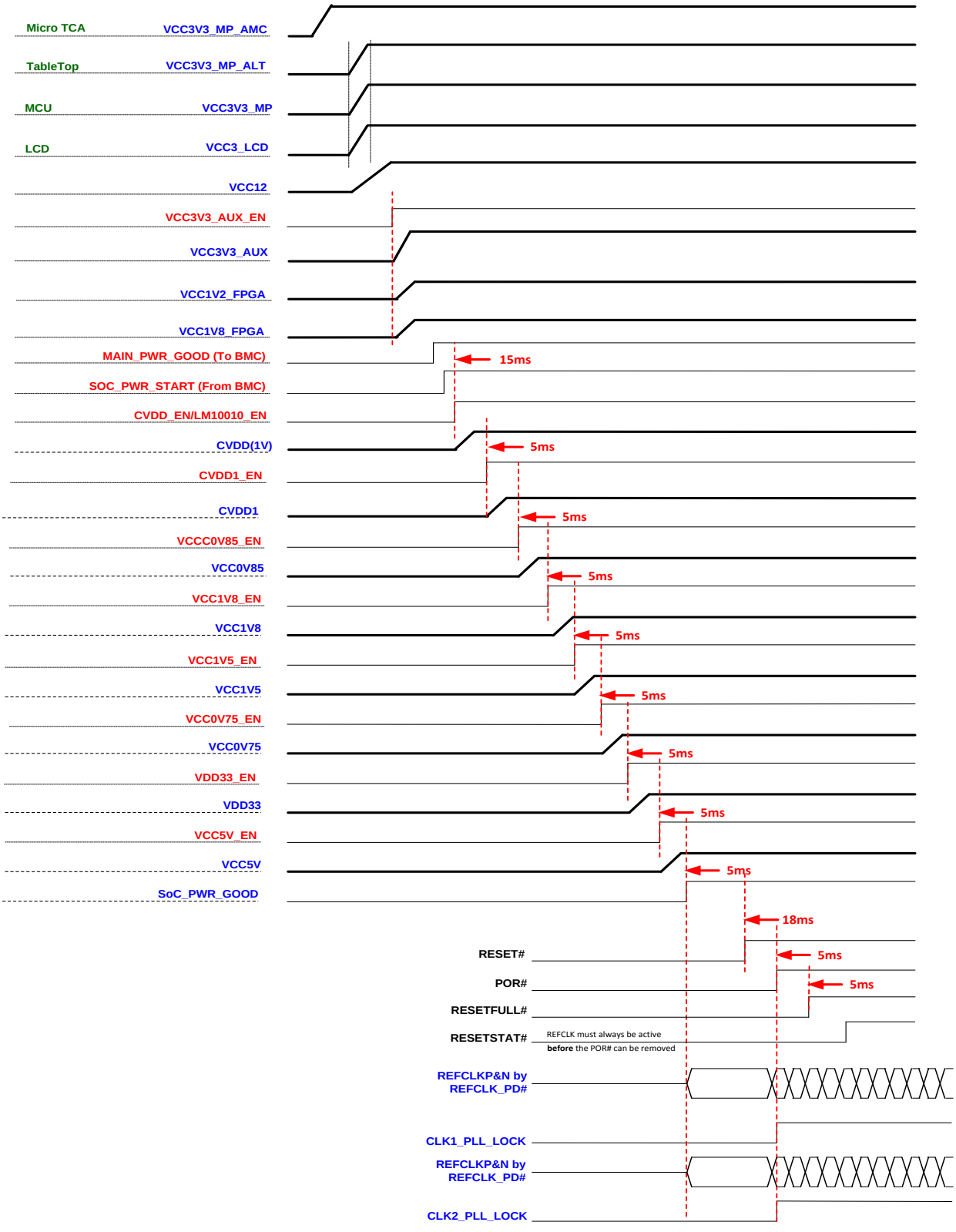


Figure 4.6: Initial Power up Sequence Timing Diagram

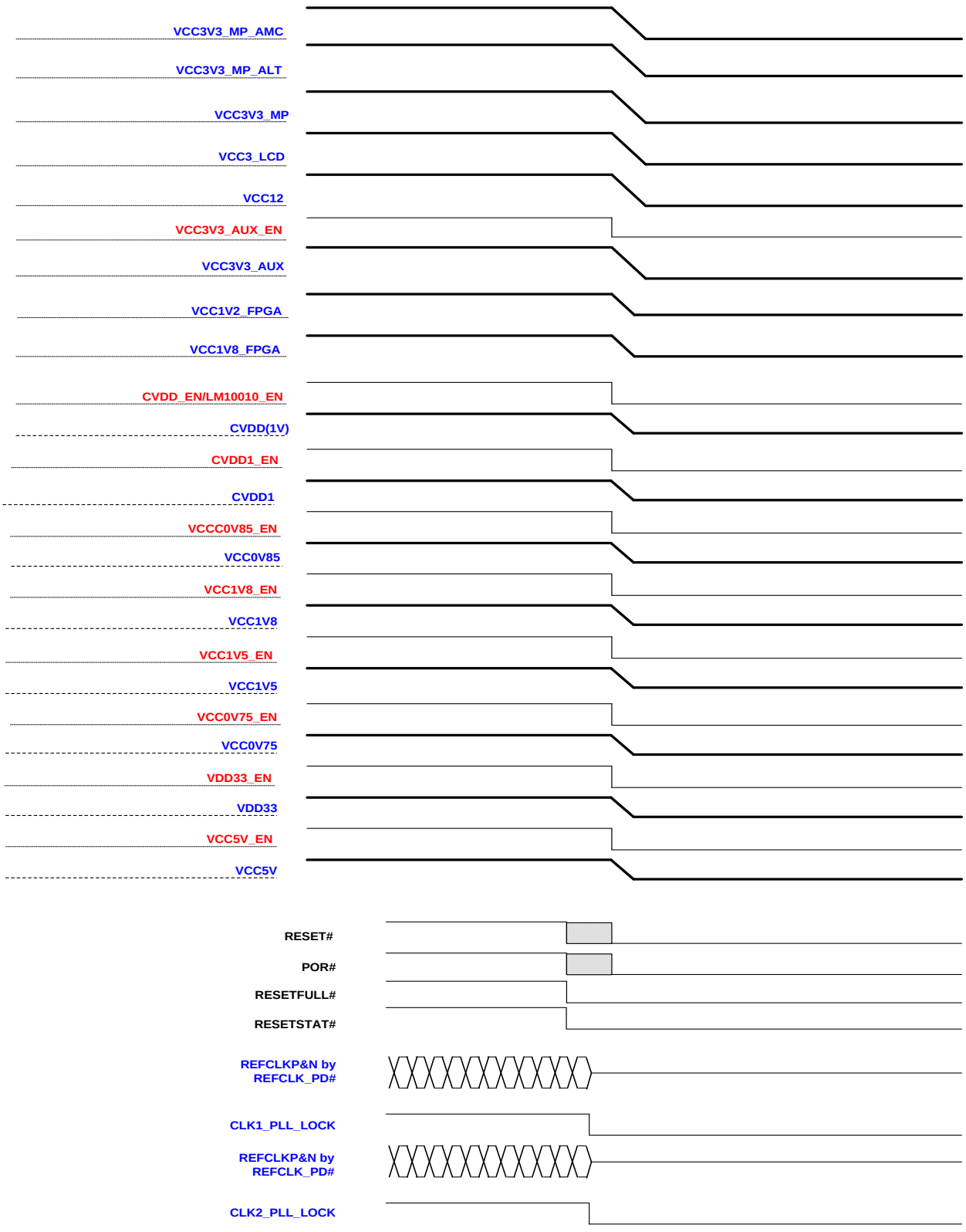


Figure 4.7: Power down Sequence Timing Diagram

5. TCIEVMK2LX FPGA Functional Description

This chapter describes the FPGA Functionality of TCIEVMK2LX EVM board. It contains:

5.1 FPGA Overview

FPGA plays a key role in interfacing of AFE7500EVM card. Five GPIO expanders (each 16bit width) have been implemented inside FPGA to save the board space.

The key functionalities of TCIEVMK2LX EVM FPGA are:

- FPGA provides glue logic interface for two AFE7500EVM card
- It generates system reference signal for both AFE7500EVM card
- It provides five GPIO expanders which are controllable by BMC
- It provides logic for controlling timer pins and two boot mode pin

5.2 FPGA Signal Description

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The following notations are used to describe the signal and type.

Table 5.1: Pin Type Notation Interpretation

Pin Type	Function
I	Input Pin
O	Output Pin
I/O	Bidirectional Pin
Differential	Differential Pair Pins
PU	Internal Pull-Up
PD	Internal Pull-Down

Table 5.2: TCIEVMK2LX EVM FPGA Pin Description

Pin Name	IO Type	Description
EXT_SWITCH_IN1_1V8	I	**EXT_SWITCH_IN1_1V8:** This is a General Purpose Input from external switch. It is reserved for future purpose if needed.

EXT_SWITCH_IN2_1V8	I	**EXT_SWITCH_IN2_1V8:** This is a General Purpose Input from external switch. It is reserved for future purpose if needed.
FPGA_CLK [P/N]	I, Diff	**FPGA_CLK Differential Clock input pairs:** 122.88MHz input is the main clock source for FPAG from external clock generator
SYSREF_DIVCLK [P/N]	I, Diff	**SYSREF_DIVCLK Differential Clock input pairs:** 122.88MHz input used for generating reference signal for AFE7500EVM card
GPIO_3_TCON_FPGA_1V8	O	**GPIO_3_TCON_FPGA_1V8:** This is a General Purpose test output to external header. It is reserved for future purpose if needed.
GPIO_4_TCON_FPGA_1V8	O	**GPIO_3_TCON_FPGA_1V8:** This is a General Purpose test output to external header. It is reserved for future purpose if needed.
GPIO_5_TCON_FPGA_1V8	O	**GPIO_5_TCON_FPGA_1V8:** This is a General Purpose test output to external header. It is reserved for future purpose if needed.
GPIO_0_TCON_FPGA_3V3	O	**GPIO_0_TCON_FPGA_3V3:** This is a General Purpose test output to external header. It is reserved for future purpose if needed.
GPIO_1_TCON_FPGA_3V3	O	**GPIO_1_TCON_FPGA_3V3:** This is a General Purpose test output to external header. It is reserved for future purpose if needed.
GPIO_2_TCON_FPGA_3V3	O	**GPIO_2_TCON_FPGA_3V3:** This is a General Purpose test output to external header. It is reserved for future purpose if needed.
SYSREFREQ_TCON_FPGA_3V3	O	**SYSREFREQ_TCON_FPGA_3V3:** This is a General Purpose test output to external header. It is reserved for future purpose if needed.
TDD_TIME_SYNC_3V3_TIMINGCON	O	**TDD_TIME_SYNC_3V3_TIMINGCON:** This is a General Purpose test output to external header. It is reserved for future purpose if needed.
DLSYNC_3V3_TIMINGCON	O	**DLSYNC_3V3_TIMINGCON:** This is a General Purpose test output to external header. It is reserved for future purpose if needed.
SOC_SPI1_CLK	I	**SOC SPI1 Serial Clock:** This signal is connected to FPGA as input. It is SPI1 clock input from SoC to FPGA.
SOC_SPI1_MISO	O	**SOC SPI1 Serial Data MISO:** This signal is connected to FPGA as output. It is a SPI1 data output from FPGA to SoC.

SOC_SPI1_MOSI	I	**SOC SPI1 Serial Data MOSI:** This signal is connected to FPGA as input. It is SPI1 data output from SoC to FPGA
SOC_SPI1SCS1	I	**SOC SPI1 Chip Select:** This signal is connected to FPGA as input. It is chips select1 from SoC to FPGA
SOC_SPI1SCS2	I	**SOC SPI1 Chip Select:** This signal is connected to FPGA as input. It is chips select2 from SoC to FPGA
SPI_CLK_FMC1_FPGA_1V8	O	**FMC1 SPI Serial Clock:** This signal is connected to FMC1 connector. It is FMC1 SPI clock from FPGA to FMC1 connector.
SPI_MOSI_FMC1_FPGA_1V8	O	**FMC1 Serial Data MOSI:** This signal is connected to FMC1 connector. It is SPI data output from FPGA to FMC1.
SPI_MISO_FMC1_FPGA_1V8	I	**FMC1 SPI Serial Data MISO:** This signal is connected to FMC1. It is a SPI data output from FMC1 to FPGA.
SPI_CLK_LMK_FMC1_FPGA_1V8	O	**FMC1 LMK SPI Serial Clock:** This signal is connected to FMC1 connector. It is LMK chip clock from FPGA to FMC1 connector.
SPI_MOSI_LMK_FMC1_FPGA_1V8	O	**FMC1 LMK SPI Serial Data MOSI:** This signal is connected to FMC1 connector. It is LMK data input from FPGA to FMC1.
SPI_MISO/RST_LMK_FMC1_FPGA_1V8	I/O	**FMC1 LMK SPI Serial Data MISO:** This signal is connected to FMC1. It is a LMK data output from FMC1 to FPGA.
SPI_CLK_FMC2_FPGA_1V8	O	**FMC2 SPI Serial Clock:** This signal is connected to FMC2 connector. It is FMC2 clock from FPGA to FMC2 connector.
SPI_MOSI_FMC2_FPGA_1V8	O	**FMC2 Serial Data MOSI:** This signal is connected to FMC2 connector. It is SPI data output from FPGA to FMC2.
SPI_MISO_FMC2_FPGA_1V8	I	**FMC2 SPI Serial Data MISO:** This signal is connected to FMC2. It is a SPI data output from FMC2 to FPGA.
SPI_CLK_LMK_FMC2_FPGA_1V8	O	**FMC2 LMK SPI Serial Clock:** This signal is connected to FMC2 connector. It is LMK chip clock from FPGA to FMC2 connector.
SPI_MOSI_LMK_FMC2_FPGA_1V8	O	**FMC2 LMK SPI Serial Data MOSI:** This signal is connected to FMC2 connector. It is LMK data input from FPGA to FMC1.
SPI_MISO/RST_LMK_FMC2_FPGA_1V8	I/O	**FMC2 LMK SPI Serial Data MISO:** This signal is connected to FMC2. It is a LMK data output from FMC2 to FPGA.
SPI_CS0_FMC1_FPGA_1V8	O	**FMC1 SPI Chip Select:** This signal is connected to FMC1. It is chips select from FPGA to FMC1.
SPI_CS1_LMK_FMC1_FPGA_1V8	O	**FMC1 LMK SPI Chip Select:** This signal is connected to FMC1. It is LMK chips select from FPGA to FMC1.

SPI_CS2_FMC2_FPGA_1V8	O	**FMC2 SPI Chip Select:** This signal is connected to FMC2. It is chips select from FPGA to FMC2.
SPI_CS3_LMK_FMC2_FPGA_1V8	O	**FMC2 LMK SPI Chip Select:** This signal is connected to FMC2. It is LMK chips select from FPGA to FMC2.
SOC_TSSYNCEVT	I	**SOC_TSSYNCEVT:** This signal comes from SoC and connected to FPGA as input. It is reserved for future use.
SOC_TSCOMPOUT	I	**SOC_TSSYNCEVT:** This signal comes from SoC and connected to FPGA as input. It is reserved for future use.
SOC_EXTFRAMEEVENT	I	**SOC_TSSYNCEVT:** This signal comes from SoC and connected to FPGA as input. It is reserved for future use.
SOC_TSRXCLKOUT0 [P/N]	I, Diff	**SOC_TSRXCLKOUT0:** This differential signal comes from SoC and connected to FPGA as input. It is reserved for future use.
SYSREF_FPGA [P/N]	O	**SYSTEM REFERENCE:** This differential signal comes from FPGA and connected to external buffer. The output of this clock is 120KHz and it provides reference signal to AFE7500EVM card.
EVM_TS_SYNCEVT_FPGA_1V8	O	**EVM_TS_SYNCEVT_FPGA_1V8:** This signal comes from FPGA and connected to external header. It is reserved for future use.
EVM_TS_COMPOUT_FPGA_1V8	O	**EVM_TS_COMPOUT_FPGA_1V8:** This signal comes from FPGA and connected to external header. It is reserved for future use.
EVM_TS_EXTFRAMEEVT_FPGA_1V8	O	**EVM_TS_EXTFRAMEEVT_FPGA_1V8:** This signal comes from FPGA and connected to external header. It is reserved for future use.
SOC_DFE_GPIO[0..17]	I/O	**SOC DFE GPIO:** DFE GPIO signals comes from SoC and connected to FPGA. These DFE GPIOs are mapped to AFE7500EVM GPIO inside FPGA.
GPIO0_FMC1_FPGA [0 : 7]	I/O	**FMC1 GPIO0:** GPIO0 bank comes from FPGA and connected to FMC1 Connector.
GPIO1_1_FMC1_FPGA_1V8 / TX_CAP_ PULSE_FMC1	O	**FMC1 GPIO/TX CAP PULSE:** Indicates TX capture of AFE7500EVM card. On low to high transition on this pin identifies DL time and AFE7500EVM captures selected TX stream in its buffer.
GPIO1_2_FMC1_FPGA_1V8 / RX_ON_ PULSE_FMC1	O	**FMC1 GPIO/RX ON PULSE:** AFE7500EVM's TDD control signal where low to high transition is used to identify the start of UL cycle (Rx). It is also used to identify the end of the DL (Tx) cycle. AFE7500EVM PG2.0 this signal is modified and low to high is start of Rx, and a high to low is the end of the Rx UL cycle.
GPIO1_3_FMC1_FPGA_1V8 / TX_ON_ PULSE_FMC1	O	**FMC1 GPIO/TX ON PULSE:** AFE7500EVM's TDD control signal where low to high transition is used to identify the start of DL cycle (Tx). This signal is used differently for AFE7500EVM's PG2.0 where low to high

		transition is TxON, and high to low transition is TxOFF.
GPIO1_4_FMC1_FPGA_1V8 / RX_OFF_ PULSE_FMC1	O	**FMC1 GPIO/RX OFF PULSE:** AFE7500EVM's TDD control signal where low to high transition is used to identify the end of the UL (Rx) cycle. This signal is not used for AFE7500EVM's PG2.0.
GPIO1_5_FMC1_FPGA_3V3 (PAON)	O	**FMC1 GPIO/PAON:** It provides a timed event for TDD RF control to external equipment. It is a 3.3V signal to enable the power amplifier. It is used for slow drain modulation control.
GPIO1_6_FMC1_FPGA_3V3 (TXON)	O	**FMC1 GPIO/TXON:** It provides a timed event for TDD RF control to external equipment. It is a 3.3V signal to switch the Tx/Rx signal to RF antenna.
GPIO1_7_FMC1_FPGA_3V3 / RX_CAP_ PULSE_FMC1	O	**FMC1 GPIO/RX CAP PULSE:** Indicates RX capture of AFE7500EVM card. On low to high transition on this pin identifies UL time and AFE7500EVM captures selected RX stream in its buffer.
STATUS_FMC1_FPGA_1V8 [0 : 1]	I	**FMC1 STATUS:** These signals come from Marconi and are used to indicate AFE7500EVM operating condition.
GPDAC_FMC1_FPGA [0 : 7]	I/O	**FMC1 AFE7500EVM PG2.0 GPIO:** GPIO bank comes from FPGA and connected to FMC1 Connector. These GPIOs are used for AFE7500EVM PG2.0.
IRQ_FMC1_FPGA_3V3	O	**FMC1 INTERRUPT:** It is an active high interrupt input to Marconi. It is used for additional controls beyond SPI commands or directed GPIO commands.
BUSY#_FMC1_FPGA_1V8	I	**FMC1 BUSY:** It is an active low, indicates that AFE7500EVM is processing the last SPI operation.
RST#_FMC1_FPGA_1V8	O	**FMC1 RESET:** It is an active low Reset signal for AFE7500 chip.
GPIO0_FMC2_FPGA [0 : 7]	I/O	**FMC2 GPIO0:** GPIO0 bank comes from FPGA and connected to FMC2 Connector.
GPIO1_1_FMC2_FPGA_1V8 / TX_CAP_PULSE_FMC2	O	**FMC2 GPIO/TX CAP PULSE:** Indicates TX capture of AFE7500EVM card. On low to high transition on this pin identifies DL time and AFE7500EVM captures selected TX stream in its buffer.
GPIO1_2_FMC2_FPGA_1V8 / RX_ON_PULSE_FMC2	O	**FMC2 GPIO/RX ON PULSE:** AFE7500EVM's TDD control signal where low to high transition is used to identify the start of UL cycle (Rx). It is also used to identify the end of the DL (Tx) cycle. AFE7500EVM PG2.0 this signal is modified and low to high is start of Rx, and a high to low is the end of the Rx UL cycle.
GPIO1_3_FMC2_FPGA_1V8 / TX_ON_PULSE_FMC2	O	**FMC2 GPIO/TX ON PULSE:** AFE7500EVM's TDD control signal where low to high transition is used to identify the start of DL cycle (Tx). This signal is used differently for AFE7500EVM's PG2.0 where low to high transition is TxON, and high to low transition is TxOFF.
GPIO1_4_FMC2_FPGA_1V8 / RX_OFF_PULSE_FMC2	O	**FMC2 GPIO/RX OFF PULSE:** AFE7500EVM's TDD control signal where low to high transition is used to identify the end of the UL (Rx) cycle. This signal is not used for AFE7500EVM's PG2.0.
GPIO1_5_FMC2_FPGA_3V3 (PAON)	O	**FMC2 GPIO/PAON:** It provides a timed event for TDD RF control to external equipment. It is a 3.3V signal to enable the power amplifier. It is used for slow drain modulation control.

GPIO1_6_FMC2_FPGA_3V3 (TxON)	O	**FMC2 GPIO/TXON:** It provides a timed event for TDD RF control to external equipment. It is a 3.3V signal to switch the Tx/Rx signal to RF antenna.
GPIO1_7_FMC2_FPGA_3V3 / RX_CAP_PULSE_FMC2	O	**FMC2 GPIO/RX CAP PULSE:** Indicates RX capture of AFE7500EVM card. On low to high transition on this pin identifies UL time and AFE7500EVM captures selected RX stream in its buffer.
STATUS_FMC2_FPGA_1V8 [0 : 1]	I	**FMC2 STATUS:** These signals come from Marconi and are used to indicate AFE7500EVM operating condition.
GPDAC1_FMC2_FPGA_1V8 [0 : 7]	I/O	**FMC2 AFE7500EVM PG2.0 GPIO:** GPIO bank comes from FPGA and connected to FMC2 Connector. These GPIOs are used for AFE7500EVM PG2.0.
IRQ_FMC2_FPGA_3V3	O	**FMC2 INTERRUPT:** It is an active high interrupt input to Marconi. It is used for additional controls beyond SPI commands or directed GPIO commands.
BUSY#_FMC2_FPGA_1V8	I	**FMC2 BUSY:** It is an active low, indicates that AFE7500EVM is processing the last SPI operation.
RST#_FMC2_FPGA_1V8	O	**FMC2 RESET:** It is an active low Reset signal for AFE7500 chip.
SOC_TIMI0_FPGA_1V8	O	**SOC TIMI0:** This signal is the output of multiplexer implemented in FPGA, which provides selection between AMC_TIMO0 and EXP_TIMO0. It is connected to TIMI0_AVSIFSEL0 pin of SoC.
SOC_TIMI1_FPGA_1V8	O	**SOC TIMI0:** This signal is the output of multiplexer implemented in FPGA which provides selection between EXTFRAMEEVT and EXP_TIMO1. It is connected to timer input pin of SoC.
SOC_TIMO0_FPGA_1V8	I	**SOC TIMO0:** This signal is timer output from SoC and it is connected to FPGA as input signal. It is connected to expansion connector based on selection of internal register bit.
SOC_TIMO1_FPGA_1V8	I	**SOC TIMO1:** This signal is timer output from SoC and it is connected to FPGA as input signal. It is being sent to expansion connector based on status of internal register bit.
TIMO0_EVM_FPGA_1V8	O	**TIMO0 EVM:** This signal is output from FPGA and connected to AMC connector and Expansion connector.
TIMO1_EVM_FPGA_1V8	O	**TIMO1 EVM:** This signal is output from FPGA and connected to external header and Expansion connector.
AMC_TIMO0	I	**AMC TIMO0:** This signal comes from AMC connector and connected to FPGA as input.
EXP_TIMO0	I	**EXPANSION TIMO0:** This signal comes from expansion connector and connected to FPGA as input.
EXT_TIMO1	I	**EXTFRAMEEVT TIMO1:** This signal comes from SoC and connected to FPGA as input.

EXP_TIMO1	I	**EXPANSION TIMO1:** This signal comes from expansion connector and connected to FPGA as input.
BMC_SPI0_CLK_FPGA_3V3	I	**BMC SPI0 Serial Clock:** This signal is connected to FPGA as input. It is SPI0 clock input from BMC to FPGA
BMC_SPI0_MISO_FPGA_3V3	O	**BMC SPI0 Serial Data MISO:** This signal is output from FPGA. It is a SPI0 data output from FPGA to BMC.
BMC_SPI0_MOSI_FPGA_3V3	I	**BMC SPI0 Serial Data MOSI:** This signal is connected to FPGA as input. It is SPI0 data output from BMC to FPGA.
BMC_SPI0_CS0#_FPGA_3V3	I	**BMC SPI0 Chip Select:** This signal is connected to FPGA as input. It is chips select0 from BMC to FPGA. It is used for controlling various FPGA registers.
SOC_GPIO_FPGA_1V8_EXP2 [0 : 15]	I/O	**SOC GPIO:** Bidirectional GPIOs which comes from SoC and are connected to FPGA expander2. These GPIOs are accessible to BCM through SPI0 bus.
BMC_GPIOINT0_FPGA_1V8_EXP2	O	**EXPANDER2 INTERRUPT:** It is an interrupt to BMC controller if any activity occurs on any of expander2 16 GPIO lines.
NC	-	Reserved for future use
NC	-	Reserved for future use
BMC_GPS_EN_FPGA_1V8_EXP3	O	**EXPANDER3 GPS ENABLE:** This signal is output of GPIO expander3 and BMC SPI0 controls enable signals of GPS device on it.
SOC_VPPB_EN_FPGA_1V8_EXP3	O	**EXPANDER3 VPP ENABLE:** This signal is output of GPIO expander3 and BMC SPI0 controls VPP power supply of SoC through it.
SOC_GPIO_16_FPGA_1V8_EXP3	I/O	**EXPANDER3 SOC GPIO16:** Bidirectional GPIO is connected to FPGA from SoC and it is connected to expander3 inside FPGA and accessible to BCM through SPI0 bus.
PLLLOCK_LED_FPGA_1V8_EXP3	O	**PLLLOCK LED:** Indicates PLL Lock status of SoC and drives external transistor base to drive the LED. It is accessed by BMC SPI0 bus.
SOC_PLLLOCK_FPGA_1V8_EXP3	I	**SOC PLLLOCK:** Input signal to FPGA from SoC. It is read by BMC through its SPI0 bus.
NOR_WPz	O	**NOR WP:** BMC microcontroller can control this signal and make NOR flash write protect through this signal.
NAND_WPZ_FPGA_1V8_EXP3	O	**NAND WP:** BMC microcontroller can control this signal and make NAND flash write protect through this signal.
EEPROM_WPZ_FPGA_1V8_EXP3	O	**EEPROM WP:** BMC microcontroller can control this signal and make EEPROM write protect through this signal.

EXPCON_BDPRESENT_FPGA_1V8_EXP3	I	**BOARD DETECTION ON EXPANSION CONNECTOR:** Indicates card present on Expansion connector. It is read by SPI0 bus of BMC.
EXPCON_BOARD-ID0_FPGA_1V8_EXP3	I	**BOARD ID0 OF EXPANSION CONNECTOR:** Indicates board ID of present board on Expansion connector.
EXPCON_BOARD-ID1_FPGA_1V8_EXP3	I	**BOARD ID1 OF EXPANSION CONNECTOR:** Indicates board ID of present board on Expansion connector.
EXPCON_BOARD-ID2_FPGA_1V8_EXP3	I	**BOARD ID2 OF EXPANSION CONNECTOR:** Indicates board ID of present board on Expansion connector.
EXT_SCL_FPGA_1V8_EXP3	I	I2C Serial Clock to FPGA
EXT_SDA_FPGA_1V8_EXP3	I/O	I2C Serial Data from/to FPGA
BMC_GPIOINT1_FPGA_1V8_EXP3	O	**GPIO EXPANDER3 INTERRUPT:** It is an interrupt to BMC controller if any activity occurs on any of expander3 GPIO lines.
SOC_CORECLKSEL0_FPGA_1V8_ EXP1 [0 : 1]	O	**SOC CORE CLOCK SELECTION:** BMC microcontroller configures SoC core clock through this pins.
SOC_HOUT_FPGA_1V8_EXP1	I	**SOC OUTPUT INTERRUPT PULSE:** Interrupt output pulse created by IPC Generation Host Register of SoC
SOC_NMIZ_FPGA_1V8_EXP1	O	Non-maskable Interrupt signal for SoC
SOC_LRESETZ_FPGA_1V8_EXP1	O	Local (Warm) Reset signal for SoC
SOC_LRESETNMIENZ_FPGA_1V8_EXP1	O	Enable signal for SoC core selects
SOC_BOOTCOMPLETE_FPGA_1V8_EXP1	I	Boot progress indication input from SoC
SOC_RESETSTATZ_FPGA_1V8_EXP1	I	Reset Status Input from SoC
SOC_CORESEL0_FPGA_1V8_EXP1	O	SOC Core selection bit 0
SOC_CORESEL1_FPGA_1V8_EXP1	O	SOC Core selection bit 1
SOC_CORESEL2_FPGA_1V8_EXP1	O	SOC Core selection bit 2
NC	-	Reserved for future use
TIMI_MUX_OEZ_FPGA_1V8_EXP1	O	Timer Mux Output Enable signal
SOC_RESETFULLZ_FPGA_1V8_EXP1	O	SOC Full Reset
SOC_RESETZ_FPGA_1V8_EXP1	O	SOC Reset
SOC_PORZ_FPGA_1V8_EXP1	O	SOC Power-On Reset
BMC_GPIOINT2_FPGA_1V8_EXP1	O	**GPIO EXPANDER1 INTERRUPT:** It is an interrupt to BMC controller if any activity occurs on any of expander1 GPIO lines.
PHY_INT1#_FPGA_3V3_EXP4	I	**PHY1 INTERRUPT:** Interrupt input which can be read by BMC if any activity occurs on PHY1 device.
EXPCON_MCU_RESETSTATZ_FPGA_ 3V3_EXP4	O	Reset Status Output signal
EXT-PS#_FPGA_3V3_EXP4	I	EXP_TP2, Test Point
NC	-	Reserved for future use
NC	-	Reserved for future use

CDCM2_REF_SEL_FPGA_3V3_EXP4	O	**CDCM2 REFERENCE SELECTION:** BMC selects reference input of CDCM6208 - 2 chips through this signal.
CDCM1_REF_SEL_FPGA_3V3_EXP4	O	**CDCM1 REFERENCE SELECTION:** BMC selects reference input of CDCM6208 - 1 chip through this signal.
NC	-	Reserved for future use
CDCM1_REFCLK1_PD#_FPGA_ 3V3_EXP4	O	**CLOCK GENERATOR1 POWER DOWN:** Clock generator is in power down mode when this signal is asserted low. Once all the power supplies are up and initialized, this power down signal is de-asserted by BMC.
CDCM2_REFCLK1_PD#_FPGA_ 3V3_EXP4	O	**CLOCK GENERATOR2 POWER DOWN:** Clock generator is in power down mode when this signal is asserted low. Once all the power supplies are up and initialized, this power down signal is de-asserted by BMC.
NC	-	Reserved for future use
NC	-	Reserved for future use
NC	-	Reserved for future use
NC	-	Reserved for future use
NC	-	Reserved for future use
PHY_INT2#_FPGA_3V3_EXP4	I	**PHY2 INTERRUPT:** Interrupt input which can be read by BMC if any activity occurs on PHY2 device.
BMC_GPIOINT3_FPGA_3V3_EXP4	O	**GPIO EXPANDER4 INTERRUPT:** It is an interrupt to BMC controller if any activity occurs on any of expander4 GPIO lines.
CLK_MUXCTRL2_FPGA_3V3_EXP5	O	**INPUT CLOCK SOURCE SELECTION:** BMC selects required input reference clock for CMCD6208 generator - 2 using this multiplexer control. It selects either AMC 25MHz or 19.2MHz Slave Clock as primary reference of CDCM6208 clock generator - 2.
CLK_MUXCTRL0_FPGA_3V3_EXP5	O	**DFESYNC AND RPCLK/RPFB SELECTION:** It is a common selection control to U48 and U50. BMC can assert this selection control of multiplexer to select input for SoC. By asserting this signal SoC input would be either JESD SYNC or RP CLK and RP FB.
CLK_MUXCTRL1_FPGA_3V3_EXP5	O	**INPUT CLOCK SOURCE SELECTION:** BMC selects required input reference clock for CMCD6208 generator - 1 using this multiplexer control. It selects either external 10MHz or 19.2MHz Clock from oscillator as primary reference of CDCM6208 clock generator - 1.

SERDES_SW1_SEL0_FPGA_3V3_EXP5	O	**SERDES SWITCH1 SELECTION CONTROL:** BMC selects either JESD0 or AIF0 lane which come from SoC, should communicate to FMC1 connector or AMC connector respectively.
SERDES_SW1_SEL1_FPGA_3V3_EXP5	O	**SERDES SWITCH1 SELECTION CONTROL:** BMC selects either JESD1 or AIF1 lane which come from SoC, should communicate to FMC1 connector or AMC connector respectively.
SERDES_SW2_SEL0_FPGA_3V3_EXP5	O	**SERDES SWITCH2 SELECTION CONTROL:** BMC selects JESD2 lane which comes from SoC, should switch to either FMC1 connector or FMC2 connector.
SERDES_SW2_SEL1_FPGA_3V3_EXP5	O	**SERDES SWITCH2 SELECTION CONTROL:** BMC selects JESD3 lane which comes from SoC, should switch to either FMC1 connector or FMC2 connector.
SERDES_SW3_SEL0_FPGA_3V3_EXP5	O	**SERDES SWITCH3 SELECTION CONTROL:** BMC selects either PCI0 lane or SGMII2 lane which comes from SoC, should communicate to AMC connector.
SERDES_SW3_SEL1_FPGA_3V3_EXP5	O	**SERDES SWITCH3 SELECTION CONTROL:** BMC selects either PCI1 lane or SGMII3 lane which comes from SoC, should communicate to AMC connector.
DONE_FPGA_3V3	O	**FPGA PROGRAMMING DONE:** Indicates the status of FPGA programming. It goes to high when FPGA configuration completes.
EXP_GPIO_EN	O	**EXPANSION CONNECTOR GPIO ENABLE:** It enable sets of buffer which connects SoC GPIO [0 : 16] with expansion connector.
NC	-	
NC	-	
NC	-	
NC	-	
NC	-	
BMC_GPIOINT4_FPGA_3V3_EXP5	O	**GPIO EXPANDER5 INTERRUPT:** It is an interrupt to BMC controller if any activity occurs on any of expander5 GPIO lines.
FPGA_GPIO [12 : 15]	O	**FPGA GPIO[12:15]:** These signals control to Debug LED [1:4] respectively through outside buffer.
FPGA_RST#	I	**FPGA RESET:** It is active low reset to FPGA.
JTAG_RST#_FPGA_3V3	I	**FPGA JTAG RESET**
JTAG_FPGA_TCK	I	**FPGA JTAG Clock Input**
JTAG_FPGA_TDI	I	**FPGA JTAG Data Input**
JTAG_FPGA_TDI	O	**FPGA JTAG Data Output**

JTAG_FPGA_TMS	I	**FPGA JTAG Mode Select Input**

5.3 FPGA AFE7500EVM Interface

FPGA provides glue logic such that TCI6630K2L SoC can access AFE7500 chip over Marconi SPI bus. It can also configure clock chip of AFE7500EVM i.e.LMK6208 over LMK SPI bus. DFEGPIO and SOCGPIO of SoC are mapped to AFE7500 chip's GPIO and control signals inside FPGA. The CDCM6208 provides DIVCLK i.e. 122.88MHz as input to FPGA which is divided by1024 factor and 120 KHz SYSREF signal is generated and provided to AFE7500EVM.

FPGA AFE7500EVM interface diagram is shown in below figure.

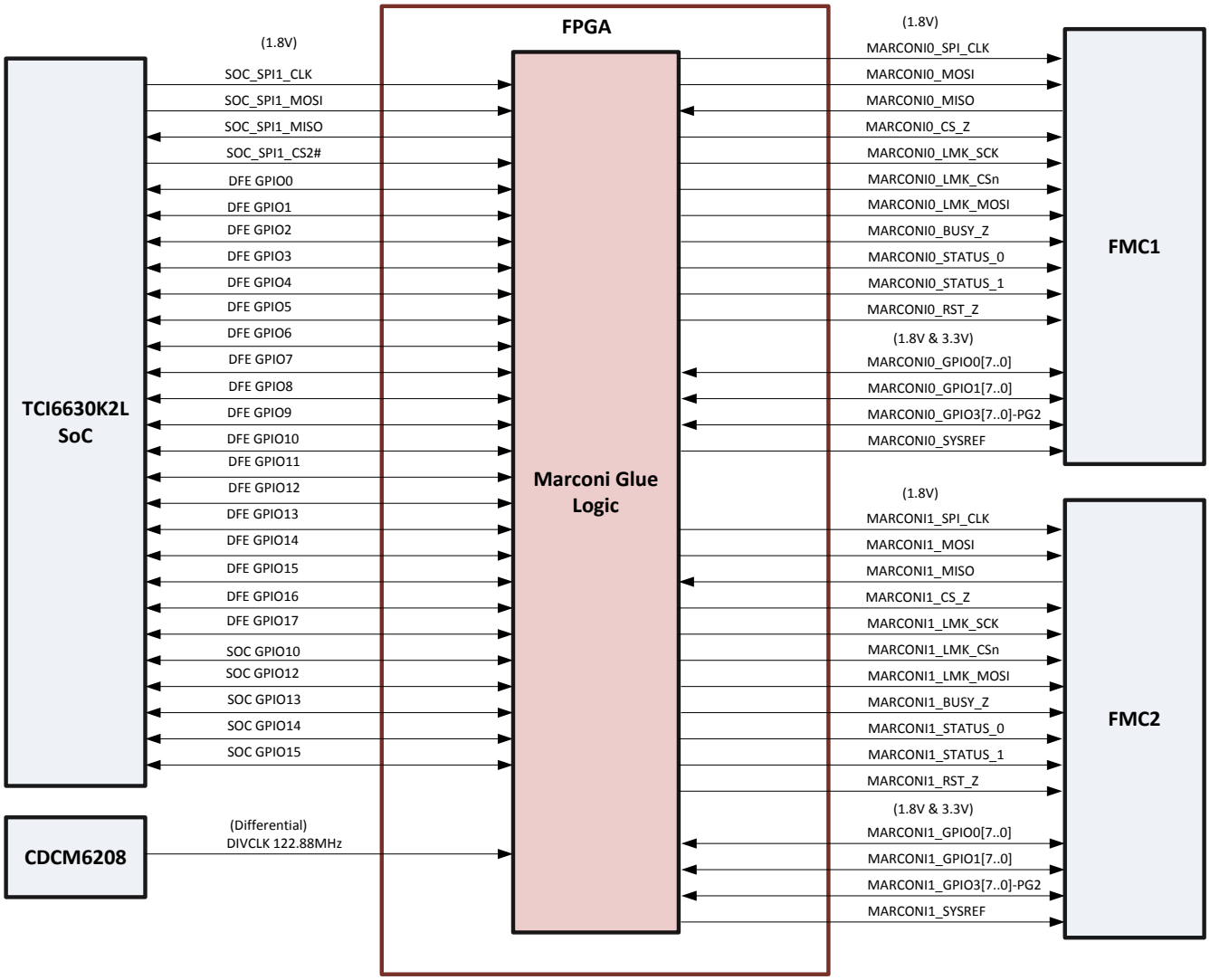


Figure 5.1: FPGA AFE7500EVM Interface

5.4 BMC GPIO Expander

There are five GPIO expander have been implemented inside FPGA to save the board space which can be consumed by discrete components. Each expander provides 16 GPIO lines which Board management controller (BMC) can access this GPIO over SPI0 bus. BCM also receives interrupt with respect to any activity on each expander respectively.

BMC GPIO Expander diagram is shown in below figure.

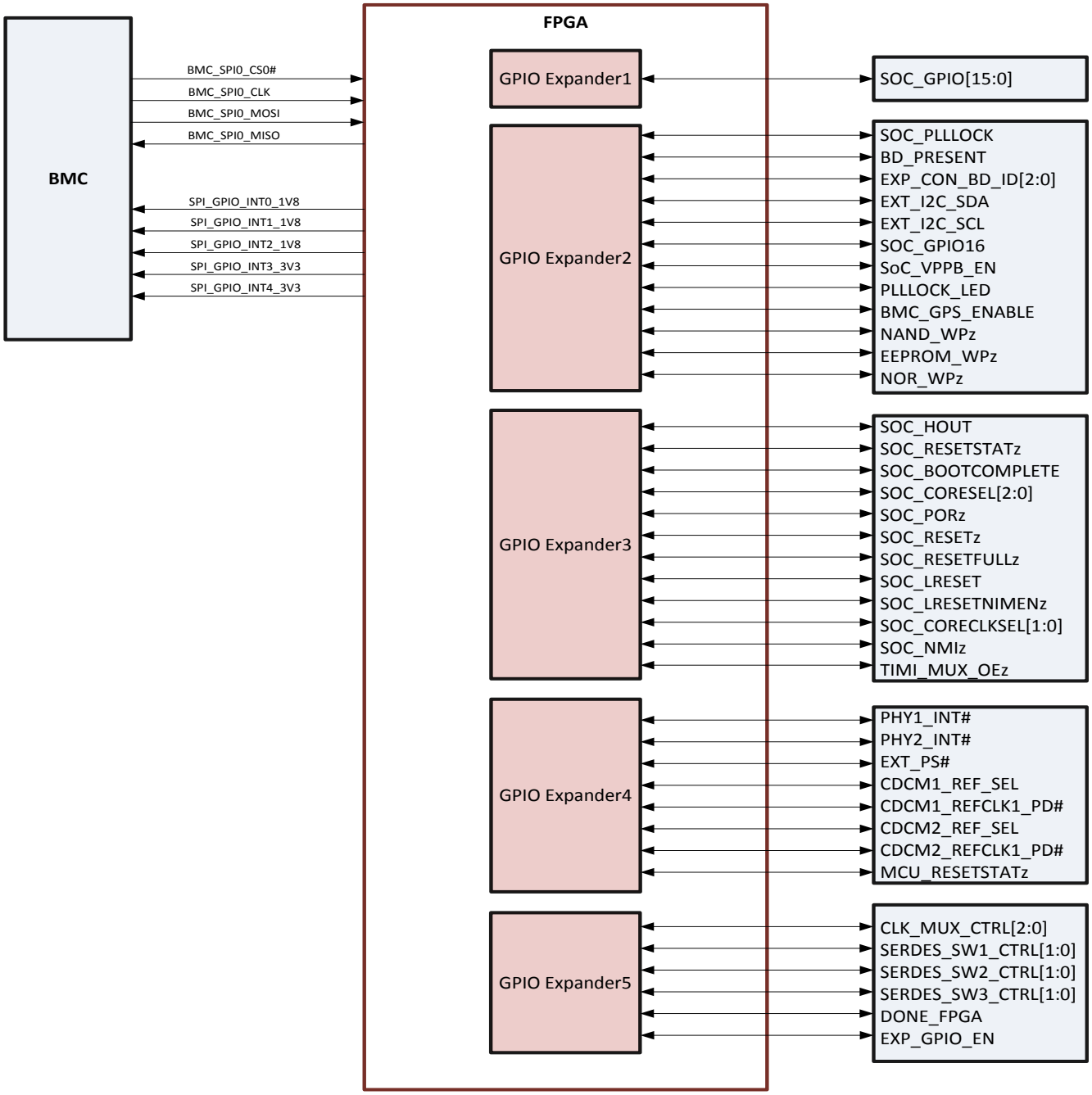


Figure 5.2: BMC GPIO Expander

5.5 TIMER Control Logic

FPGA provides multiplexer logic to select the proper source of timer for SoC input. It also provides access to boot control pin (SOC_TIMO0, SOC_TIMO1) at boot up time through BMC SPI0 bus.

Below figure shows the timer control logic implemented in FPGA.

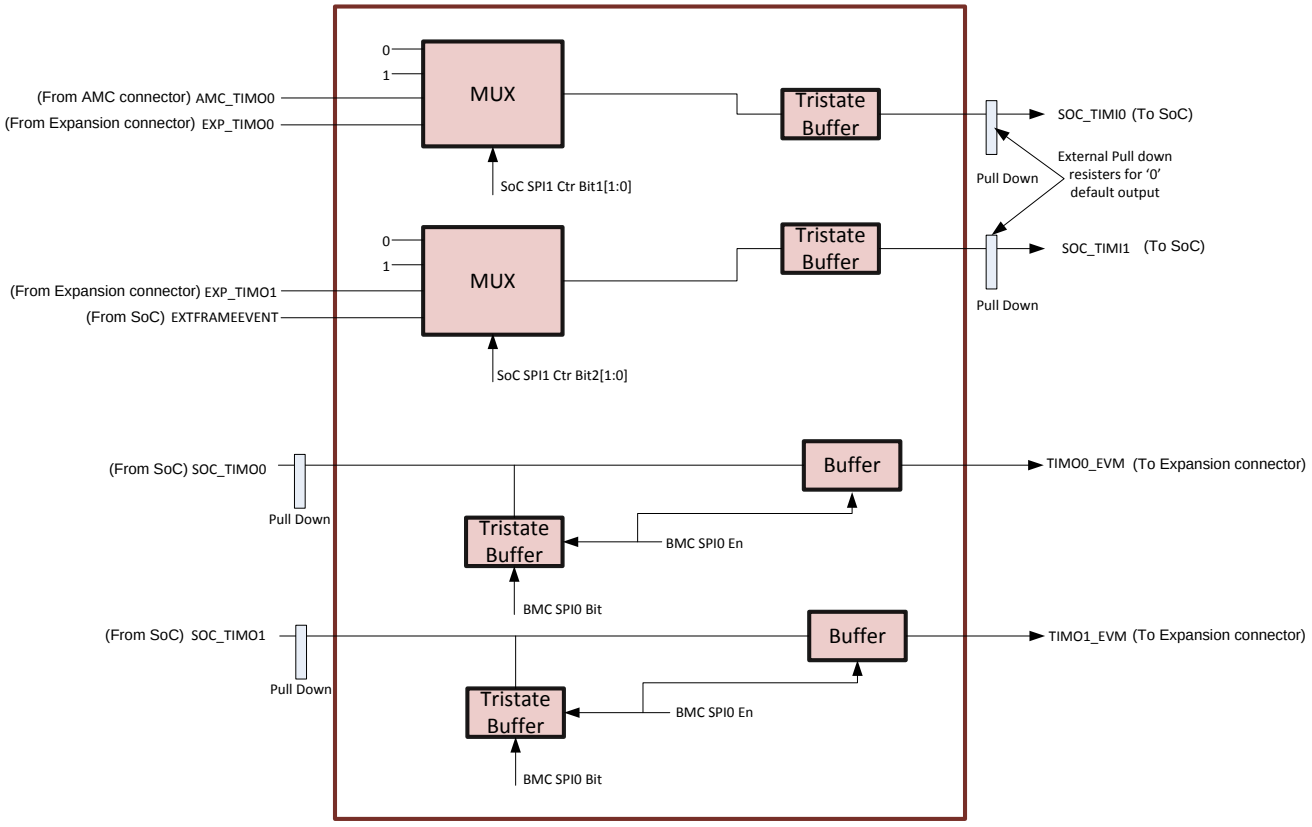


Figure 5.3: TIMER Control Logic

5.6 SPI Protocol

This section describes the FPGA SPI bus protocol design specification for interfacing with TCI6630K2L and BMC. It contains:

5.6.1 FPGA SoC/BMC SPI Protocol

5.6.1 FPGA SoC/BMC Protocol

FPGA supports simple write and read commands for TCI6630K2L and BMC to access the FPGA configuration registers through SPI interface. TCI6630K2L and BMC both follow common protocol to access FPGA configuration registers. The FPGA SPI bus clocks data in on the falling edge of SoC SPI Clock as well as BMC SPI Clock. Data transitions therefore occur on the rising edge of the clock.

The figures below illustrate a SoC to FPGA SPI and BMC to FPGA SPI write operation.

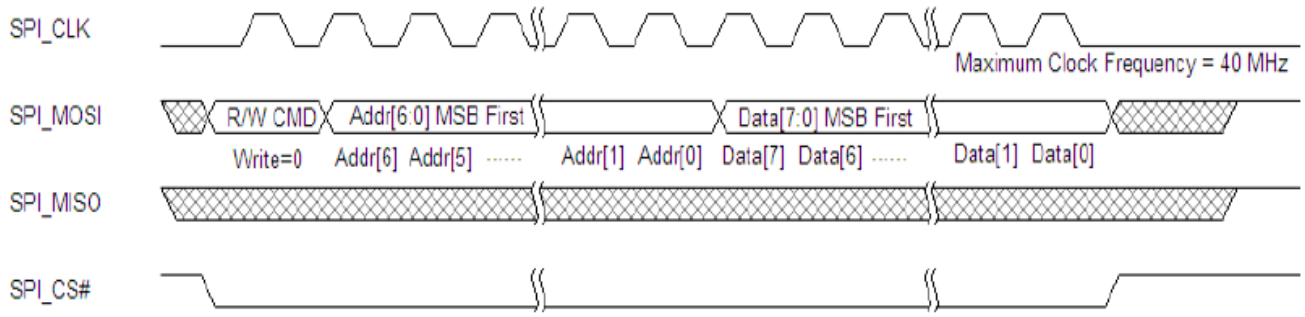


Figure 5.4: SPI access from TCI6630K2L and BMC to FPGA (WRITE / high level)

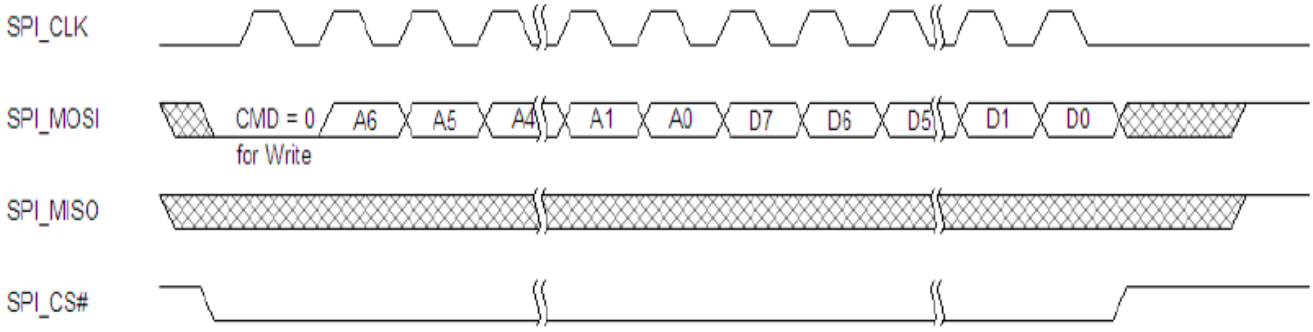


Figure 5.5: SPI access from TCI6630K2L and BMC to FPGA (WRITE)

The below figures illustrate a TCI6630K2L and BMC to FPGA SPI read operation.

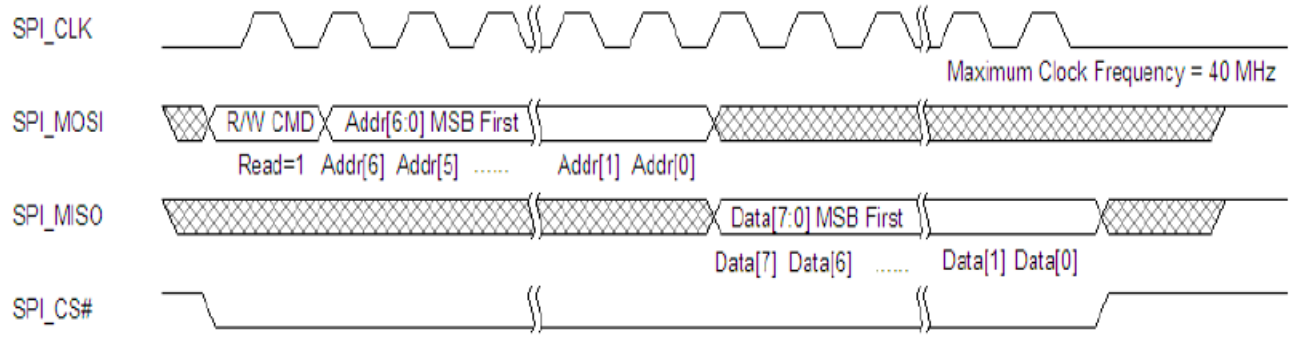


Figure 5.5: SPI access from TCI6630K2L and BMC to FPGA (READ / high level)

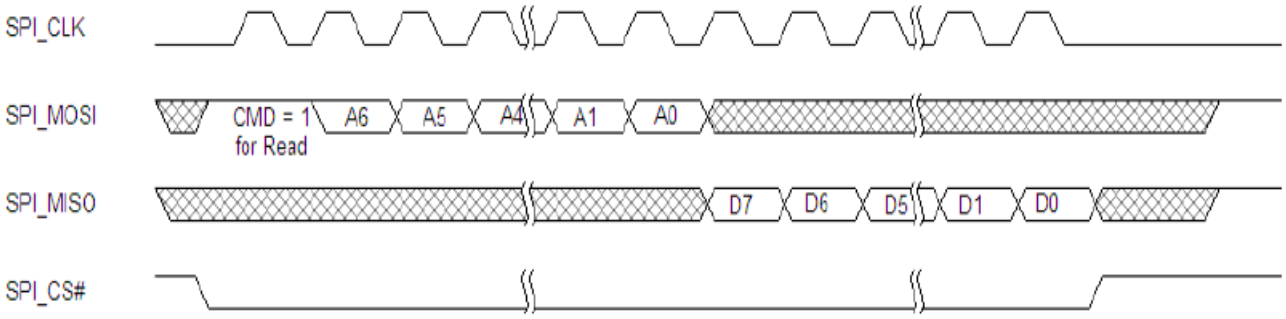


Figure 5.6: SPI access from TCI6630K2L and BMC to FPGA (READ)

5.7 FPGA Configuration Register

The TCI6630K2L SoC and BMC communicate with the FPGA configuration registers through the SPI interface. These registers are addressed by memory mapped location and defined by the SoC/BMC SPI chip enable setting. The following tables list the FPGA configuration registers and the respective descriptions.

Table 5.3: BMC FPGA Pin Description

Memory Map Base Address	Memory Map Offset Address	Memory
BMC SPI Chip Select 0 0x20BF0000-0x20BF03FF (BMC SPI Memory Map Address)	0x00-0x22	Configuration Registers

Table 5.4: TCI6630K2L EVM FPGA Pin Description

Memory Map Base Address	Memory Map Offset Address	Memory
DSP SPI1 Chip Select 1 0x21000600-0x210007FF (TMS320C6657 DSP SPI Memory Map Address)	0x00-0x27	Configuration Registers

5.7.1 FPGA Configuration Register accessible from BMC

There are five 16-bit GPIO expanders in FPGA. Each expander has two 8-bit ports i.e lower byte as Port 0 and higher byte as Port 1. There is a set of three register for each 16-bit GPIO expander, named 16 bit Input Register, 16 bit Output Register and 16 bit Direction control Register. These registers are also divided into two 8 bit Port 0 and port1 respectively.

Table 5.5: BMC FPGA Configuration Registers Summary

Address	Register Name	Attribute (R/W) (RO : Read-Only)	Default Value
0x00	Expander1 Port0 Input	RO	XX
0x01	Expander1 Port1 Input	RO	XX
0x02	Expander1 Port0 Output	R/W	0x00
0x03	Expander1 Port1 Output	R/W	0x00
0x04	Expander1 Port0 Direction	R/W	0x00
0x05	Expander1 Port1 Direction	R/W	0x00
0x06	Expander2 Port0 Input	RO	XX
0x07	Expander2 Port1 Input	RO	0x00
0x08	Expander2 Port0 Output	R/W	0x00
0x09	Expander2 Port1 Output	R/W	0x00
0x0A	Expander2 Port0 Direction	R/W	0x00
0x0B	Expander2 Port1 Direction	R/W	0x00
0x0C	Expander3 Port0 Input	RO	XX
0x0D	Expander3 Port1 Input	RO	XX
0x0E	Expander3 Port0 Output	R/W	0x00
0x0F	Expander3 Port1 Output	R/W	0x00
0x10	Expander3 Port0 Direction	R/W	0x00
0x11	Expander3 Port1 Direction	R/W	0x00
0x12	Expander4 Port0 Input	RO	XX
0x13	Expander4 Port1 Input	RO	XX
0x14	Expander4 Port0 Output	R/W	0x00
0x15	Expander4 Port1 Output	R/W	0x00
0x16	Expander4 Port0 Direction	R/W	0x00
0x17	Expander4 Port1 Direction	R/W	0x00
0x18	Expander5 Port0 Input	RO	XX
0x19	Expander5 Port1 Input	RO	XX
0x1A	Expander5 Port0 Output	R/W	0x00
0x1B	Expander5 Port1 Output	R/W	0x00
0x1C	Expander5 Port0 Direction	R/W	0x00
0x1D	Expander5 Port1 Direction	R/W	0x00
0x1E	Interrupt register for Expander	R/W	0x00
0x1F	Debug LED	R/W	0x00
0x20	BMC_BOOT_TIMO0	R/W	0x00

0x21	BMC_BOOT_TIMO1	R/W	0x00
0x22	FPGA Revison ID	RO	0x00

5.7.1.1. FPGA Configuration Register Descriptions

Register Address: **00h**
Register Name: **Expander1 Port0 Input (07-00 Low Byte) Register**
Default Value: ------
Attribute: Read Only

Bit	Description	Read/Write
0	**SoC GPIO 00:** This bit reflects the state of the SoC general purpose input signal GPIO 00 and writes will have no effect. 0 : SoC GPIO 00 state is low 1 : SoC GPIO 00 state is high	RO
1	**SoC GPIO 01:** This bit reflects the state of the SoC general purpose input signal GPIO 01 and writes will have no effect. 0 : SoC GPIO 01 state is low 1 : SoC GPIO 01 state is high	RO
2	**SoC GPIO 02:** This bit reflects the state of the SoC general purpose input signal GPIO 02 and writes will have no effect. 0 : SoC GPIO 02 state is low 1 : SoC GPIO 02 state is high	RO
3	**SoC GPIO 03:** This bit reflects the state of the SoC general purpose input signal GPIO 03 and writes will have no effect. 0 : SoC GPIO 03 state is low 1 : SoC GPIO 03 state is high	RO
4	**SoC GPIO 04:** This bit reflects the state of the SoC general purpose input signal GPIO 04 and writes will have no effect. 0 : SoC GPIO 04 state is low 1 : SoC GPIO 04 state is high	RO
5	**SoC GPIO 05:** This bit reflects the state of the SoC general purpose input signal GPIO 05 and writes will have no effect. 0 : SoC GPIO 05 state is low 1 : SoC GPIO 05 state is high	RO
6	**SoC GPIO 06:** This bit reflects the state of the SoC general purpose input signal GPIO 06 and writes will have no effect. 0 : SoC GPIO 06 state is low 1 : SoC GPIO 06 state is high	RO
7	**SoC GPIO 07:** This bit reflects the state of the SoC general purpose input signal GPIO 07 and writes will have no effect. 0 : SoC GPIO 07 state is low 1 : SoC GPIO 07 state is high	RO

Register Address: **01h**
Register Name: **Expander1 Port1 Input (15-08 High Byte) Register**
Default Value: ------
Attribute: Read Only

Bit	Description	Read/Write
0	**SoC GPIO 08:** This bit reflects the state of the SoC general purpose input signal GPIO 08 and writes will have no effect. 0 : SoC GPIO 08 state is low 1 : SoC GPIO 08 state is high	RO
1	**SoC GPIO 09:** This bit reflects the state of the SoC general purpose input signal GPIO 09 and writes will have no effect. 0 : SoC GPIO 09 state is low 1 : SoC GPIO 09 state is high	RO
2	**SoC GPIO 10:** This bit reflects the state of the SoC general purpose input signal GPIO 10 and writes will have no effect. 0 : SoC GPIO 10 state is low 1 : SoC GPIO 10 state is high	RO
3	**SoC GPIO 11:** This bit reflects the state of the SoC general purpose input signal GPIO 11 and writes will have no effect. 0 : SoC GPIO 11 state is low 1 : SoC GPIO 11 state is high	RO
4	**SoC GPIO 12:** This bit reflects the state of the SoC general purpose input signal GPIO 12 and writes will have no effect. 0 : SoC GPIO 12 state is low 1 : SoC GPIO 12 state is high	RO
5	**SoC GPIO 13:** This bit reflects the state of the SoC general purpose input signal GPIO 13 and writes will have no effect. 0 : SoC GPIO 13 state is low 1 : SoC GPIO 13 state is high	RO
6	**SoC GPIO 14:** This bit reflects the state of the SoC general purpose input signal GPIO 14 and writes will have no effect. 0 : SoC GPIO 14 state is low 1 : SoC GPIO 14 state is high	RO
7	**SoC GPIO 15:** This bit reflects the state of the SoC general purpose input signal GPIO 15 and writes will have no effect. 0 : SoC GPIO 15 state is low 1 : SoC GPIO 15 state is high	RO

Register Address: **02h**
Register Name: **Expander1 Port0 Output (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write

0	**SoC GPIO 00:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 00 pin. 0 : SoC GPIO 00 drives low 1 : SoC GPIO 00 drives high	R/W
1	**SoC GPIO 01:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 01 pin. 0 : SoC GPIO 01 drives low 1 : SoC GPIO 01 drives high	R/W
2	**SoC GPIO 02:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 02 pin. 0 : SoC GPIO 02 drives low 1 : SoC GPIO 02 drives high	R/W
3	**SoC GPIO 03:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 03 pin. 0 : SoC GPIO 03 drives low 1 : SoC GPIO 03 drives high	R/W
4	**SoC GPIO 04:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 04 pin. 0 : SoC GPIO 04 drives low 1 : SoC GPIO 04 drives high	R/W
5	**SoC GPIO 05:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 05 pin. 0 : SoC GPIO 05 drives low 1 : SoC GPIO 05 drives high	R/W
6	**SoC GPIO 06:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 06 pin. 0 : SoC GPIO 06 drives low 1 : SoC GPIO 06 drives high	R/W
7	**SoC GPIO 07:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 07 pin. 0 : SoC GPIO 07 drives low 1 : SoC GPIO 07 drives high	R/W

Register Address: **03h**
Register Name: **Expander1 Port1 Output (15-08 High Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**SoC GPIO 08:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 08 pin. 0 : SoC GPIO 08 drives low 1 : SoC GPIO 08 drives high	R/W
1	**SoC GPIO 09:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 09 pin. 0 : SoC GPIO 09 drives low 1 : SoC GPIO 09 drives high	R/W

2	**SoC GPIO 10:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 10 pin. 0 : SoC GPIO 10 drives low 1 : SoC GPIO 10 drives high	R/W
3	**SoC GPIO 11:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 11 pin. 0 : SoC GPIO 11 drives low 1 : SoC GPIO 11 drives high	R/W
4	**SoC GPIO 12:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 12 pin. 0 : SoC GPIO 12 drives low 1 : SoC GPIO 12 drives high	R/W
5	**SoC GPIO 13:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 13 pin. 0 : SoC GPIO 13 drives low 1 : SoC GPIO 13 drives high	R/W
6	**SoC GPIO 14:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 14 pin. 0 : SoC GPIO 14 drives low 1 : SoC GPIO 14 drives high	R/W
7	**SoC GPIO 15:** This bit can be updated by the BMC software to drive a high or low value on the SoC GPIO 15 pin. 0 : SoC GPIO 15 drives low 1 : SoC GPIO 15 drives high	R/W

Register Address: **04h**
Register Name: **Expander1 Port0 Direction (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**EXP1_GPIO_DIR_0_00:** This bit can be updated by the BMC software to set a direction of expander 1 pin 0 (SoC GPIO 00) 0 : sets direction of pin 0 of exp 1 as input 1 : sets direction of pin 0 of exp 1 as output	R/W
1	**EXP1_GPIO_DIR_0_01:** This bit can be updated by the BMC software to set a direction of expander 1 pin 1 (SoC GPIO 01) 0 : sets direction of pin 1 of exp 1 as input 1 : sets direction of pin 1 of exp 1 as output	R/W
2	**EXP1_GPIO_DIR_0_02:** This bit can be updated by the BMC software to set a direction of expander 1 pin 2 (SoC GPIO 02) 0 : sets direction of pin 2 of exp 1 as input 1 : sets direction of pin 2 of exp 1 as output	R/W
3	**EXP1_GPIO_DIR_0_03:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 3 (SoC GPIO 03) 0 : sets direction of pin 3 of exp 1 as input 1 : sets direction of pin 3 of exp 1 as output	R/W

4	**EXP1_GPIO_DIR_0_04:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 4. (SoC GPIO 04) 0 : sets direction of pin 4 of exp 1 as input 1 : sets direction of pin 4 of exp 1 as output	R/W
5	**EXP1_GPIO_DIR_0_05:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 5. (SoC GPIO 05) 0 : sets direction of pin 5 of exp 1 as input 1 : sets direction of pin 5 of exp 1 as output	R/W
6	**EXP1_GPIO_DIR_0_06:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 6. (SoC GPIO 06) 0 : sets direction of pin 6 of exp 1 as input 1 : sets direction of pin 6 of exp 1 as output	R/W
7	**EXP1_GPIO_DIR_0_07:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 7. (SoC GPIO 07) 0 : sets direction of pin 7 of exp 1 as input 1 : sets direction of pin 7 of exp 1 as output	R/W

Register Address: **05h**
Register Name: **Expander1 Port1 Direction (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**EXP1_GPIO_DIR_1_0:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 8.. (SoC GPIO 08) 0 : sets direction of pin 8 of exp 1 as input 1 : sets direction of pin 8 of exp 1as output	R/W
1	**EXP1_GPIO_DIR_1_1:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 9. (SoC GPIO 09) 0 : sets direction of pin 9 of exp 1 as input 1 : sets direction of pin 9 of exp 1 as output	R/W
2	**EXP1_GPIO_DIR_1_2:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 10. (SoC GPIO 10) 0 : sets direction of pin 10 of exp 1 as input 1 : sets direction of pin 10 of exp 1 as output	R/W
3	**EXP1_GPIO_DIR_1_3:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 11. (SoC GPIO 11) 0 : sets direction of pin 11 of exp 1 as input 1 : sets direction of pin 11 of exp 1 as output	R/W
4	**EXP1_GPIO_DIR_1_4:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 12. (SoC GPIO 12) 0 : sets direction of pin 12 of exp 1 as input 1 : sets direction of pin 12 of exp 1 as output	R/W
5	**EXP1_GPIO_DIR_1_5:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 13. (SoC GPIO 13) 0 : sets direction of pin 13 of exp 1 as input 1 : sets direction of pin 13 of exp 1 as output	R/W

6	**EXP1_GPIO_DIR_1_6:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 14. (SoC GPIO 14) 0 : sets direction of pin 14 of exp 1 as input 1 : sets direction of pin 14 of exp 1 as output	R/W
7	**EXP1_GPIO_DIR_1_7:** This bit can be updated by the BMC software to drive the pin direction of expander 1 pin 15. (SoC GPIO 15) 0 : sets direction of pin 15 of exp 1 as input 1 : sets direction of pin 15 of exp 1 as output	R/W

Register Address: **06h**
Register Name: **Expander2 Port0 Input (07-00 Low Byte) Register**
Default Value: ------
Attribute: Read Only

Bit	Description	Read
0	**RESERVED**	R
1	**RESERVED**	R
2	**BMC GPS EN:** This bit reflects the state of the “BMC_GPS_EN” pin and writes will have no effect. 0 : BMC GPS EN state is low 1 : BMC GPS EN state is high	R
3	**SoC VPPB EN:** This bit reflects the state of the “SoC_VPPB_EN” pin and writes will have no effect. 0 : SoC_VPPB_EN state is low 1 : SoC_VPPB_EN state is high	R
4	**SoC GPIO 16:** This bit reflects the state of the “SoC_GPIO16” pin and writes will have no effect. 0 : SoCGPIO16 state is low 1 : SoCGPIO16 state is high	R
5	**PLL LOCK LED:** This bit reflects the state of the “PLL_LOCK_LED” pin and writes will have no effect. 0 : PLL_LOCK_LED state is low 1 : PLL_LOCK_LED state is high	R
6	**SOC PLL LOCK :** This bit reflects the state of the “SOC_PLL_LOCK” pin and writes will have no effect. 0 : SOC_PLL_LOCK state is low 1 : SOC_PLL_LOCK state is high	R
7	**NOR WPZ:** This bit reflects the state of the “NOR_WPZ” pin and writes will have no effect. 0 : NOR_WPZ state is low 1 : NOR_WPZ state is high	R

Register Address: **07h**
Register Name: **Expander2 Port1 Input (07-00 Low Byte) Register**
Default Value: 0x00
Attribute: Read Only

Bit	Description	Read
0	**NAND WPZ:** This bit reflects the state of the “NAND_WPZ” pin and writes will have no effect. 0 : NAND_WPZ state is low 1 : NAND_WPZ state is high	R
1	**EEPROM WPZ:** This bit reflects the state of the “EEPROMWPZ” pin and writes will have no effect. 0 : EEPROM_WPZ state is low 1 : EEPROM_WPZ state is high	R
2	**EXPCON BDPRESENT:** This bit reflects the state of the “EXPCONBDPRESENT” (Board Detect) pin and writes will have no effect. 0 : EXPCONBDPRESENT state is low 1 : EXPCONBDPRESENT state is high	R
3	**EXPCON BD ID [0]:** This bit reflects the state of the “EXPCON_BD_ID_0” (Board Identification) pin and writes will have no effect. 0 : EXPCON_BD_ID state is low 1 : EXPCON_BD_ID state is high	R
4	**EXPCON BD ID [1]:** This bit reflects the state of the “EXPCON_BD_ID_1” (Board Identification) pin and writes will have no effect. 0 : EXPCON_BD_ID_1 state is low 1 : EXPCON_BD_ID_1 state is high	R
5	**EXPCON BD ID [2]:** This bit reflects the state of the “EXPCON_BD_ID_2” (Board Identification) pin and writes will have no effect. 0 : EXPCON_BD_ID_2 state is low 1 : EXPCON_BD_ID_2 state is high	R
6	**EXT SCL:** This bit reflects the state of the “EXT_SCL” (Serial Clock)pin and writes will have no effect. 0 : EXT_SCL state is low 1 : EXT_SCL state is high	R
7	**EXT SDA:** This bit reflects the state of the “EXT_SDA” (Serial Data)pin and writes will have no effect. 0 : EXT_SDA state is low 1 : EXT_SDA state is high	R

Register Address: **08h**
Register Name: **Expander2 Port0 Output (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**RESERVED**	R/W
1	**RESERVED**	R/W
2	**BMC GPS EN:** This bit can be updated by the BMC software to drive a high or low value on the “BMC_GPS_EN” pin. 0 : BMC_GPS_EN drives low 1 : BMC_GPS_EN drives high	R/W
3	**SoC VPPB EN:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_VPPB_EN” pin. 0 : SoC_VPPB_EN drives low 1 : SoC_VPPB_EN drives high	R/W
4	**SoC GPIO 16:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_GPIO16” pin. 0 : SoC_GPIO16 drives low 1 : SoC_GPIO16 drives high	R/W
5	**PLL LOCK LED:** This bit can be updated by the BMC software to drive a high or low value on the “PLL_LOCK_LED” pin. 0 : PLL_LOCK_LED drives low 1 : PLL_LOCK_LED drives high	R/W
6	**SoC PLL LOCK:** This bit can be updated by the BMC software to drive a high or low value on the “Soc_PLL_LOCK” pin. 0 : SoC_PLL_LOCK drives low 1 : SoC_PLL_LOCK drives high	R/W
7	**NOR WPZ:** This bit can be updated by the BMC software to drive a high or low value on the “NOR_WPZ” pin. 0 : NOR_WPZ drives low 1 : NOR_WPZ drives high	R/W

Register Address: **09h**
Register Name: **Expander2 Port1 Output (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**NAND WPZ:** This bit can be updated by the BMC software to drive a high or low value on the “NAND_WPZ” pin. 0 : NAND_WPZ drives low 1 : NAND_WPZ drives high	R/W
1	**EEPROM WPZ:** This bit can be updated by the BMC software to drive a high or low value on the “EEPROM_WPZ” pin. 0 : EEPROM_WPZ drives low 1 : EEPROM_WPZ drives high	R/W

2	**EXPCON BDPRESENT:** This bit can be updated by the BMC software to drive a high or low value on the “EXPCON_BDPRESENT” (Board Detect)” pin. 0 : EXPCON_BDPRESENT drives low 1 : EXPCON_BDPRESENT drives high	R/W
3	**EXPCON BD ID[0]:** This bit can be updated by the BMC software to drive a high or low value on the “EXPCON_BD_ID_0” (Board Identification) pin. 0 : EXPCON_BD_ID_0 drives low 1 : EXPCON_BD_ID_0 drives high	R/W
4	**EXPCON BD ID[1]:** This bit can be updated by the BMC software to drive a high or low value on the EXPCON_BD_ID_1” (Board Identification) pin. 0 : EXPCON_BD_ID_1 drives low 1 : EXPCON_BD_ID_1 drives high	R/W
5	**EXPCON BD ID[2]:** This bit can be updated by the BMC software to drive a high or low value on the EXPCON_BD_ID_2” (Board Identification) pin. 0 : EXPCON_BD_ID_2 drives low 1 : EXPCON_BD_ID_2 drives high	R/W
6	**EXT SCL :** This bit can be updated by the BMC software to drive a high or low value on the “EXT_SCL” (Serial Clock) pin. 0 : EXT_SCL state is low 1 : EXT_SCL state is high	R/W
7	**EXT SDA:** This bit can be updated by the BMC software to drive a high or low value on the “EXT_SDA” (Serial Data) pin. 0 : EXT_SDA state is low 1 : EXT_SDA state is high	R/W

Register Address: **0Ah**
Register Name: **Expander2 Port0 Direction (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**RESERVED**	R/W
1	**RESERVED**	R/W
2	**EXP2_GPIO_DIR_0_2:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 2. (BMC_GPS_EN) 0 : sets direction of pin 2 of exp 2 as input 1 : sets direction of pin 2 of exp 2 as out	R/W

3	**EXP2_GPIO_DIR_0_3:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 3. (SoC_VPPB_EN). 0 : sets direction of pin 3 of exp 2 as input 1 : sets direction of pin 3 of exp 2 as out	R/W
4	**EXP2_GPIO_DIR_0_4:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 4. (SoC_GPIO16). 0 : sets direction of pin 4 of exp 2 as input 1 : sets direction of pin 4 of exp 2 as out	R/W
5	**EXP2_GPIO_DIR_0_5:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 5. (PLL_LOCK_LED). 0 : sets direction of pin 5 of exp 2 as input 1 : sets direction of pin 5 of exp 2 as out	R/W
6	**EXP2_GPIO_DIR_0_6:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 6. (Soc_PLL_LOCK). 0 : sets direction of pin 6 of exp 2 as input 1 : sets direction of pin 6 as out	R/W
7	**EXP2_GPIO_DIR_0_7:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 7. (NOR_WPZ). 0 : sets direction of pin 7 of exp 2 as input 1 : sets direction of pin 7 of exp 2 as out	R/W

Register Address: **0Bh**
Register Name: **Expander2 Port1 Direction (07-00 High Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**EXP2_GPIO_DIR_1_0:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 8. (NAND_WPZ). 0 : sets direction of pin 8 of exp 2 as input 1 : sets direction of pin 8 of exp 2 as out	R/W
1	**EXP2_GPIO_DIR_1_1:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 9. (EEPROM_WPZ). 0 : sets direction of pin 9 of exp 2 as input 1 : sets direction of pin 9 of exp 2 as out	R/W
2	**EXP2_GPIO_DIR_1_2:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 10. (EXPCON_BDPRESENT). 0 : sets direction of pin 10 of exp 2 as input 1 : sets direction of pin 10 of exp 2 as out	R/W
3	**EXP2_GPIO_DIR_1_3:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin11. (EXPCON_BD_ID_0). 0 : sets direction of pin 11 of exp 2 as input 1 : sets direction of pin 11 of exp 2 as out	R/W
4	**EXP2_GPIO_DIR_1_4:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 12. (EXPCON_BD_ID_1). 0 : sets direction of pin 12 of exp 2 as input 1 : sets direction of pin 12 of exp 2 as out	R/W

5	**EXP2_GPIO_DIR_1_5:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 13. (EXPCON_BD_ID_2). 0 : sets direction of pin 13 of exp 2 as input 1 : sets direction of pin 13 of exp 2 as out	R/W
6	**EXP2_GPIO_DIR_1_6:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 14. (EXT_SCL) 0 : sets direction of pin 14 of exp 2 as input 1 : sets direction of pin 14 of exp 2 as out	R/W
7	**EXP2_GPIO_DIR_1_7:** This bit can be updated by the BMC software to drive the pin direction of expander 2 pin 15. (EXT_SDA). 0 : sets direction of pin 15 of exp 2 as input 1 : sets direction of pin 15 of exp 2 as out	R/W

Register Address: **0Ch**
Register Name: **Expander3 Port0 Input (07-00 Low Byte) Register**
Default Value: ----
Attribute: Read Only

Bit	Description	Read
0	**SoC CORE SEL [0]:** This bit reflects the state of the “SoCCORESEL0” pin and writes will have no effect. 0 : SoCCORESEL0state is low 1 : SoCCORESEL0state is high	R
1	**SoC CORE SEL [1]:** This bit reflects the state of the “SoCCORESEL1” pin and writes will have no effect. 0 : SoCCORESEL1state is low 1 : SoCCORESEL1state is high	R
2	**SoC HOUT:** This bit reflects the state of the “SoCHOUT” pin and writes will have no effect. 0 : SoCHOUT state is low 1 : SoCHOUT state is high	R
3	**SoC NMIZ:** This bit reflects the state of the “SoCNMIZ” pin and writes will have no effect. 0 : SoCNMIZ state is low 1 : SoCNMIZ state is high	R
4	**SoC LRESETZ:** This bit reflects the state of the “SoCLRESETZ” pin and writes will have no effect. 0 : SoCLRESETZ state is low 1 : SoCLRESETZ state is high	R
5	**SoC LRESETNMIENZ:** This bit reflects the state of the “SoCLRESETNMIENZ” pin and writes will have no effect. 0 : SoCLRESETNMIENZ state is low 1 : SoCLRESETNMIENZ state is high	R
6	**SoC BOOTCOMPLETE:** This bit reflects the state of the “SoCBOOTCOMPLETE” pin and writes will have no effect. 0 : SoCBOOTCOMPLETE state is low 1 : SoCBOOTCOMPLETE state is high	R

7	**SoC RESETSTATZ:** This bit reflects the state of the "SoCRESETSTATZ" pin and writes will have no effect. 0 : SoCRESETSTATZ state is low 1 : SoCRESETSTATZ state is high	R

Register Address: **0Dh**
Register Name: **Expander3 Port1 Input (07-00 Low Byte) Register**
Default Value: ----
Attribute: Read Only

Bit	Description	Read
0	**SoC CORE SEL [0]:** This bit reflects the state of the "SoCCORESEL0" pin and writes will have no effect. 0 : SoCCORESEL0state is low 1 : SoCCORESEL0state is high	R
1	**SoC CORE SEL [1]:** This bit reflects the state of the "SoCCORESEL1" pin and writes will have no effect. 0 : SoCCORESEL1state is low 1 : SoCCORESEL1state is high	R
2	**SoC CORE SEL [2]:** This bit reflects the state of the "SoCCORESEL2" pin and writes will have no effect. 0 : SoCCORESEL2 state is low 1 : SoCCORESEL2 state is high	R
3	**RESERVED**	R
4	**SoC TIMI MUX OEZ:** This bit reflects the state of the "SoCTIMIMUXOEZ" pin and writes will have no effect. 0 : SoCTIMIMUXOEZ state is low 1 : SoCTIMIMUXOEZ state is high	R
5	**SoC RESETFULLZ:** This bit reflects the state of the "SoCRESETFULLZ" pin and writes will have no effect. 0 : SoCRESETFULLZ state is low 1 : SoCRESETFULLZ state is high	R
6	**SoC RESETZ:** This bit reflects the state of the "SoCRESETZ" pin and writes will have no effect. 0 : SoCRESETZ state is low 1 : SoCRESETZ state is high	R
7	**SoC PORZ:** This bit reflects the state of the "SoCPORZ" pin and writes will have no effect. 0 : SoCPORZ state is low 1 : SoCPORZ state is high	R

Register Address: **0Eh**
Register Name: **Expander3 Port0 Output (07-00 Low Byte) Register**
Default Value: 00

Attribute: Read/Write

Bit	Description	Read/Write
0	**SoC CORE SEL [0]:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_CORECLKSEL0” pin. 0 : SoC_CORECLKSEL0 drives low 1 : SoC_CORECLKSEL0 drives high	R/W
1	**SoC CORE SEL [1]::** This bit can be updated by the BMC software to drive a high or low value on the “SoC_CORECLKSEL1” pin. 0 : SoC_CORECLKSEL1 drives low 1 : SoC_CORECLKSEL1 drives high	R/W
2	**SoC HOUT:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_HOUT” pin. 0 : SoC_HOUT drives low 1 : SoC_HOUT drives high	R/W
3	**SoC NMIZ**: This bit can be updated by the BMC software to drive a high or low value on the “SoC_NMIZ”. 0 : SoC_NMIZ drives low 1 : SoC_NMIZ drives high	R/W
4	**SoC LRESETZ:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_LRESETZ” pin. 0 : SoC_LRESETZ drives low 1 : SoC_LRESETZ drives high	R/W
5	**SoC LRESETNMIENZ:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_LRESETNMIENZ” pin. 0 : SoC_LRESETNMIENZ drives low 1 : SoC_LRESETNMIENZ drives high	R/W
6	**SoC BOOTCOMPLETE:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_BOOTCOMPLETE” pin. 0 : SoC_BOOTCOMPLETE state is low 1 : SoC_BOOTCOMPLETE state is high	R/W
7	**SoC RESETSTATZ:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_RESETSTATZ” pin. 0 : SoC_RESETSTATZ state is low 1 : SoC_RESETSTATZ state is high	R/W

Register Address: **0Fh**
Register Name: **Expander3 Port1 Output (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**SoC CORE SEL[0]:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_CORESEL0” pin. 0 : SoC_CORESEL0 drives low 1 : SoC_CORESEL0 drives high	R/W

1	**SoC CORE SEL[1]::** This bit can be updated by the BMC software to drive a high or low value on the “SoC_CORESEL1” pin. 0 : SoC_CORESEL1 drives low 1 : SoC_CORESEL1 drives high	R/W
2	**SoC CORE SEL[2]::** This bit can be updated by the BMC software to drive a high or low value on the “SoC_CORESEL2” pin. 0 : SoC_CORESEL2 drives low 1 : SoC_CORESEL2 drives high	R/W
3	**RESERVED**	R/W
4	**TIMI MUX OEZ:** This bit can be updated by the BMC software to drive a high or low value on the “TIMI_MUXOEZ” pin. 0 : TIMI_MUXOEZ drives low 1 : TIMI_MUXOEZ drives high	R/W
5	**SoC RESETFULLZ:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_RESETFULLZ” pin. 0 : SoC_RESETFULLZ drives low 1 : SoC_RESETFULLZ drives high	R/W
6	**SoC RESETZ:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_RESETZ” pin. 0 : SoC_RESETZ state is low 1 : SoC_RESETZ state is high	R/W
7	**SoC PORZ:** This bit can be updated by the BMC software to drive a high or low value on the “SoC_PORZ” (Power on reset) pin. 0 : SoC_PORZ state is low 1 : SoC_PORZ state is high	R/W

Register Address: **10h**
Register Name: **Expander3 Port0 Direction (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**EXP3_GPIO_DIR_0_0:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 0. (SoC_CORECLK_SEL0). 0 : sets direction of pin 0 of exp 3 as input 1 : sets direction of pin 0 of exp 3 as out	R/W
1	**EXP3_GPIO_DIR_0_1:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 1. (SoC_CORECLK_SEL1). 0 : sets direction of pin 1 of exp 3 as input 1 : sets direction of pin 1 of exp 3 as out	R/W

2	**EXP3_GPIO_DIR_0_2:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 2. (SoC_HOUT). 0 : sets direction of pin 2 of exp 3 as input 1 : sets direction of pin 2 of exp 3 as out	R/W
3	**EXP3_GPIO_DIR_0_3:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 3. (SoC_NMIZ). 0 : sets direction of pin 3 of exp 3 as input 1 : sets direction of pin 3 of exp 3 as out	R/W
4	**EXP3_GPIO_DIR_0_4:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 4. (SoC_LRESETZ). 0 : sets direction of pin 4 of exp 3 as input 1 : sets direction of pin 4 of exp 3 as out	R/W
5	**EXP3_GPIO_DIR_0_5:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 5. (SoC_LRESETNMIENZ). 0 : sets direction of pin 5 of exp 3 as input 1 : sets direction of pin 5 of exp 3 as out	R/W
6	**EXP3_GPIO_DIR_0_6:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 6. (SoC_BOOTCOMPLETE). 0 : sets direction of pin 6 of exp 3 as input 1 : sets direction of pin 6 of exp 3 as out	R/W
7	**EXP3_GPIO_DIR_0_7:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 7. (SoC_RESETSTATZ). 0 : sets direction of pin 7 of exp 3 as input 1 : sets direction of pin 7 of exp 3 as out	R/W

Register Address: **11h**
Register Name: **Expander3 Port1 Direction (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**EXP3_GPIO_DIR_1_0:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 8. (SoC_CORESEL0). 0 : sets direction of pin 8 of exp 3 as input 1 : sets direction of pin 8 of exp 3 as out	R/W
1	**EXP3_GPIO_DIR_1_1:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 9. (SoC_CORESEL1).. 0 : sets direction of pin 9 of exp 3 as input 1 : sets direction of pin 9 of exp 3 as out	R/W
2	**EXP3_GPIO_DIR_1_2:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 10. (SoC_CORESEL2). 0 : sets direction of pin 10 of exp 3 as input 1 : sets direction of pin 10 of exp 3 as out	R/W
3	**RESERVED**	R/W

4	**EXP3_GPIO_DIR_1_4:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 12. (TIMI_MUXOEZ). 0 : sets direction of pin 12 of exp 3 as input 1 : sets direction of pin 12 of exp 3 as out	R/W
5	**EXP3_GPIO_DIR_1_5:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 13. (SoC_RESETFULLZ). 0 : sets direction of pin 13 of exp 3 as input 1 : sets direction of pin 13 of exp 3 as out	R/W
6	**EXP3_GPIO_DIR_1_6:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 14. (SoC_RESETZ). 0 : sets direction of pin 14 of exp 3 as input 1 : sets direction of pin 14 of exp 3 as out	R/W
7	**EXP3_GPIO_DIR_1_7:** This bit can be updated by the BMC software to drive the pin direction of expander 3 pin 15. (SoC_PORZ). 0 : sets direction of pin 15 of exp 3 as input 1 : sets direction of pin 15 of exp 3 as out	R/W

Register Address: **12h**
Register Name: **Expander4 Port0 Input (07-00 Low Byte) Register**
Default Value: ----
Attribute: Read Only

Bit	Description	Read
0	**PHY INT:** This bit reflects the state of the “PHY_INT” pin and writes will have no effect. 0 : PHY_INT state is low 1 : PHY_INT state is high	R
1	**EXPCON MCU RESETSTATZ[1]:** This bit reflects the state of the “EXP_CONMCURESETSTATZ” pin and writes will have no effect. 0 : EXP_CONMCURESETSTATZ state is low 1 : EXP_CONMCURESETSTATZ state is high	R
2	**EXT PS:** This bit reflects the state of the “EXT_PS” pin and writes will have no effect. 0 : EXT_PS state is low 1 : EXT_PS state is high	R
3	**RESERVED**	R
4	**RESERVED**	R
5	**CDCM2 REF SEL:** This bit reflects the state of the “CDCM2_REFSEL” pin and writes will have no effect. 0 : CDCM2_REFSEL state is low 1 : CDCM2_REFSEL state is high	R

6	**CDCM1 REF SEL:** This bit reflects the state of the “CDCM1_REFSEL” pin and writes will have no effect. 0 : CDCM1_REFSEL state is low 1 : CDCM1_REFSEL state is high	R
7	**RESERVED**	R

Register Address: **13h**
Register Name: **Expander4 Port1 Input (07-00 Low Byte) Register**
Default Value: ----
Attribute: Read Only

Bit	Description	Read
0	**CDCM1 REF SEL PD:** This bit reflects the state of the “CDCM1_REFSELPD” pin and writes will have no effect. 0 : CDCM1_REFSELPD state is low 1 : CDCM1_REFSELPD state is high	R
1	**CDCM2 REF SEL PD:** This bit reflects the state of the “CDCM2REFSELPD” pin and writes will have no effect. 0 : CDCM2REFSELPD state is low 1 : CDCM2REFSELPD state is high	R
2	**RESERVED**	R
3	**RESERVED**	R
4	**RESERVED**	R
5	**RESERVED**	R
6	**RESERVED**	R
7	**PHY INT2:** This bit reflects the state of the “PHYINT2” pin and writes will have no effect. 0 : PHYINT2 state is low 1 : PHYINT2 state is high	R

Register Address: **14h**
Register Name: **Expander4 Port0 Output (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**PHY INT1:** This bit can be updated by the BMC software to drive a high or low value on the “PHY_INT1” pin. 0 : PHY_INT1drives low 1 : PHY_INT1drives high	R/W
1	**EXPCON MCU RESETSTATZ:** This bit can be updated by the BMC software to drive a high or low value on the “EXP_CONMCURESETZ” pin. 0 : EXP_CONMCURESETZ drives low 1 : EXP_CONMCURESETZ drives high	R/W
2	**EXP PS:** This bit can be updated by the BMC software to drive a high or low value on the “EXP_PS” pin. 0 : EXP_PS drives low 1 : EXP_PS drives high	R/W
3	**RESERVED**	R/W
4	**RESERVED**	R/W
5	**CDCM2 REF SEL:** This bit can be updated by the BMC software to drive a high or low value on the “CDCM2_REFSEL” pin. 0 : CDCM2_REFSEL drives low 1 : CDCM2_REFSEL drives high	R/W
6	**CDCM1 REF SEL:** This bit can be updated by the BMC software to drive a high or low value on the “CDCM1_REFSEL” pin. 0 : CDCM1_REFSEL drives low 1 : CDCM1_REFSEL drives high	R/W
7	**RESERVED**	R/W

Register Address: **15h**
Register Name: **Expander4 Port1 Output (07-00 High Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write

0	**CDCM1 REFCLK1 PD:** This bit can be updated by the BMC software to drive a high or low value on the “CDCM1_REFCLK1PD” pin. 0 : CDCM1_REFCLK1PD drives low 1 : CDCM1_REFCLK1PD drives high	R/W
1	**CDCM2 REFCLK1 PD:** This bit can be updated by the BMC software to drive a high or low value on the “CDCM2_REFCLK1PD” pin. 0 : CDCM2_REFCLK1PD drives low 1 : CDCM2_REFCLK1PD drives high	R/W
2	**RESERVED**	R/W
3	**RESERVED**	R/W
4	**RESERVED**	R/W
5	**RESERVED**	R/W
6	**RESERVED**	R/W
7	**PHY INT2:** This bit can be updated by the BMC software to drive a high or low value on the “PHY_INT2” pin. 0 : PHY_INT2 drives low 1 : PHY_INT2 drives high	R/W

Register Address: **16h**
Register Name: **Expander4 Port0 Direction (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**EXP4_GPIO_DIR_0_0:** This bit can be updated by the BMC software to drive the pin direction of expander 4 pin 0. (PHY_INT1). 0 : sets direction of pin 0 of exp 4 as input 1 : sets direction of pin 0 of exp 4 as out	R/W

1	**EXP4_GPIO_DIR_0_1:** This bit can be updated by the BMC software to drive the pin direction of expander 4 pin 1. (EXP_CONMCURESETZ). 0 : sets direction of pin 1 of exp 4 as input 1 : sets direction of pin 1 of exp 4 as out	R/W
2	**EXP4_GPIO_DIR_0_2:** This bit can be updated by the BMC software to drive the pin direction of expander 4 pin 2. (EXP_PS). 0 : sets direction of pin 2 of exp 4 as input 1 : sets direction of pin 2 of exp 4 as out	R/W
3	**RESERVED**	R/W
4	**RESERVED**	R/W
5	**EXP4_GPIO_DIR_0_5:** This bit can be updated by the BMC software to drive the pin direction of expander 4 pin 5. (CDCM2_REFSEL). 0 : sets direction of pin 5 of exp 4 as input 1 : sets direction of pin 5 of exp 4 as out	R/W
6	**EXP4_GPIO_DIR_0_6:** This bit can be updated by the BMC software to drive the pin direction of expander 4 pin 6. (CDCM1_REFSEL). 0 : sets direction of pin 6 of exp 4 as input 1 : sets direction of pin 6 of exp 4 as out	R/W
7	**RESERVED**	R/W

Register Address: **17h**
Register Name: **Expander4 Port1 Direction (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**EXP4_GPIO_DIR_1_0:** This bit can be updated by the BMC software to drive the pin direction of expander 4 pin 8. (CDCM1_REFCLK1PD). 0 : sets direction of pin 8 of exp 4 as input 1 : sets direction of pin 8 of exp 4 as out	R/W
1	**EXP4_GPIO_DIR_1_1:** This bit can be updated by the BMC software to drive the pin direction of expander 4 pin 9. (CDCM2_REFCLK1PD). 0 : sets direction of pin 9 of exp 4 as input 1 : sets direction of pin 9 of exp 4 as out	R/W
2	**RESERVED**	R/W

3	**RESERVED**	R/W
4	**RESERVED**	R/W
5	**RESERVED**	R/W
6	**RESERVED**	R/W
7	**EXP4_GPIO_DIR_1_7:** This bit can be updated by the BMC software to drive the pin direction of expander 4 pin 15. (PHY_INT2). 0 : sets direction of pin 15 of exp 4 as input 1 : sets direction of pin 15 of exp 4 as out	R/W

Register Address: **18h**
Register Name: **Expander5 Port0 Input (07-00 Low Byte) Register**
Default Value: ----
Attribute: Read Only

Bit	Description	Read
0	**CLK MUXCTRL [2]:** This bit reflects the state of the "CLKMUXCTRL[0]" pin and writes will have no effect. 0 : CLKMUXCTRL2 state is low 1 : CLKMUXCTRL2 state is high	R
1	**CLK MUXCTRL [0]:** This bit reflects the state of the "CLKMUXCTRL[1]" pin and writes will have no effect. 0 : CLKMUXCTRL0 state is low 1 : CLKMUXCTRL0 state is high	R
2	**CLK MUXCTRL [1]:** This bit reflects the state of the "CLKMUXCTRL[2]" pin and writes will have no effect. 0 : CLKMUXCTRL1 state is low 1 : CLKMUXCTRL1 state is high	R
3	**SERDES SW1 SEL [0]:** This bit reflects the state of the "SERDESSW1SEL[0]" pin and writes will have no effect. 0 : SERDESSW1SEL0 state is low 1 : SERDESSW1SEL0 state is high	R
4	**SERDES SW1 SEL [1]:** This bit reflects the state of the "SERDESSW1SEL[1]" pin and writes will have no effect. 0 : SERDESSW1SEL1 state is low 1 : SERDESSW1SEL1 state is high	R

5	**SERDES SW2 SEL [0]:** This bit reflects the state of the "SERDESSW2SEL[0]" pin and writes will have no effect. 0 : SERDESSW2SEL0 state is low 1 : SERDESSW2SEL0 state is high	R
6	**SERDES SW2 SEL [1]:** This bit reflects the state of the "SERDESSW2SEL[1]" pin and writes will have no effect. 0 : SERDESSW2SEL1 state is low 1 : SERDESSW2SEL1 state is high	R
7	**SERDES SW3 SEL [0]:** This bit reflects the state of the "SERDESSW3SEL[0]" pin and writes will have no effect. 0 : SERDESSW3SEL0 state is low 1 : SERDESSW3SEL0 state is high	R

Register Address: **19h**
Register Name: **Expander5 Port1 Input (07-00 Low Byte) Register**
Default Value: ----
Attribute: Read Only

Bit	Description	Read
0	**SERDES SW3 SEL [1]:** This bit reflects the state of the "SERDESSW3SEL[1]" pin and writes will have no effect. 0 : SERDESSW3SEL1 state is low 1 : SERDESSW3SEL1 state is high	R
1	**DONE FPGA:** This bit reflects the state of the "DONEFPGA" pin and writes will have no effect. 0 : DONEFPGA state is low 1 : DONEFPGA state is high	R
2	**EXP GPIO EN:** This bit reflects the state of the "EXPGPIOEN" pin and writes will have no effect. 0 : EXPGPIOEN state is low 1 : EXPGPIOEN state is high	R
3	**RESERVED**	R
4	**RESERVED**	R
5	**RESERVED**	R
6	**RESERVED**	R

7	**RESERVED**	R

Register Address: **1Ah**
Register Name: **Expander5 Port0 Output (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**CLK MUXCTRL [2]:** This bit can be updated by the BMC software to drive a high or low value on the “CLKMUXCTRL0” pin. 0 :CLKMUXCTRL2 drives low 1 : CLKMUXCTRL2 drives high	R/W
1	**CLK MUXCTRL [0]:** This bit can be updated by the BMC software to drive a high or low value on the “CLKMUXCTRL1” pin. 0 :CLKMUXCTRL0 drives low 1 : CLKMUXCTRL0 drives high	R/W
2	**CLK MUXCTRL [1]:** This bit can be updated by the BMC software to drive a high or low value on the “CLKMUXCTRL2” pin. 0 :CLKMUXCTRL1 drives low 1 : CLKMUXCTRL1 drives high	R/W
3	**SERDES SW1 SEL [0]:** This bit can be updated by the BMC software to drive a high or low value on the “SERDESSW1SEL0” pin. 0 : SERDESSW1SEL0 drives low 1 : SERDESSW1SEL0 drives high	R/W
4	**SERDES SW1 SEL [1]:** This bit can be updated by the BMC software to drive a high or low value on the “SERDESSW1SEL1” pin. 0 : SERDESSW1SEL1 drives low 1 : SERDESSW1SEL1 drives high	R/W
5	**SERDES SW2 SEL [0]:** This bit can be updated by the BMC software to drive a high or low value on the “SERDESSW2SEL0” pin. 0 : SERDESSW2SEL0 drives low 1 : SERDESSW2SEL0 drives high	R/W
6	**SERDES SW2 SEL [1]:** This bit can be updated by the BMC software to drive a high or low value on the “SERDESSW2SEL1” pin. 0 : SERDESSW2SEL1 drives low 1 : SERDESSW2SEL1 drives high	R/W
7	**SERDES SW3 SEL [0]:** This bit can be updated by the BMC software to drive a high or low value on the “SERDESSW3SEL0” pin. 0 : SERDESSW3SEL0 drives low 1 : SERDESSW3SEL0 drives high	R/W

Register Address: **1Bh**
Register Name: **Expander5 Port1 Output (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**SERDES SW3 SEL [1]:** This bit can be updated by the BMC software to drive a high or low value on the “SERDESSW3SEL1” pin. 0 : SERDESSW3SEL1 drives low 1 : SERDESSW3SEL1 drives high	R/W
1	**DONE FPGA:** This bit can be updated by the BMC software to drive a high or low value on the “DONE_FPGA” pin. 0 : DONE_FPGA drives low 1 : DONE_FPGA drives high	R/W
2	**EXP GPIO EN:** This bit can be updated by the BMC software to drive a high or low value on the “EXP_GPIO_EN” pin. 0 : EXP_GPIO_EN drives low 1 : EXP_GPIO_EN drives high	R/W
3	**RESERVED**	R/W
4	**RESERVED**	R/W
5	**RESERVED**	R/W
6	**RESERVED**	R/W
7	**RESERVED**	R/W

Register Address: **1Ch**
Register Name: **Expander5 Port0 Direction (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**EXP5_GPIO_DIR_0_0:** This bit can be updated by the BMC software to drive the pin direction of expander 5 pin 0. (CLKMUXCTRL0). 0 : sets direction of pin 0 of exp 5 as input 1 : sets direction of pin 0 of exp 5 as out	R/W
1	**EXP5_GPIO_DIR_0_1:** This bit can be updated by the BMC software to drive the pin direction of expander 5 pin 1. (CLKMUXCTRL1). 0 : sets direction of pin 1 of exp 5 as input 1 : sets direction of pin 1 of exp 5 as out	R/W
2	**EXP5_GPIO_DIR_0_2:** This bit can be updated by the BMC software to drive the pin direction of expander 5 pin 2. (CLKMUXCTRL2). 0 : sets direction of pin 2 of exp 5 as input 1 : sets direction of pin 2 of exp 5 as out	R/W
3	**EXP5_GPIO_DIR_0_3:** This bit can be updated by the BMC software to drive the pin direction of expander 5 pin 3. (SERDES_SW1_SEL0). 0 : sets direction of pin 3 of exp 5 as input 1 : sets direction of pin 3 of exp 5 as out	R/W
4	**EXP5_GPIO_DIR_0_4:** This bit can be updated by the BMC software to drive the pin direction of expander 5 pin 4. (SERDES_SW1_SEL1). 0 : sets direction of pin 4 of exp 5 as input 1 : sets direction of pin 4 of exp 5 as out	R/W
5	**EXP5_GPIO_DIR_0_5:** This bit can be updated by the BMC software to drive the pin direction of expander 5 pin 5. (SERDES_SW2_SEL0). 0 : sets direction of pin 5 of exp 5 as input 1 : sets direction of pin 5 of exp 5 as out	R/W
6	**EXP5_GPIO_DIR_0_6:** This bit can be updated by the BMC software to drive the pin direction of expander 5 pin 6. (SERDES_SW2_SEL1). 0 : sets direction of pin 6 of exp 5 as input 1 : sets direction of pin 6 of exp 5 as out	R/W
7	**EXP5_GPIO_DIR_0_7:** This bit can be updated by the BMC software to drive the pin direction of expander 5 pin 7. (SERDES_SW3_SEL0). 0 : sets direction of pin 7 of exp 5 as input 1 : sets direction of pin 7 of exp 5 as out	R/W

Register Address: **1Dh**
Register Name: **Expander5 Port1 Direction (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**EXP5_GPIO_DIR_1_0:** This bit can be updated by the BMC software to drive the pin direction of expander 5 pin 8. (SERDES_SW3_SEL1). 0 : sets direction of pin 8 of exp 5 as input 1 : sets direction of pin 8 of exp 5 as out	R/W

1	**EXP5_GPIO_DIR_1_1:** This bit can be updated by the BMC software to drive the pin direction of expander 5 pin 9. (DONE_FPGA). 0 : sets direction of pin 9 of exp 5 as input 1 : sets direction of pin 9 of exp 5 as out	R/W
2	**EXP5_GPIO_DIR_1_2:** This bit can be updated by the BMC software to drive the pin direction of expander 5 pin 10. (EXP_GPIO_EN). 0 : sets direction of pin 10 of exp 5 as input 1 : sets direction of pin 10 of exp 5 as out	R/W
3	**RESERVED**	R/W
4	**RESERVED**	R/W
5	**RESERVED**	R/W
6	**RESERVED**	R/W
7	**RESERVED**	R/W

Register Address: **1Eh**
Register Name: **Interrupt register for Expander (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**INT CLR REGD [0]:** This bit can be updated by the BMC software to drive a high or low value on the “INTCLRREGD0”(INT for Exp - 1) pin. 0 : INTCLRREGD0 drives low 1 : INTCLRREGD0 drives high	R/W
1	**INT CLR REGD[1]:** This bit can be updated by the BMC software to drive a high or low value on the “INTCLRREGD1”(INT for Exp - 2) pin. 0 : INTCLRREGD1 drives low 1 : INTCLRREGD1 drives high	R/W

2	**INT CLR REGD [2]:** This bit can be updated by the BMC software to drive a high or low value on the “INTCLRREGD2”(INT for Exp - 3) pin. 0 : INTCLRREGD2 drives low 1 : INTCLRREGD2 drives high	R/W
3	**INT CLR REGD [3]:** This bit can be updated by the BMC software to drive a high or low value on the “INTCLRREGD3”(INT for Exp - 4) pin. 0 : INTCLRREGD3 drives low 1 : INTCLRREGD3 drives high	R/W
4	**INT CLR REGD [4]:** This bit can be updated by the BMC software to drive a high or low value on the “INTCLRREGD4”(INT for Exp - 5) pin. 0 : INTCLRREGD4 drives low 1 : INTCLRREGD4 drives high	R/W
5	**RESERVED**	R/W
6	**RESERVED**	R/W
7	**RESERVED**	R/W

Register Address: **1Fh**
Register Name: **Debug LED (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**LED ON OFF [0]:** This bit can be updated by the BMC software to drive a high or low value on the “LEDONOFF0” pin. 0 : LEDONOFF0 drives low (LED OFF) 1 : LEDONOFF0 drives high(LED ON)	R/W
1	**LED ON OFF [1]:** This bit can be updated by the BMC software to drive a high or low value on the “LEDONOFF1” pin. 0 : LEDONOFF1 drives low (LED OFF) 1 : LEDONOFF1 drives high(LED ON)	R/W
2	**LED ON OFF [2]:** This bit can be updated by the BMC software to drive a high or low value on the “LEDONOFF2” pin. 0 : LEDONOFF2 drives low (LED OFF) 1 : LEDONOFF2 drives high(LED ON)	R/W

3	**LED ON OFF [3]:** This bit can be updated by the BMC software to drive a high or low value on the “LEDONOFF3” pin. 0 : LEDONOFF3 drives low (LED OFF) 1 : LEDONOFF3 drives high(LED ON)	R/W
4	**RESERVED**	R/W
5	**RESERVED**	R/W
6	**RESERVED**	R/W
7	**RESERVED**	R/W

Register Address: **20h**
Register Name: **BMC_BOOT_TIMO0 (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**BMC BOOT TIMO0 EN:** This bit can be updated by the BMC software to drive a high or low value on the “BMC_BOOT_TIMO0_EN” pin. 0 : BMC_BOOT_TIMO0_EN drives low 1 : BMC_BOOT_TIMO0_EN drives high	R/W
1	**BMC BOOT TIMO0 WR:** This bit can be updated by the BMC software to drive a high or low value on the “BMC_BOOT_TIMO0_WR” pin. 0 : BMC_BOOT_TIMO0_WR drives low 1 : BMC_BOOT_TIMO0_WR drives high	R/W
2	**RESERVED**	R/W
3	**RESERVED**	R/W

4	**RESERVED**	R/W
5	**RESERVED**	R/W
6	**RESERVED**	R/W
7	**RESERVED**	R/W

Register Address: **21h**
Register Name: **BMC_BOOT_TIMO1 (07-00 Low Byte) Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**BMC BOOT TIMO1 EN:** This bit can be updated by the BMC software to drive a high or low value on the “BMC_BOOT_TIMO1_EN” pin. 0 : BMC_BOOT_TIMO1_EN drives low 1 : BMC_BOOT_TIMO1_EN drives high	R/W
1	**BMC BOOT TIMO1 WR:** This bit can be updated by the BMC software to drive a high or low value on the “BMC_BOOT_TIMO1_WR” pin. 0 : BMC_BOOT_TIMO1_WR drives low 1 : BMC_BOOT_TIMO1_WR drives high	R/W
2	**RESERVED**	R/W
3	**RESERVED**	R/W
4	**RESERVED**	R/W

5	**RESERVED**	R/W
6	**RESERVED**	R/W
7	**RESERVED**	R/W

Register Address: **22h**
Register Name: **FPGA REVISON ID (07-00 Low Byte) Register**
Default Value: ----
Attribute: READ

Bit	Description	Read/Write
7:0	**FPGA BIT VERSION:** This bit reflects the state of the "FPGABITVERSION" pin and writes will have no effect. 0 : FPGABITVERSION state is low 1 : FPGABITVERSION state is high	R

5.7.2 FPGA Configuration Register accessible from SoC

The below table summarizes the list of registers which are accessible from TCI6630K2L SPI. All GPIOs, SPI bus, LMK SPI bus, status and control signals of AFE7500EVM are accessible by TCI6630K2L SPI bus0.

Table 5.6: TCI6630K2L FPGA Configuration Registers Summary

Address	Register Name	Attribute (R/W) (RO : Read-Only)	Default Value
0x00	SPL Status Register Address	R/W	0x00
0x01	Marconi0 Gpio0 Direction Register	R/W	0x00
0x02	Marconi0 Gpio0 Input Data Register	RO	XX
0x03	Marconi0 Gpio0 Output Register	R/W	0x00
0x04	Marconi0 Gpio1 Direction Register	R/W	0x00
0x05	Marconi0 Gpio1 Input Data Register	RO	XX
0x06	Marconi0 Gpio1 Output Register	R/W	0x00
0x07	Marconi0 Gpio3 Direction Register	R/W	0x00
0x08	Marconi0 Gpio3 Input Data Register	RO	XX
0x09	Marconi0 Gpio3 Output Register	R/W	0x00
0x0A	Marconi1 Gpio0 Direction Register	R/W	0x00
0x0B	Marconi1 Gpio0 Input Data Register	RO	XX
0x0C	Marconi1 Gpio0 Output Register	R/W	0x00
0x0D	Marconi1 Gpio1 Direction Register	R/W	0x00
0x0E	Marconi1 Gpio1 Input Data Register	RO	XX
0x0F	Marconi1 Gpio1 Output Register	R/W	0x00
0x10	Marconi1 Gpio3 Direction Register	R/W	0x00
0x11	Marconi1 Gpio3 Input Data Register	RO	XX
0x12	Marconi1 Gpio3 Output Register	R/W	0x00
0x13	Marconi0 Status Register	RO	XX
0x14	Marconi1 Status Register	RO	XX
0x18	SYSREF CONTROL REGISTER	R/W	0x00
0x19	SYSREF SPI GPIO REGISTER	R/W	0x00
0x1A	SOC TIMER0 CONTROL REGISTER	R/W	0x00
0x1B	SOC TIMER1 CONTROL REGISTER	R/W	0x00
0x1C	FMC LED DATA Register	R/W	0x00
0x1D	FPGA SEL TX RX Pulse	R/W	0x00

0x1E	LMK Start Bit Register	R/W	0x00
0x1F	LMK SPI Address MSB Register	R/W	0x00
0x20	LMK SPI Address LSB Register	R/W	0x00
0x21	LMK SPI Data Register	R/W	0x00
0x22	LMK SPI CS SEL Register	R/W	0x00
0x23	LMK RDATA IN Register	RO	XX
0x24	ROM DATA SEL Register	R/W	0x00
0x25	CLR MRC GPIO Register	R/W	0x00
0x26	FPGA UPDATE Register	R/W	0x00
0x27	LMK CFG BUSY STATUS Register	RO	XX

5.7.2.1 FPGA Configuration Register Descriptions

Register Address: **00h**
Register Name: **SPL Status Register Address**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	MAR0_IRQ: Indicates interrupt to AFE7500 and it is controlled by SoC SPI.	R/W
1	MAR1_IRQ: Indicates interrupt to AFE7500 and it is controlled by SoC SPI.	R/W
7:2	**RESERVED**	

Register Address: **01h**
Register Name: **Marconi0 Gpio0 Direction Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
0	**MAR0_GPIO0_DIR [0]:** This bit can be updated by the SOC software to drive the pin direction. 0 : Corresponding bit of register MAR0_GPIO0_DIR0 is driven In 1 : Corresponding bit of register MAR0_GPIO0_DIR0 is driven Out	R/W

1	**MAR0_GPIO0_DIR [1]:** This bit can be updated by the SOC software to drive the pin direction. 0 : Corresponding bit of register MAR0_GPIO0_DIR1 is driven In 1 : Corresponding bit of register MAR0_GPIO0_DIR1 is driven Out	R/W
2	**MAR0_GPIO0_DIR [2]:** This bit can be updated by the SOC software to drive the pin direction. 0 : Corresponding bit of register MAR0_GPIO0_DIR2 is driven In 1 : Corresponding bit of register MAR0_GPIO0_DIR2 is driven Out	R/W
3	**MAR0_GPIO0_DIR [3]:** This bit can be updated by the SOC software to drive the pin direction. 0 : Corresponding bit of register MAR0_GPIO0_DIR3 is driven In 1 : Corresponding bit of register MAR0_GPIO0_DIR3 is driven Out	R/W
4	**MAR0_GPIO0_DIR [4]:** This bit can be updated by the SOC software to drive the pin direction. 0 : Corresponding bit of register MAR0_GPIO0_DIR4 is driven In 1 : Corresponding bit of register MAR0_GPIO0_DIR4 is driven Out	R/W
5	**MAR0_GPIO0_DIR [5]:** This bit can be updated by the SOC software to drive the pin direction. 0 : Corresponding bit of register MAR0_GPIO0_DIR5 is driven In 1 : Corresponding bit of register MAR0_GPIO0_DIR5 is driven Out	R/W
6	**MAR0_GPIO0_DIR [6]:** This bit can be updated by the SOC software to drive the pin direction. 0 : Corresponding bit of register MAR0_GPIO0_DIR6 is driven In 1 : Corresponding bit of register MAR0_GPIO0_DIR6 is driven Out	R/W
7	**MAR0_GPIO0_DIR [7]:** This bit can be updated by the SOC software to drive the pin direction. 0 : Corresponding bit of register MAR0_GPIO0_DIR7 is driven In 1 : Corresponding bit of register MAR0_GPIO0_DIR7 is driven Out	R/W

Register Address: **02h**
Register Name: **Marconi0 Gpio0 Input Data Register**
Default Value: ----
Attribute: Read

Bit	Description	Read/Write
7:0	**MAR0 GPIO0 DIR:** Select direction for MARCONI0_GPIO0[7:0] i/o pins, one bit for each pin. If value of MAR0_GPIO0_DIR[n] bit of this register is 0, MARCONI0_GPIO0 [n] pin will act as Input. If value of MAR0_GPIO0_DIR[n] bit of this register is 1, MARCONI0_GPIO0[n] pin will act as Output, n varies from 0 to 7.	R

Register Address: **03h**
Register Name: **Marconi0 Gpio0 Output Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write

7:0	**MAR0 GPIO0 OUT:** When MAR0_GPIO0_DIR[n] bit of MARCONI0_GPIO0_DIR_REG is set to 1 i.e. output, value of MAR0_GPIO0_OUT[n] bit of this register will be driven to MARCONI0_GPIO0 [n] pin, n varies from 0 to 7.	R/W

Register Address: **04h**
Register Name: **Marconi0 Gpio1 Direction Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
7:0	**MAR0 GPIO1 DIR:** Select direction for MARCONI0_GPIO1[7:0] i/o pins, one bit for each pin. If value of MAR0_GPIO1_DIR[n] bit of this register is 0, MARCONI0_GPIO1[n] pin will act as Input. If value of MAR0_GPIO1_DIR[n] bit of this register is 1, MARCONI0_GPIO1[n] pin will act as Output. n varies from 0 to 7.	R/W

Register Address: **05h**
Register Name: **Marconi0 Gpio1 Input Data Register**
Default Value: ----
Attribute: Read

Bit	Description	Read/Write
7:0	**MAR0 GPIO1 IN:** When MAR0_GPIO1_DIR[n] bit of MARCONI0_GPIO1_DIR_REG is set to 0 i.e. input, value of MARCONI0_GPIO1[n] pin will be captured into MAR0_GPIO1_IN[n] bit of this register. When MAR0_GPIO1_DIR[n] bit of MARCONI0_GPIO1_DIR_REG is set to 1 i.e. output, MAR0_GPIO1_OUT[n] bit of MARCONI0_GPIO1_OUTPUT_REG will be captured into MAR0_GPIO1_IN[n] bit of this register. n varies from 0 to 7.	R

Register Address: **06h**
Register Name: **Marconi0 Gpio1 Output Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write

7:0	**MAR0 GPIO1 OUT:** When MAR0_GPIO1_DIR[n] bit of MARCONI0_GPIO1_DIR_REG is set to 1 i.e. output, value of MAR0_GPIO1_OUT[n] bit of this register will be driven to MARCONI0_GPIO1[n] pin. n varies from 0 to 7.	R/W

Register Address: **07h**
Register Name: **Marconi0 Gpio3 Direction Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
7:0	**MAR0 GPIO3 DIR:** Select direction for MARCONI0_GPIO3[7:0] i/o pins, one bit for each pin. If value of MAR0_GPIO3_DIR[n] bit of this register is 0, MARCONI0_GPIO3[n] pin will act as Input. If value of MAR0_GPIO3_DIR[n] bit of this register is 1, MARCONI0_GPIO3[n] pin will act as Output. n varies from 0 to 7.	R/W

Register Address: **08h**
Register Name: **Marconi0 Gpio3 Input Data Register**
Default Value: ----
Attribute: Read

Bit	Description	Read/Write
7:0	**MAR0 GPIO3 IN:** When MAR0_GPIO3_DIR[n] bit of MARCONI0_GPIO3_DIR_REG is set to 0 i.e. input, value of MARCONI0_GPIO3 [n] pin will be captured into MAR0_GPIO3_IN[n] bit of this register. When MAR0_GPIO3_DIR[n] bit of MARCONI0_GPIO3_DIR_REG is set to 1 i.e. output, MAR0_GPIO3_OUT[n] bit of MARCONI0_GPIO3_OUTPUT_REG will be captured into MAR0_GPIO3_IN[n] bit of this register. n varies from 0 to 7.	R

Register Address: **09h**
Register Name: **Marconi0 Gpio3 Output Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write

7:0	**MAR0 GPIO3 OUT:** When MAR0_GPIO3_DIR[n] bit of MARCONI0_GPIO3_DIR_REG is set to 1 i.e. output, value of MAR0_GPIO3_OUT[n] bit of this register will be driven to MARCONI0_GPIO3 [n] pin. n varies from 0 to 7.	R/W

Register Address: **0x0Ah**
Register Name: **Marconi1 Gpio0 Direction Register**
Default Value: 00
Attribute: Read/Write

Bit	Description	Read/Write
7:0	**MAR1 GPIO0 DIR:** Select direction for MARCONI1_GPIO0[7:0] i/o pins, one bit for each pin. If value of MAR1_GPIO0_DIR[n] bit of this register is 0, MARCONI1_GPIO0[n] pin will act as Input. If value of MAR1_GPIO0_DIR[n] bit of this register is 1, MARCONI1_GPIO0[n] pin will act as Output. n varies from 0 to 7.	R/W

Register Address: **0x0Bh**
Register Name: **Marconi1 Gpio0 Input Data Register**
Default Value: ----
Attribute: Read

Bit	Description	Read/Write
7:0	**MAR1 GPIO0 IN:** When MAR1_GPIO0_DIR[n] bit of MARCONI1_GPIO0_DIR_REG is set to 0 i.e. input, value of MARCONI1_GPIO0[n] pin will be captured into MAR1_GPIO0_IN[n] bit of this register. When MAR1_GPIO0_DIR[n] bit of MARCONI1_GPIO0_DIR_REG is set to 1 i.e. output, MAR1_GPIO0_OUT[n] bit of MARCONI1_GPIO0_OUTPUT_REG will be captured into MAR1_GPIO0_IN[n] bit of this register. n varies from 0 to 7.	R

Register Address: **0x0Ch**
Register Name: **Marconi1 Gpio0 Output Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
7:0	**MAR1 GPIO0 OUT:** When MAR1_GPIO0_DIR[n] bit of MARCONI1_GPIO0_DIR_REG is set to 1 i.e. output, value of MAR1_GPIO0_OUT[n] bit of this register will be driven to MARCONI1_GPIO0[n] pin. n varies from 0 to 7.	R/W

Register Address: **0x0Dh**
Register Name: **Marconi1 Gpio1 Direction Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
7:0	**MAR1 GPIO1 DIR:** Select direction for MARCONI1_GPIO1[7:0] i/o pins, one bit for each pin. If value of MAR1_GPIO1_DIR[n] bit of this register is 0, MARCONI1_GPIO1[n] pin will act as Input. If value of MAR1_GPIO1_DIR[n] bit of this register is 1, MARCONI1_GPIO1[n] pin will act as Output. n varies from 0 to 7.	R/W

Register Address: **0x0Eh**
Register Name: **Marconi1 Gpio1 Input Data Register**
Default Value: ----
Attribute: Read

Bit	Description	Read/Write
7:0	**MAR1 GPIO1 IN:** When MAR1_GPIO1_DIR[n] bit of MARCONI1_GPIO1_DIR_REG is set to 0 i.e. input, value of MARCONI1_GPIO1[n] pin will be captured into MAR1_GPIO1_IN[n] bit of this register. When MAR1_GPIO1_DIR[n] bit of MARCONI1_GPIO1_DIR_REG is set to 1 i.e. output, MAR1_GPIO1_OUT[n] bit of MARCONI1_GPIO1_OUTPUT_REG will be captured into MAR1_GPIO1_IN[n] bit of this register. n varies from 0 to 7.	R

Register Address: **0x0Fh**
Register Name: **Marconi1 Gpio1 Output Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
7:0	**MAR1 GPIO1 OUT:** When MAR1_GPIO1_DIR[n] bit of MARCONI1_GPIO1_DIR_REG is set to 1 i.e. output, value of MAR1_GPIO1_OUT[n] bit of this register will be driven to MARCONI1_GPIO1 [n] pin, n varies from 0 to 7.	R/W

Register Address: **0x10h**
Register Name: **Marconi1 Gpio3 Direction Register**

Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
7:0	**MAR1 GPIO3 DIR:** Select direction for MARCONI1_GPIO3[7:0] i/o pins, one bit for each pin. If value of MAR1_GPIO3_DIR[n] bit of this register is 0, MARCONI1_GPIO3[n] pin will act as Input. If value of MAR1_GPIO3_DIR[n] bit of this register is 1, MARCONI1_GPIO3[n] pin will act as Output. n varies from 0 to 7.	R/W

Register Address: **0x11h**
Register Name: **Marconi1 Gpio3 Input Data Register**
Default Value: ----
Attribute: Read

Bit	Description	Read/Write
7:0	**MAR1 GPIO3 IN:** When MAR1_GPIO3_DIR[n] bit of MARCONI1_GPIO3_DIR_REG is set to 0 i.e. input, value of MARCONI1_GPIO3[n] pin will be captured into MAR1_GPIO3_IN[n] bit of this register. When MAR1_GPIO3_DIR[n] bit of MARCONI1_GPIO3_DIR_REG is set to 1 i.e. output, MAR1_GPIO3_OUT[n] bit of MARCONI1_GPIO3_OUTPUT_REG will be captured into MAR1_GPIO3_IN[n] bit of this register. n varies from 0 to 7.	R

Register Address: **0x12h**
Register Name: **Marconi1 Gpio3 Output Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
7:0	**MAR1 GPIO3 OUT:** When MAR1_GPIO3_DIR[n] bit of MARCONI1_GPIO3_DIR_REG is set to 1 i.e. output, value of MAR1_GPIO3_OUT[n] bit of this register will be driven to MARCONI1_GPIO3[n] pin. n varies from 0 to 7.	R/W

Register Address: **0x13h**
Register Name: **Marconi0 Status Register**
Default Value: ----
Attribute: Read

Bit	Description	Read/Write
1:0	**MAR0 STATUS:** Captures Status of 2-bit MARCONI0_STATUS pins.	R
2	**MAR0 BUSY :** Captures MARCONI0_BUSY_Z pin.	R

7:3	**RESERVED**	---

Register Address: **0x14h**
Register Name: **Marconi1 Status Register**
Default Value: ----
Attribute: Read

Bit	Description	Read/Write
1:0	**MAR1 STATUS:** Captures Status of 2-bit MARCONI1_STATUS pins.	R
2	**MAR1 BUSY :** Captures MARCONI1_BUSY_Z pin.	R
7:3	**RESERVED**	---

Register Address: **0x18h**
Register Name: **SYSREF CONTROL REGISTER**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
1:0	**I_ANDLOGIC SEL:** Mux selection bits for selecting andlogic outputs. 2'b00 selects selects default (zero) value of 1st input to the mux, 2'b01 selects andlogc1, 2'b10 selects andlogc2 and 2'b11 selects andlogc3 .	R/W
4:2	**I_DLSYNC CNT:** This is a down counter value used for DLSYNC generation.	R/W
7:5	**RESERVED**	----

Register Address: **0x19h**
Register Name: **SYSREF SPI GPIO REGISTER**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
0	**I_MUX IN SYSREF FREQ:** This is one input to the 2:1 mux in the sysref.	R/W
1	**I_MUX CTRL SYSREF FREQ:** This is control bit for the 2:1 mux in the sysref.	R/W
7:2	**RESERVED**	----

Register Address: **0x1Ah**
Register Name: **SOC TIMER0 CONTROL REGISTER**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
1:0	**I_SOC TIMER0 MUX CTRL[1:0]:** These are selection lines for timer0 4:1 multiplexer. 2'b00 selects 0, 2'b01 selects 1, 2'b10 selects AMC_TIMO0, 2'b11 selects EXP_TIMO0.	R/W
7:2	**RESERVED**	----

Register Address: **0x1Bh**
Register Name: **SOC TIMER1 CONTROL REGISTER**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
1:0	**I_SOC TIMER1 MUX CTRL[1:0]:** These are selection lines for timer1 4:1 multiplexer.2'b00 selects 0, 2'b01 selects 1, 2'b10 selects EXP_TIMO1, 2'b11 selects EXTFRAMEEVENT.	R/W
7:2	**RESERVED**	----

Register Address: **0x1Ch**
Register Name: **FMC LED DATA Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
3:0	**LED ON OFF:** Each bit control one LED. If bit is set to 1, LED belongs to that bit will be turned ON. If bit is set to 0, LED belongs to that bit will be turned OFF.BMC SPI also can read/write this register. So this register should not be written or read at the same time by BMC and FMC SPI.	R/W
7:4	**RESERVED**	---

Register Address: **0x1Dh**
Register Name: **FPGA SEL TX RX Pulse**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
0	**O FPGA SPI BIT:** when o_fpga_spi_bit = '1' tx_cap_pulse is enabled else if set '0' then rx_cap_pulse enabled	R/W

7:1	**RESERVED**	---

Register Address: **0x1Eh**
Register Name: **LMK Start Bit Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
0	**LMK START BIT:** If set to '1' auto sequence is selected else if set '0' manual config is selected.	R/W
7:1	**RESERVED**	---

Register Address: **0x1Fh**
Register Name: **LMK SPI Address MSB Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
7:0	LMK SPI ADDRESS MSB: Upper 8 bit address of LMK 16 bit address.	R/W

Register Address: **0x20h**
Register Name: **LMK SPI Address LSB Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
7:0	LMK SPI ADDRESS LSB: Lower 8 bit address of LMK 16 bit address.	R/W

Register Address: **0x21h**
Register Name: **LMK SPI Data Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
7:0	LMK SPI DATA REGISTER: Configuration Data to be written on LMK chip	R/W

Register Address: **0x22h**
Register Name: **LMK SPI CS SEL Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
0	**LMK SPI CS SEL REGISTER:** If set to '1' LMK0 is selected for communication.	R/W
1	**LMK SPI CS SEL REGISTER:** If set to '1' LMK1 is selected for communication	R/W
7:2	**RESERVED**	---

Register Address: **0x23h**
Register Name: **LMK RDATA IN Register**
Default Value: ----
Attribute: Read

Bit	Description	Read/Write
7:0	**I_LMK RDATA REGISTER:** Read data from LMK chip	R

Register Address: **0x24h**
Register Name: **ROM DATA SEL Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
1:0	**LMK ROM DATA SEL REGISTER:** If set to "00" dataset 0 is selected for LMK configuration. If set to "01" dataset 1 is selected for LMK configuration. If set to "10" dataset 2 is selected for LMK configuration. Default setting is for dataset 0 for LMK configuration.	R/W
7:2	**RESERVED**	---

Register Address: **0x25h**
Register Name: **CLR MRC GPIO Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
0	CLR MRC GPIO: If set to '1' all MRC_GPIOs will force output to Zero. Else if set '0' then worked as normal GPIO's. Default is ‘0’.	R/W

7:1	**RESERVED**	---

Register Address: **0x26h**
Register Name: **FPGA UPDATE Register**
Default Value: 0x00
Attribute: Read/Write

Bit	Description	Read/Write
0	**FPGA UPDATE WR:** If set to '1' then SOC_SPI will have control over 4 SOC_GPIO's for booting/storing image file in SPI MACRO. Else if set '0' then BMC_SPI will have control over 4 SOC_GPIO's.	R/W
7:1	**RESERVED**	---

Register Address: **0x27h**
Register Name: **LMK CFG BUSY STATUS Register**
Default Value: ---
Attribute: Read

Bit	Description	Read/Write
0	**LMK CFG BUSY STATUS:** If set to '1' indicates cfg to LMK chip by auto sequence is in progress. If set to '0' indicates cfg to LMK chip by auto sequence is done.	R
1	**LMK CFG BUSY STATUS:** If set to '1' indicates cfg to LMK chip by auto sequence is in progress. If set to '0' indicates cfg to LMK chip by	R
7:2	**RESERVED**	----

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