

K2E SCHEMATIC

MAJOR REVISION HISTORY :

PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	1.0	Proto Build	15-NOV-2013
2.0	2.0	Alpha Build	05-MAR-2014
2.0	2.01	Alpha ECNs Implemented	24-APR-2014

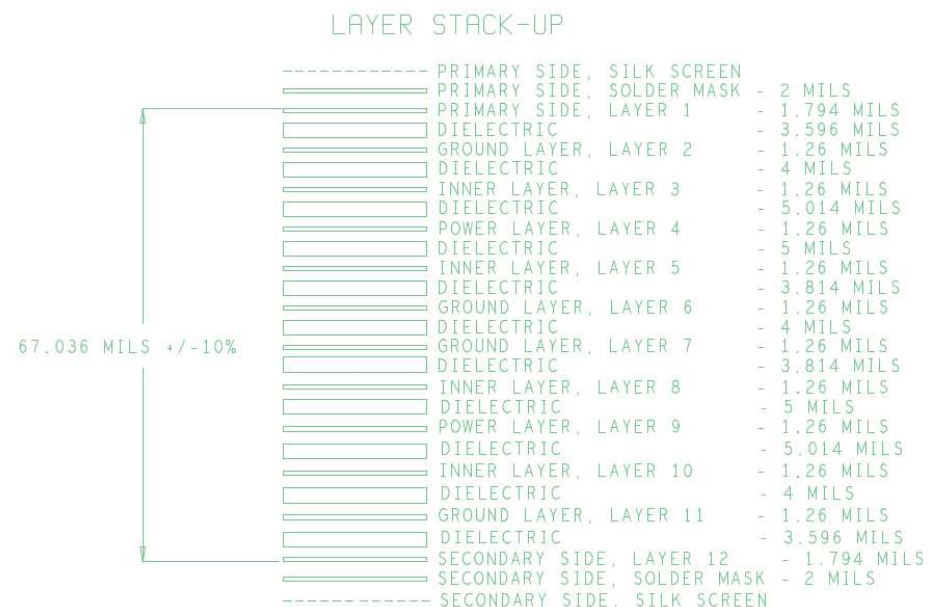
I2C ADDRESS TABLE :

REF DES	DESCRIPTION	7 BIT ADDRESS
EEPROM1	1MBit I2C EEPROM	0x50
SODIMM	SODIMM EEPROM	0x53
U4	UCD9090	0x68

PCB MECHANICAL DETAILS :

1. PCB SIZE: 7.11" x 2.89" x 0.063"
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

PCB LAYER STACK-UP DETAILS :



NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.



DISCLAIMER: THIS CIRCUIT DESIGN IS PROVIDED AS REFERENCE ONLY, WITHOUT WARRANTY EXPRESSED OR IMPLIED. THE USER IS ENCOURAGED TO PERFORM ALL DUE DILIGENCE WITH RESPECT TO DESIGN AND ANALYSIS. FOR COMMITTED PERFORMANCE AND FUNCTIONALITY, PLEASE REFER TO THE DEVICE DATA MANUAL.

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Project K2E EVM		Designed for TI by einfochips	
Title COVER PAGE			
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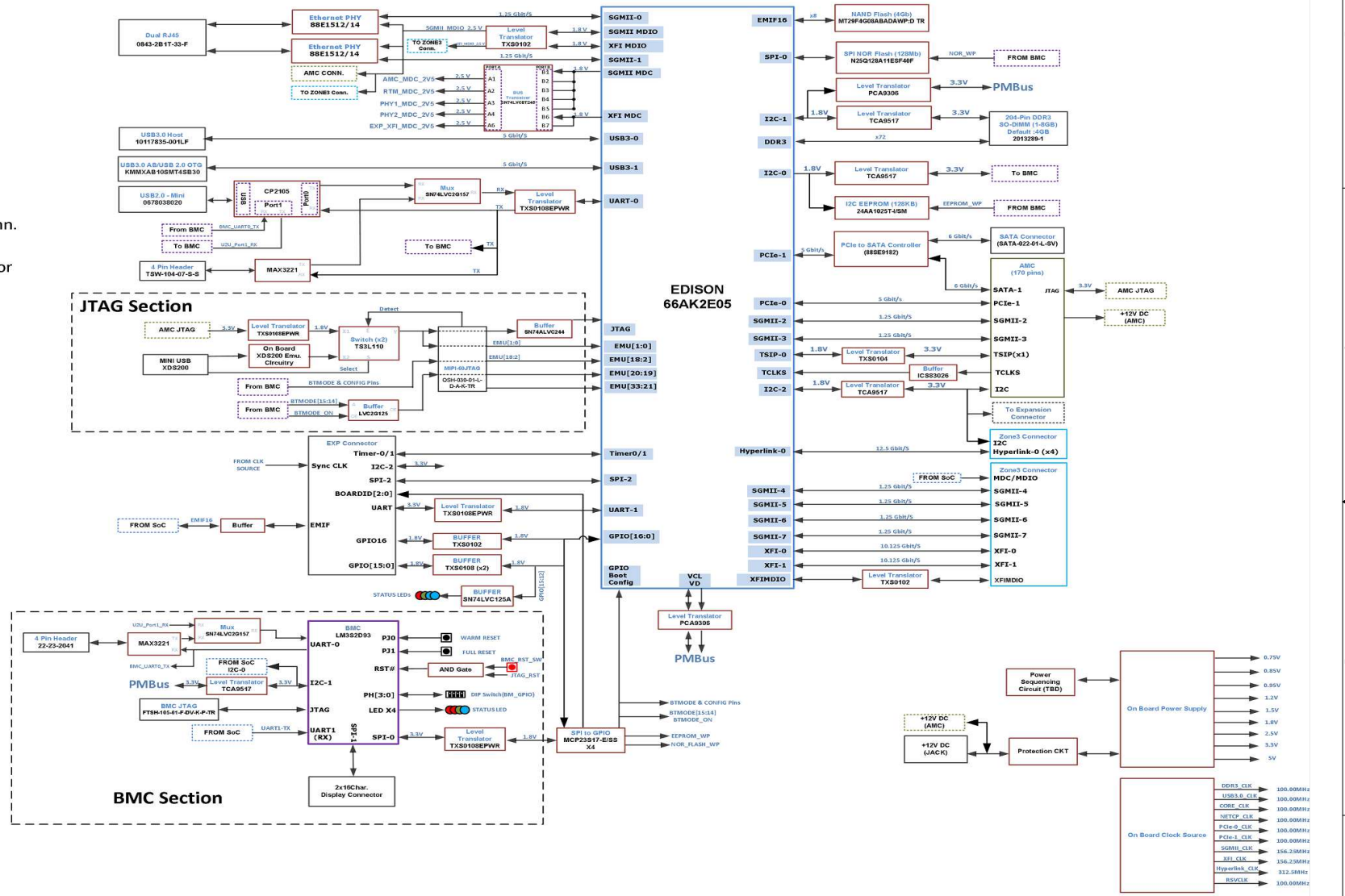
SCHEMATIC PAGE DESCRIPTION :

- 01 : COVER PAGE
- 02 : TABLE OF CONTENTS
- 03 : SYSTEM BLOCK DIAGRAM
- 04 : PLACEMENT
- 05 : POWER CONSUMPTION
- 06 : POWER SEQUENCE
- 07 : POWER DISTRIBUTION
- 08 : CLOCK DIAGRAM
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- 12 : SOC SGMII PCIE_MCM
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- 14 : SOC DDR3
- 15 : EMU & JTAG
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- 18 : MISC
- 19 : SOC CLOCK & Smart-Reflex
- 20 : SOC POWERA
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- 22 : SOC GND
- 23 : CLOCK SOURCE--1
- 24 : CLOCK SOURCE--2
- 25 : DDR3 SODIMM AND BMC LCD
- 26 : SGMII Ethernet PHY
- 27 : BMC LM3S2D93
- 28 : BMC MISC
- 29 : mTCA ZD3/120-pin Exp.
- 30 : POWER SUPPLY--1
- 31 : POWER SUPPLY-2
- 32 : XDS200_1
- 33 : XDS200_2
- 34 : XDS200_3
- 35 : XDS200_POWER
- 36 : XDS200_EMULATION
- 37 : REVISION HISTORY

Project K2E EVM		Designed for TI by eInfochips	
Title TABLE OF CONTENTS		  <small>The Solutions People</small>	
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K2E EVM BLOCK DIAGRAM

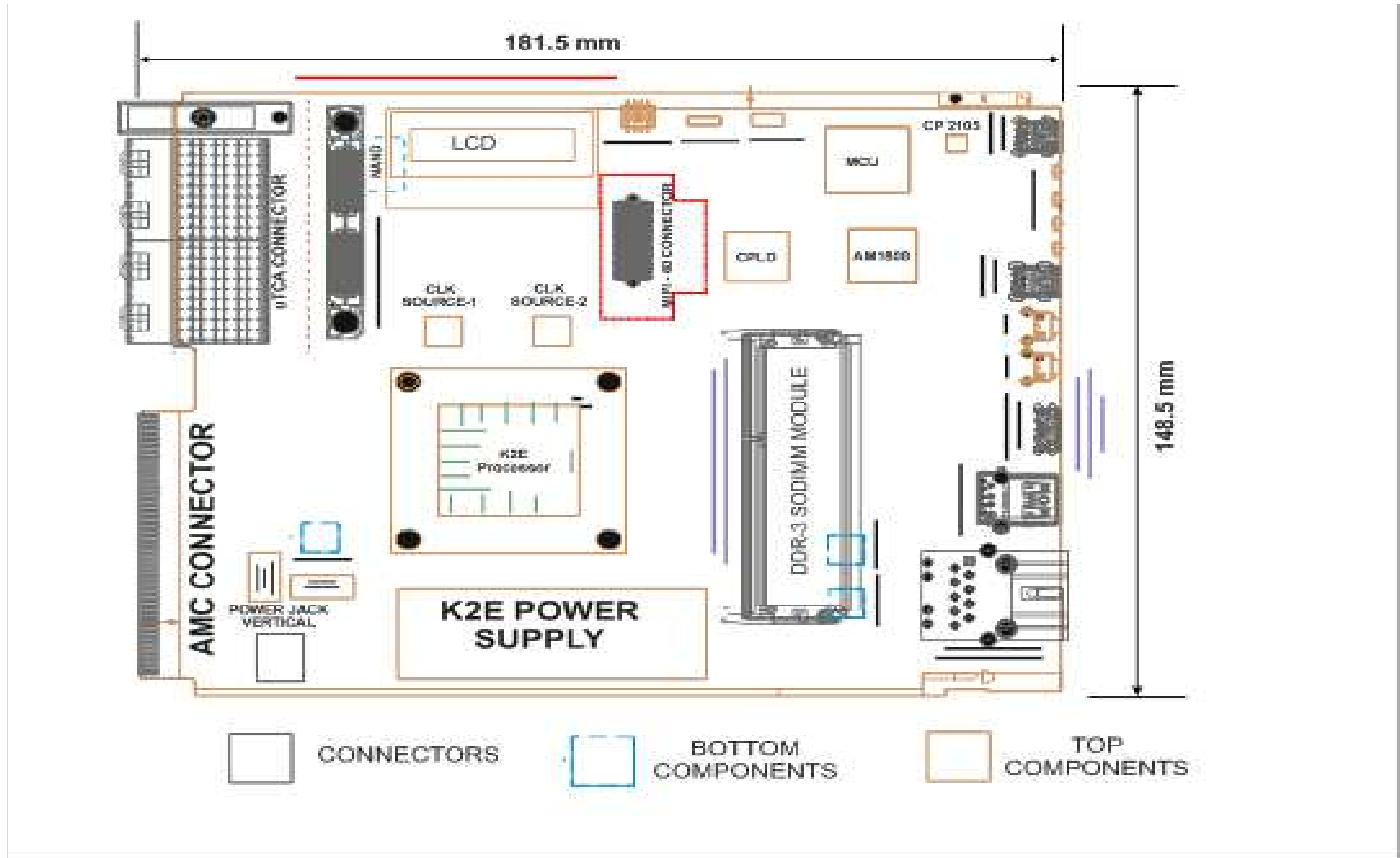
- K2E SoC
- ICs
- Connectors
- Expansion Conn.
- AMC Connector
- BMC
- Zone 3 Conn.





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DDR3_CLK	100.000MHz
USB3.0_CLK	100.000MHz
CORE_CLK	100.000MHz
NETCP_CLK	100.000MHz
PCIe-CLK	100.000MHz
PCIE3_CLK	156.250MHz
SGMII_CLK	100.000MHz
RFI_CLK	156.250MHz
Hyperlink_CLK	312.500MHz
RSWCLK	100.000MHz

PLACEMENT



Project		K2E EVM		Designed for TI by eInfochips	
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POWER CONSUMPTION

Approx Power Consumption for TI_EVM - EDISON															
Components Part No.	Description	Quantity Per Board	Current Consumed by corresponding device on power supply (mA)												Total Power (mW)
			0.75	0.85	0.95	1	1.5	1.8	2.5	3	3.3	3.3	5	12	
			VTT	AVDDS	CVDD1	CVDD	VCC1V5	VCC1V8	VCC2V5	VCC3V3_LCD	VCC3V3_ALT	VCC3V3_AUX, VDD3V3			
66AK2E05	Processor	1		800	1800	16000	800	400				50			20475
MT29F4G08ABBD4HC-D	NAND flash	1						100							180
MT18KSF51272HZ-1G4	DDR3 SODIMM Module	1	600				2088					20			3648
LCD	LCD display	1									45				135
LM3S2D93	Microcontroller	1									136				448.8
88E1512	Gigabit ethernet phy	2						8		418					1379.4
88SE9182	PCIe to SATA controller	1						663							1193.4
CP2105	USB to UART Controller	1										20			66
N25Q128A11BSF40F	SPI EEPROM	1						20							36
MCP23S17T-E/SS	Microchip	4						3				1			8.7
CDCM6208	Reference Clock generator	2										640			2112
	XDS200 circuitry	1											130		650
USB	USB 3.0	1											908		4540
SATA	SATA 3.0 HDD	1											1400		7000
	FAN	1												100	1200
	Misc	1					100	100				100	100		1160
	Total Current on individual power supply (mA)		600	800	1800	16000	2988	1286	8	45	554	831	2538	100	
	10% margin added over design (mA)		660	880	1980	17600	3286.8	1414.6	8.8	49.5	609.4	914.1	2791.8	110	
	Power Consumption in (mW)		495	748	1881	17600	4930.2	2546.28	22	148.5	2011.02	3016.53	13959	1320	

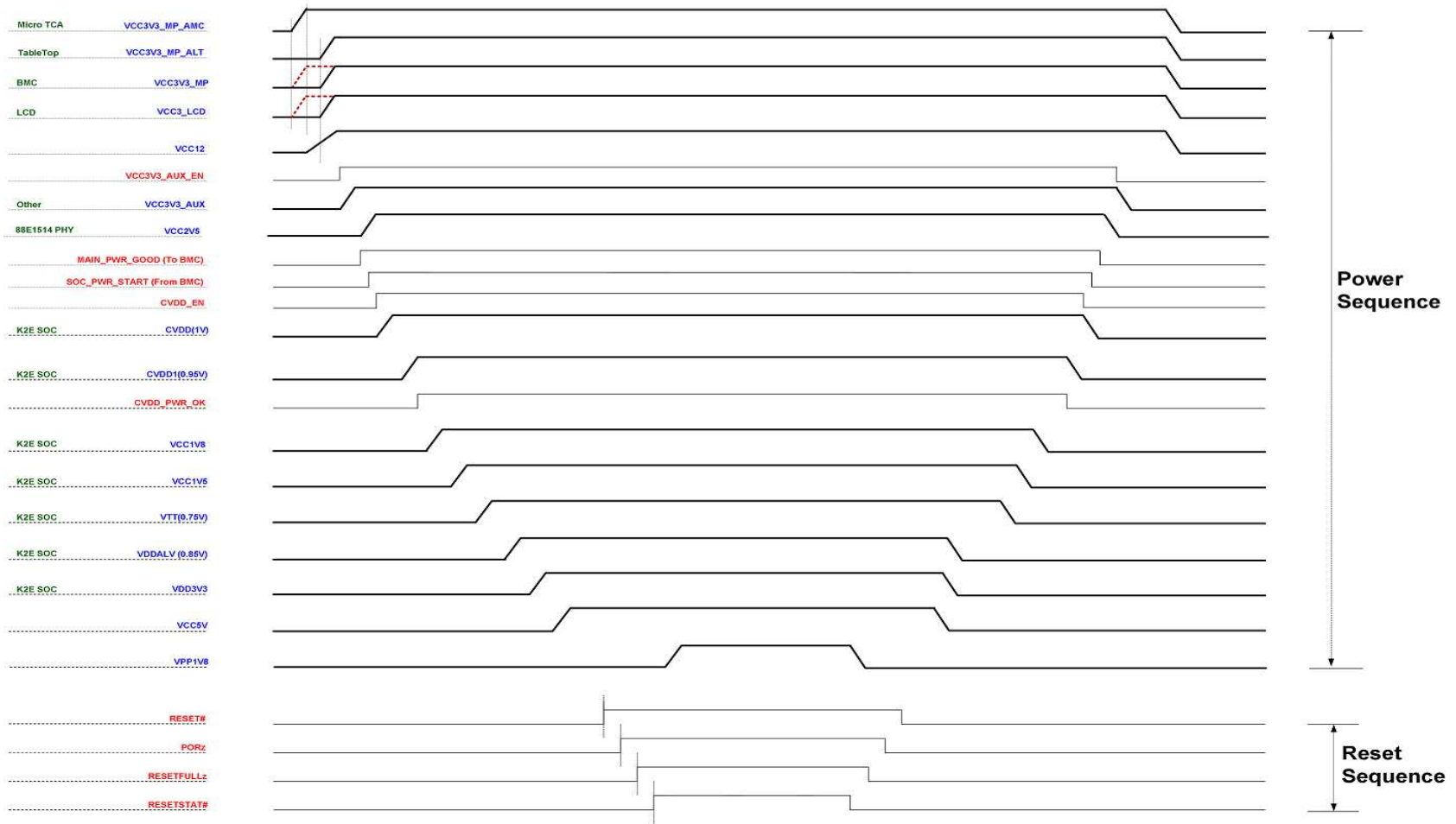
	TPS51200: 1.5V to 0.75V	660.00mA
	LM26430: 12V to 0.85V	77.92mA
	LM26430: 12V to 0.95V	195.94mA
	TPS544B24: 12V to 1.0V	1725.49mA
	TPS54620: 12V to 1.5V	573.66mA
	LM26430: 12V to 1.8V	241.13mA
	APL431: 3.3V to 3.0V	52.94mA
	TPS73701: 3.3V to 2.5V	7.84mA
	TLV1117-33CDCY: 12V to 3.3V	609.40mA
	LM26430: 12V to 3.3V	289.06mA
	TPS54620: 12V to 5.0V	1264.40mA
	Total Current @ 3.3V :	0.97A
	Total Current @ 5V :	2.79A
	Total Current @ 12V :	5.09A
	Total Power :	61.04W

Note :

1) Power consumption for 66AK2E05 is taken as TDP @ 90C & 1.4GHz* (worst case)



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Title POWER CONSUMPTION		  <small>The Solutions People</small>	
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K2E_EVM (EDISON) -- POWER SEQUENCE



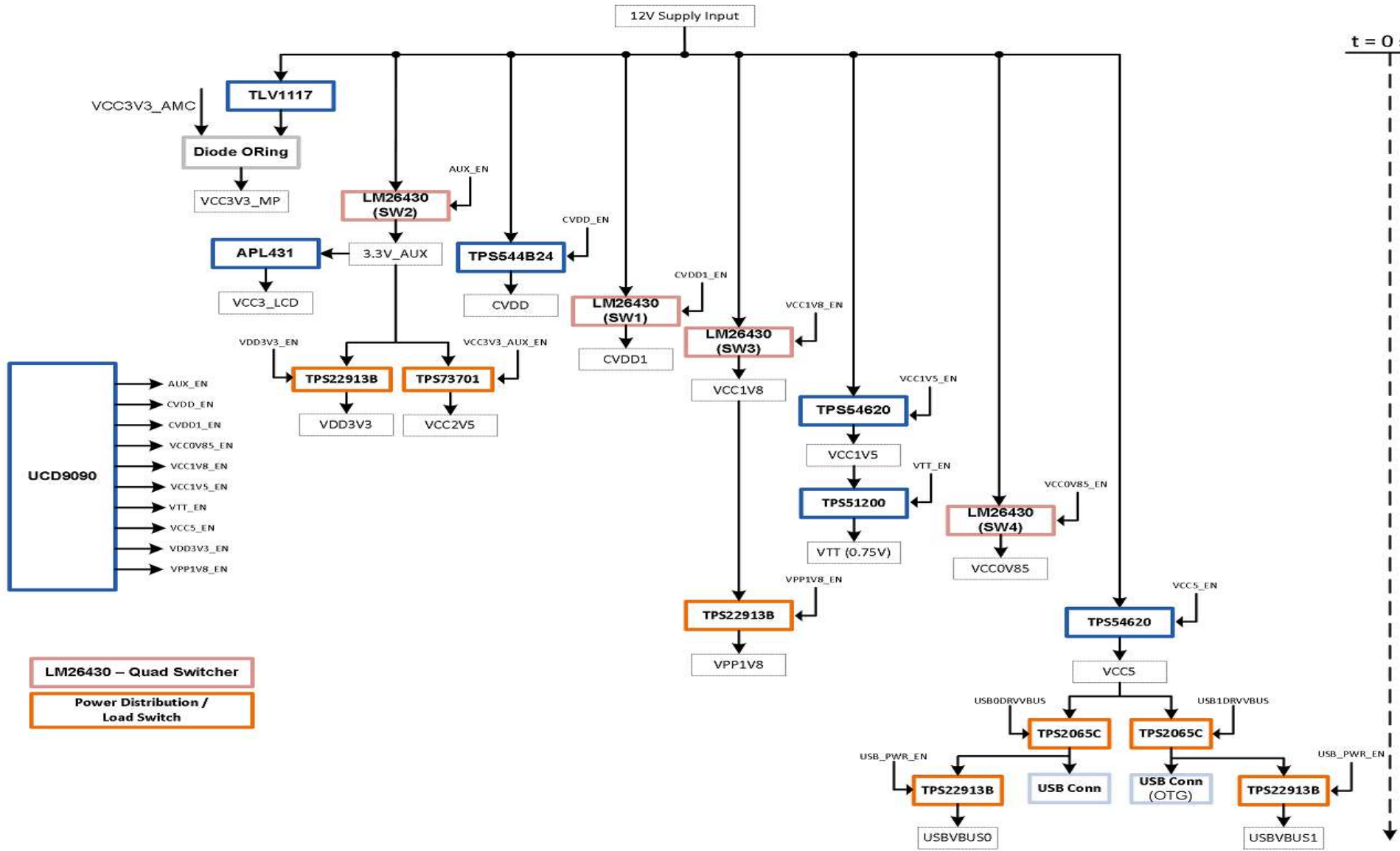
Notes:

- 1) We have referred "Table 5: Sequencing – Core before I/O" of "Keystone_IL_Power_Sequencing_Brief_r1p18_preliminary.pdf" to create above Power Sequencing
- 2) Power Sequencing was modified as per document : "FAE Alert - Power-Up Sequence Change.pdf" received from TI on 8/23

Project K2E EVM		Designed for TI by elnfochips	
Title POWER SEQUENCING		  <small>The Solutions People</small>	
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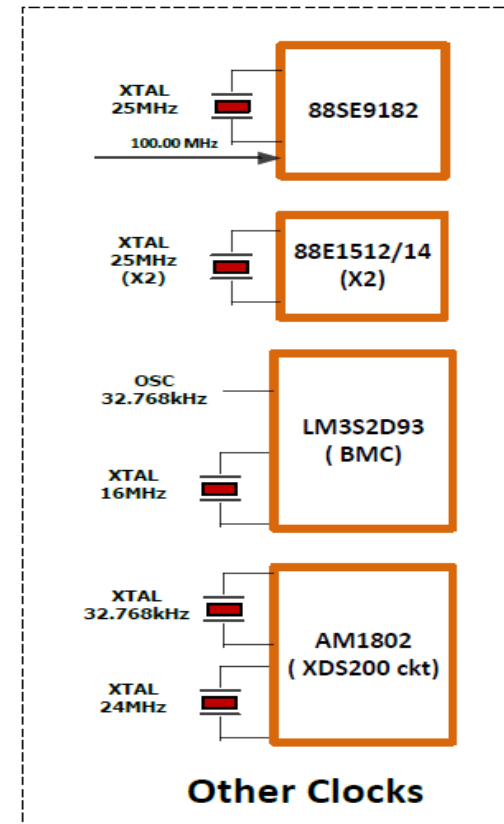
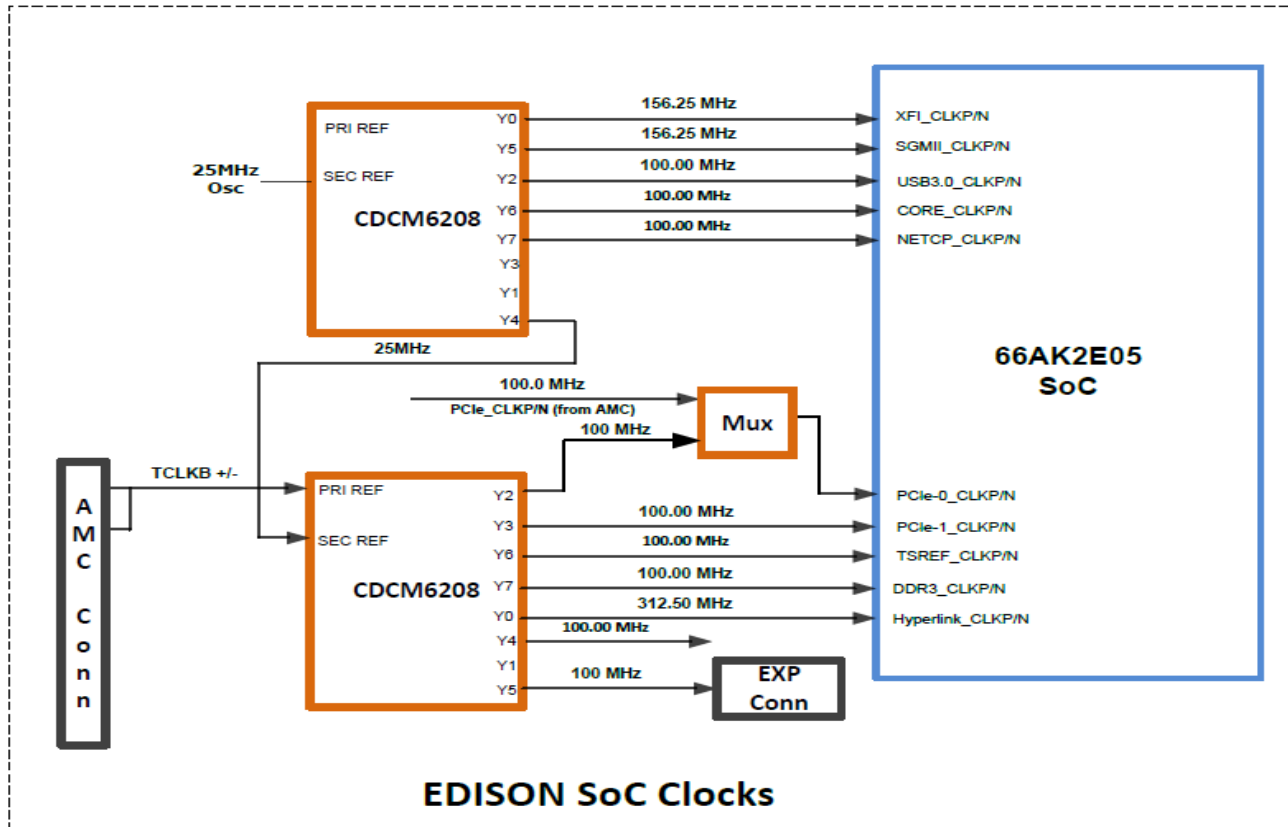
EDISON – Power Tree

t = 0 sec



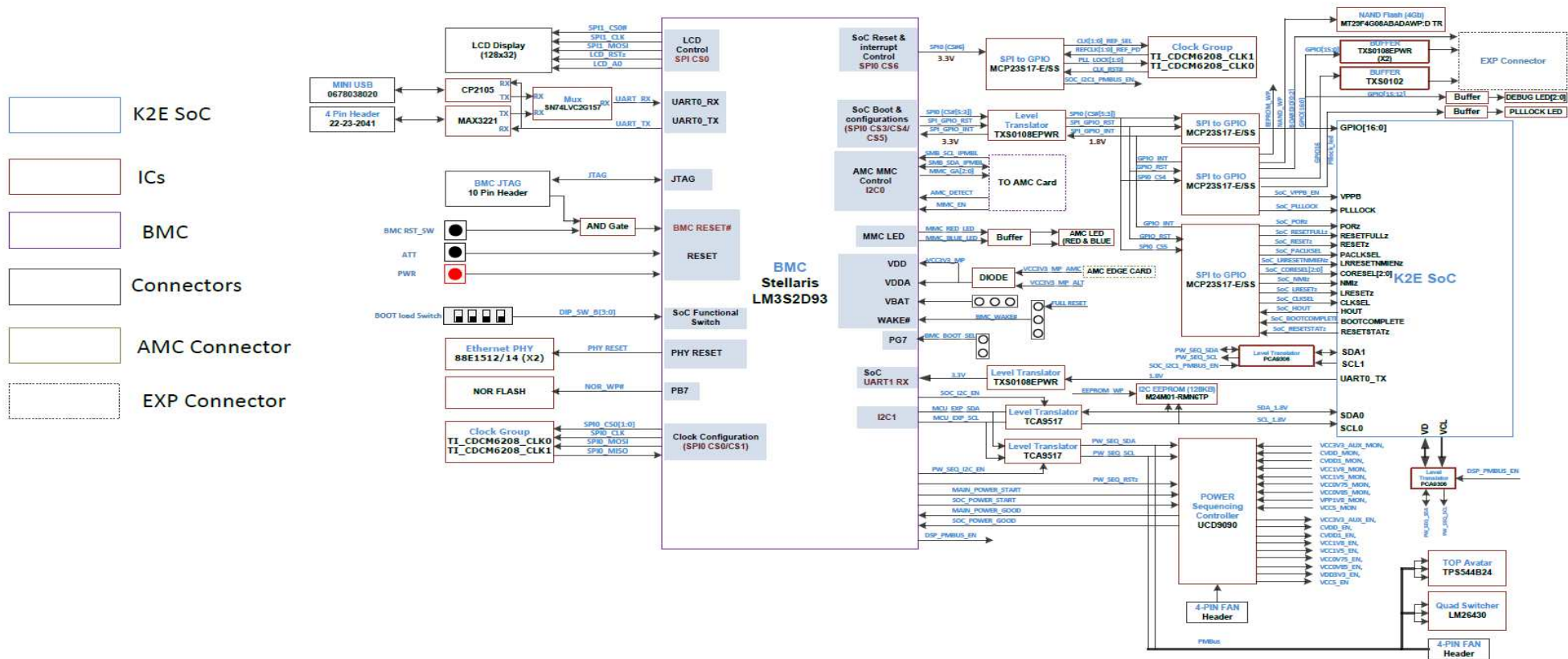
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Title		POWER DISTRIBUTION			
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EDISON CLOCK GENERATION



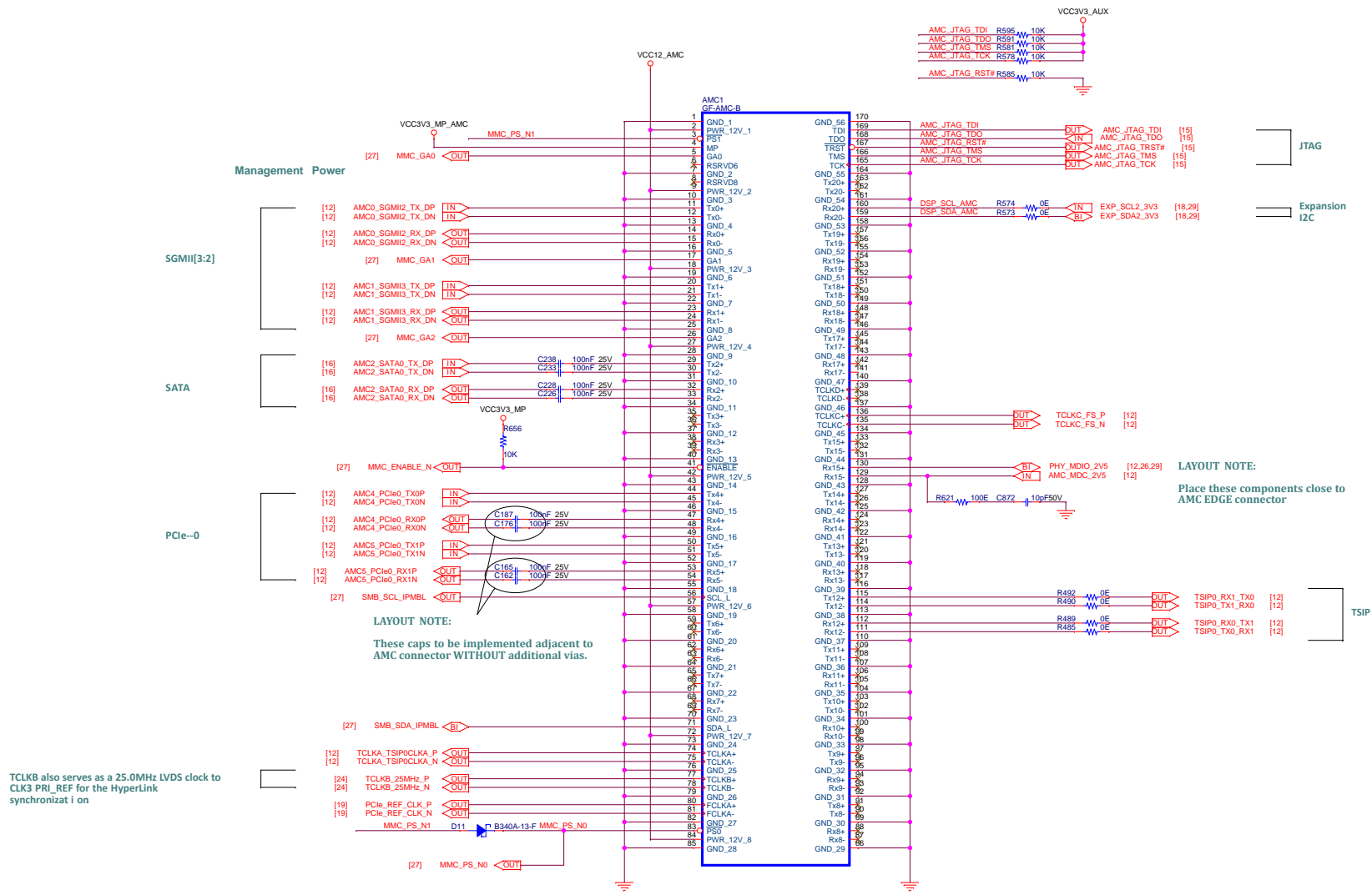
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Title CLOCK DIAGRAM			
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BMC BLOCK DIAGRAM



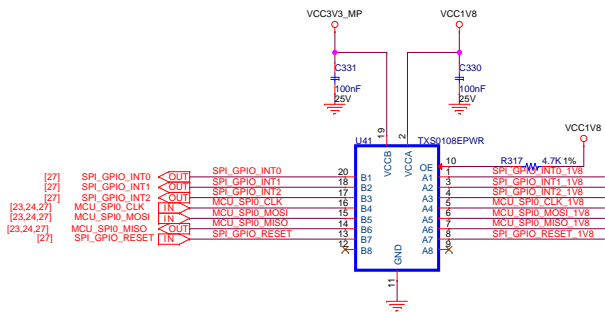
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Title		BMC BLOCK DIAGRAM			
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AMC EDGE CONNECTOR



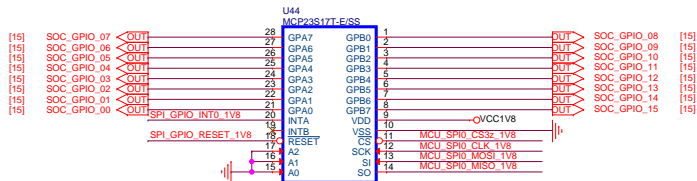
Project K2E EVM		Designed for TI by einfochips	
Title AMC INTERFACE			
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SPI LEVEL SHIFT 3V3 to 1V8



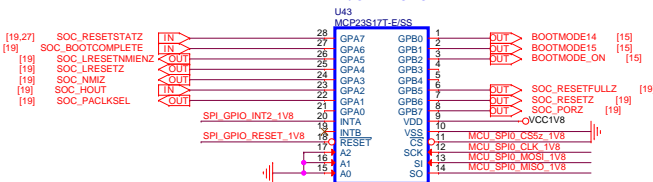
SPI TO GPIO

1.8V Level

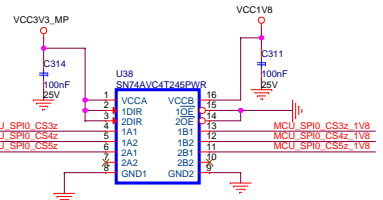
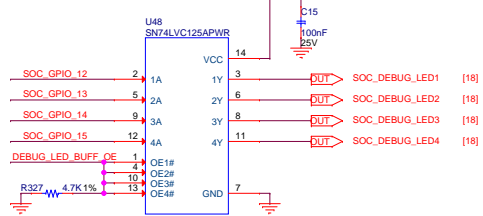
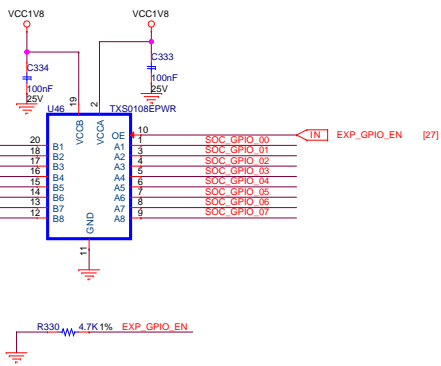
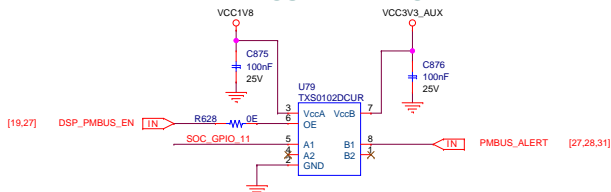


SPI TO GPIO

1.8V Level

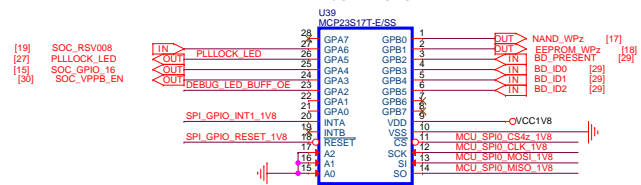


PMBUS ALERT BUFFER



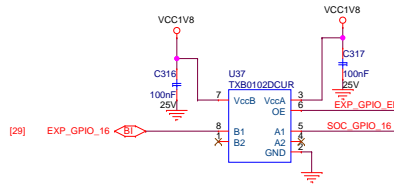
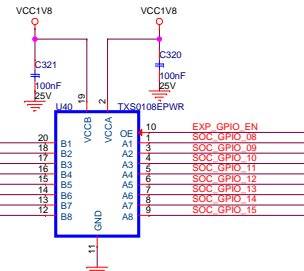
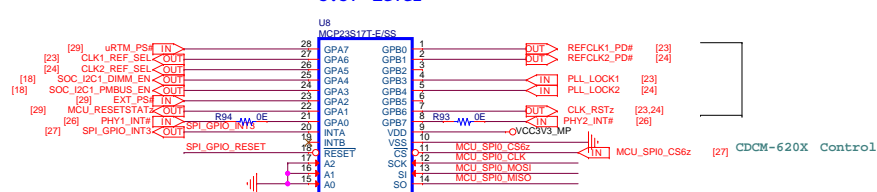
SPI TO GPIO

1.8V Level



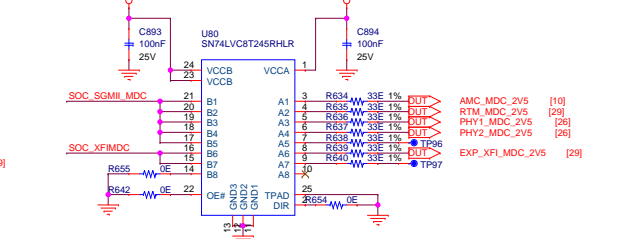
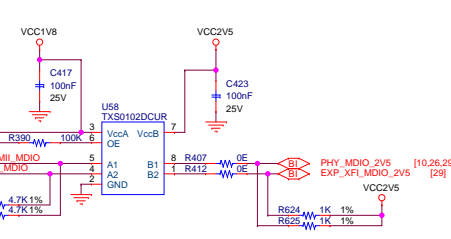
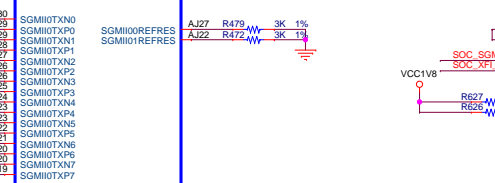
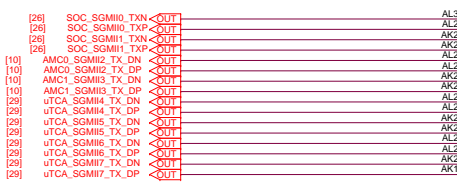
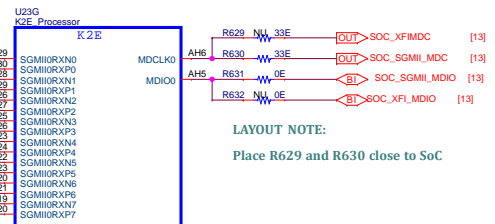
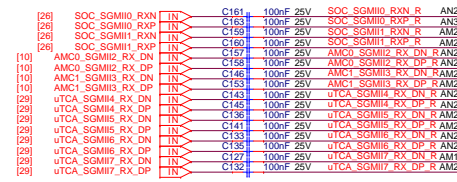
SPI TO GPIO

3.3V Level



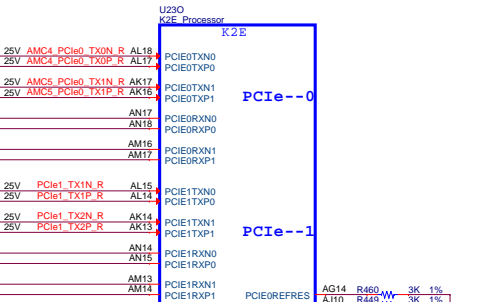
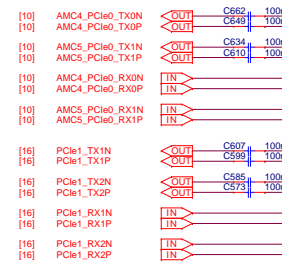
Project		K2E EVM		Designed for TI by elfin chips	
Title		SPI to GPIO Converter			
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SGMII X8

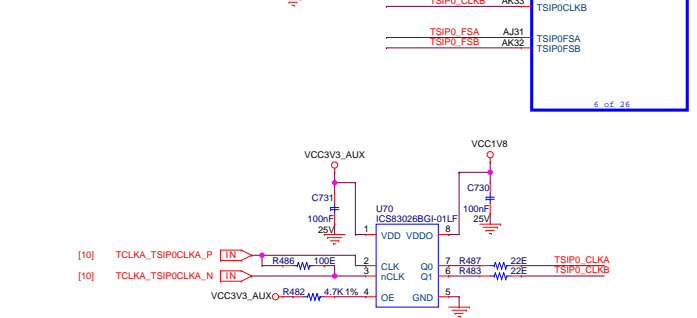
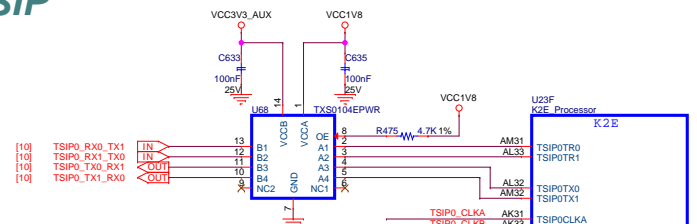


PCIE[1:0] X2

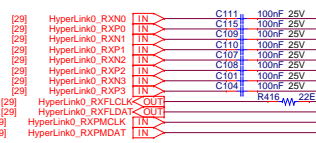
LAYOUT NOTE:
Place ALL PCIe DC-blocking caps close to the TX pins



TSIP

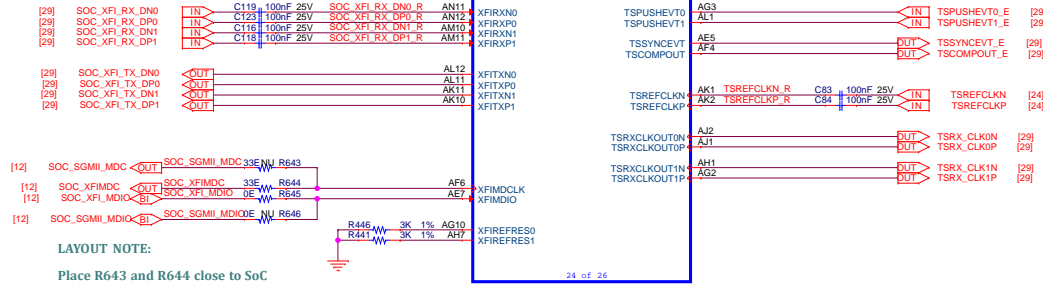


HyperLink X4

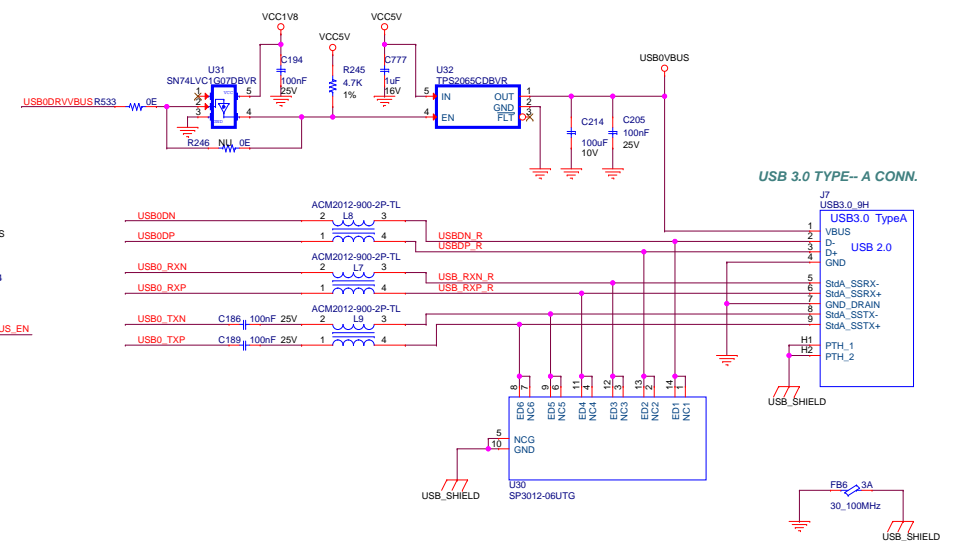
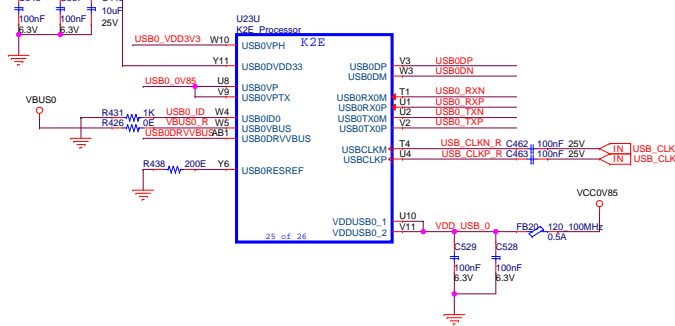


Project	K2E EVM		Designed for TI by infochips	
Title	SERDES INTERFACE			
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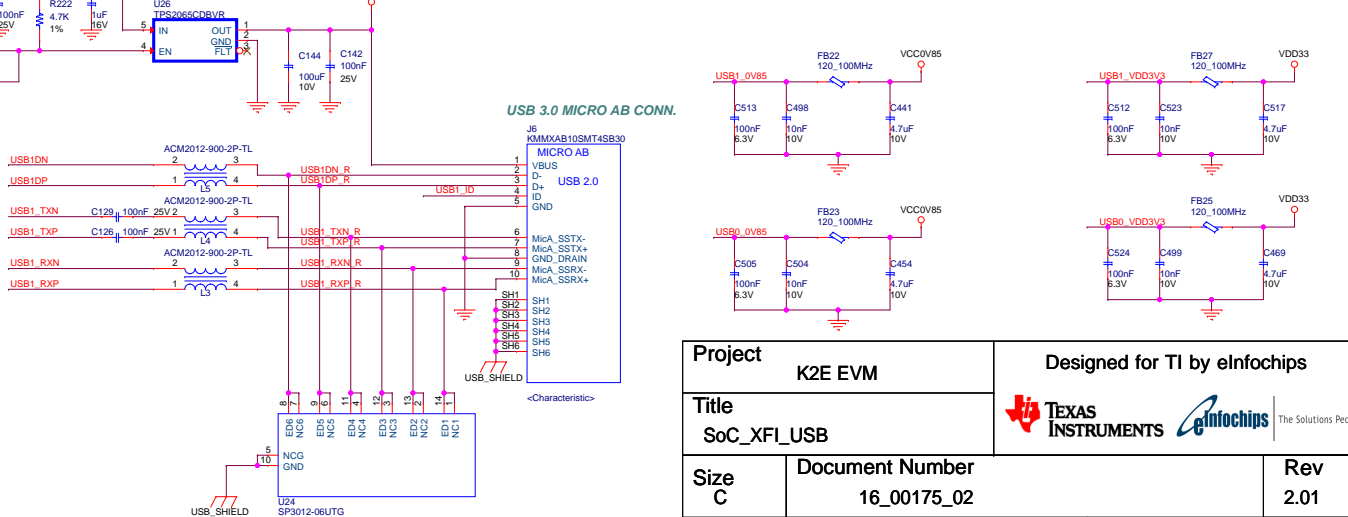
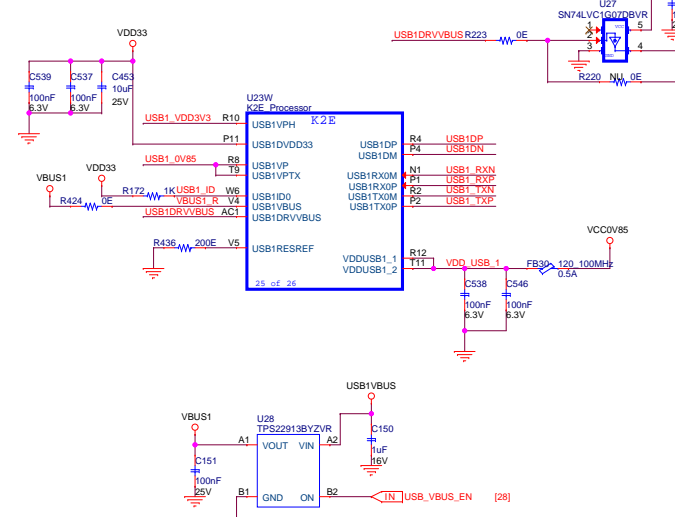
XFI X2



USB -- 0 (HOST)

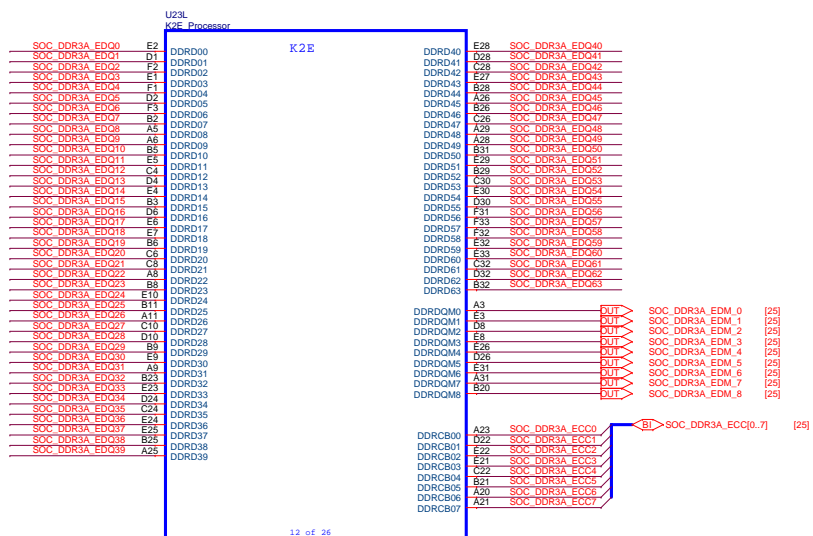
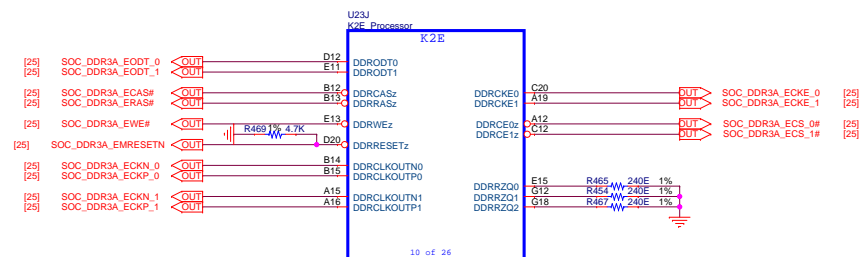
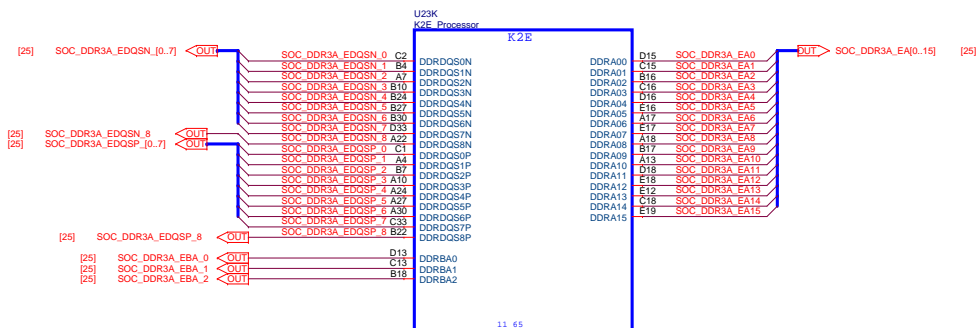


USB -- 1 (HOST or Device)



Project K2E EVM		Designed for TI by elnfochips	
Title SoC_XFI_USB			
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SOC DDR3



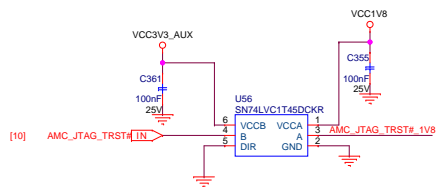
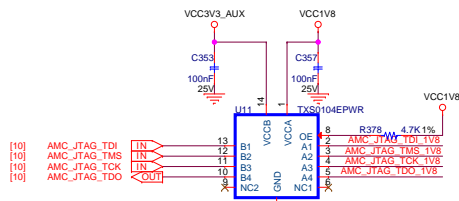
SOC_DDR3A_EDQ0_63 [25]

Project K2E EVM		Designed for TI by elfinichips	
Title SoC DDR3			
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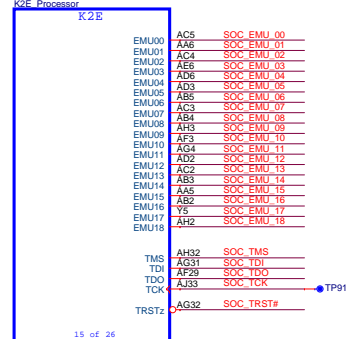
SOC GPIO



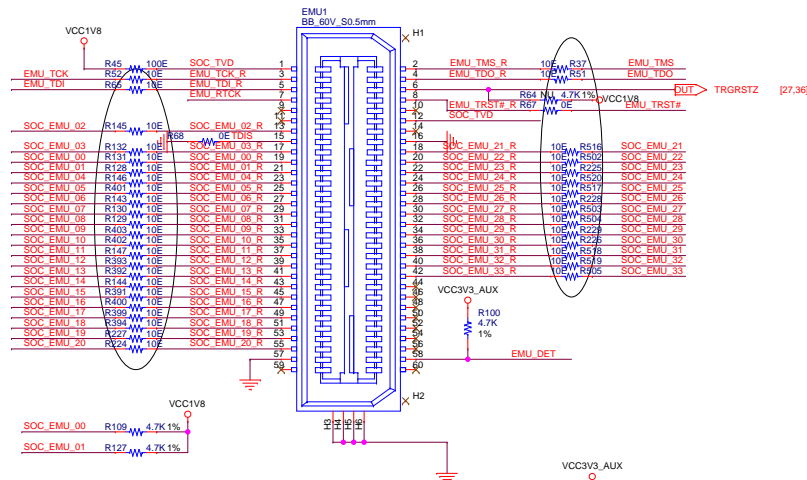
AMC JTAG 3V3 to 1V8 CONVERTER



SOC EMU

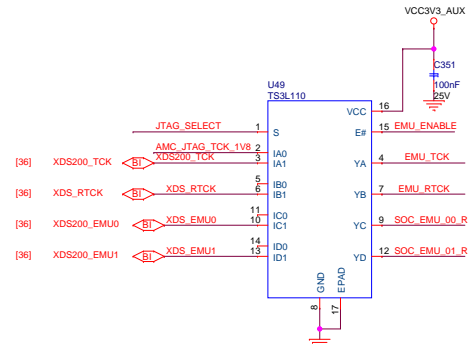
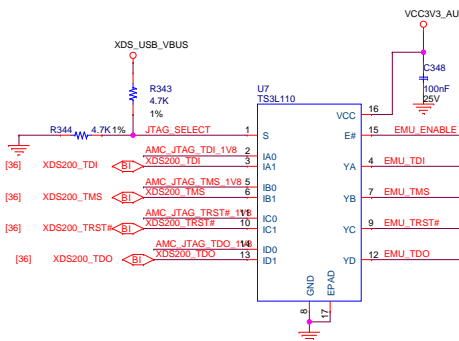
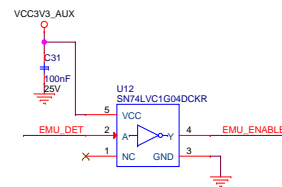


MIPI 60



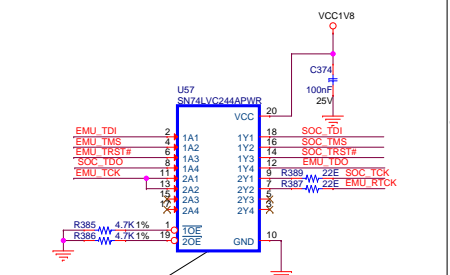
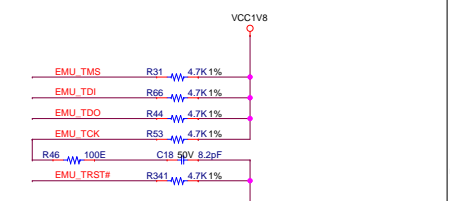
LAYOUT NOTE:

- Place termination resistors for EMU_TCK, TDI, TMS as close to MIPI-60 header as possible
- Place termination resistors for SOC_TDO and SOC_EMU* signals as close to the SoC as possible



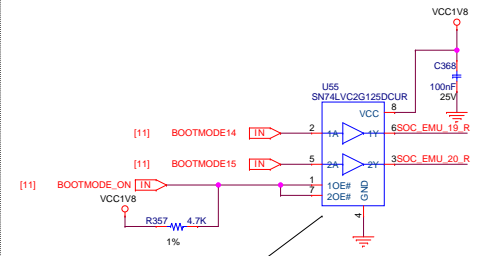
LAYOUT NOTE:

- Place U49 as close to MIPI-60 header as possible to minimize stubs on SOC_EMU_00_R and SOC_EMU_01_R



LAYOUT NOTE:

- Termination resistors for SOC_TCK and EMU_RTCK should be placed as close to U57 as possible

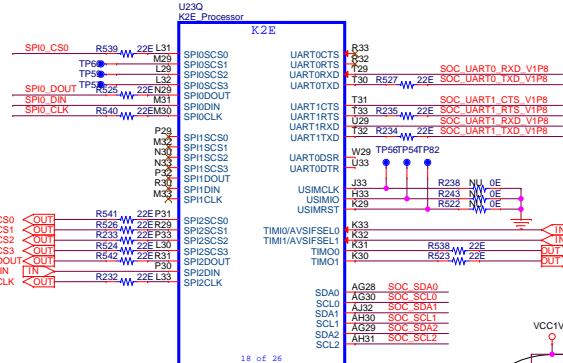


LAYOUT NOTE:

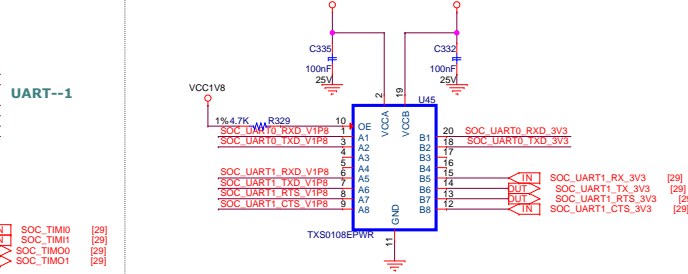
- Place U55 as close to MIPI-60 header as possible to minimize stubs on SOC_EMU_19_R and SOC_EMU_20_R

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Title EMU & JTAG			
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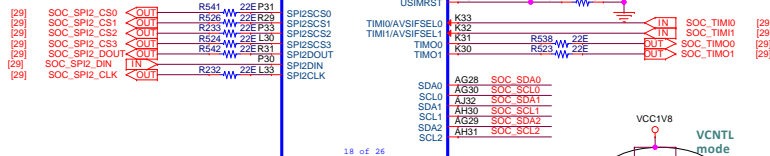
SPI--0



UART--1

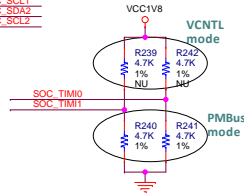


SPI--2

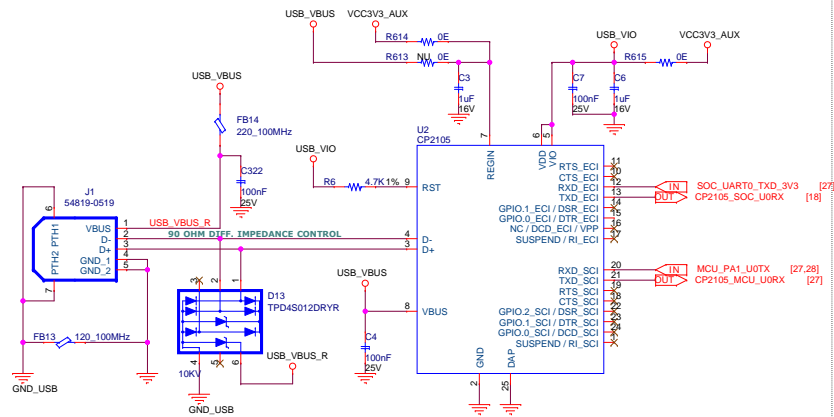


NOTE:

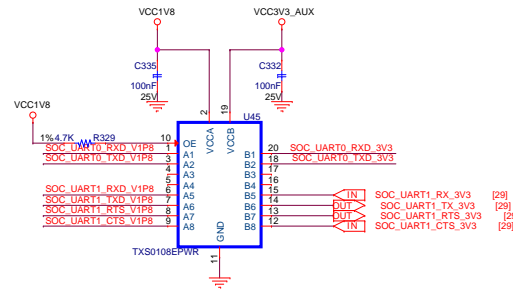
- VCNTL mode (Default): Pull-down are installed and Pull-ups are NU
- PMBus Mode: Install Pull-ups and depopulate Pull-downs



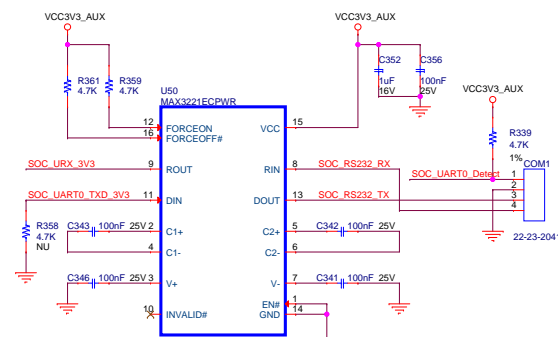
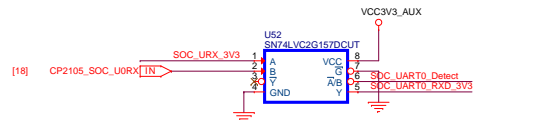
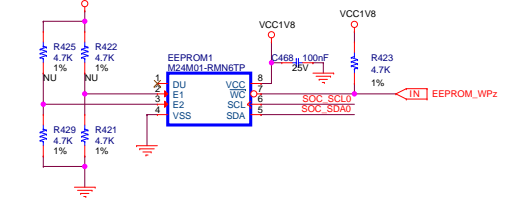
SoC UART0 TO USB



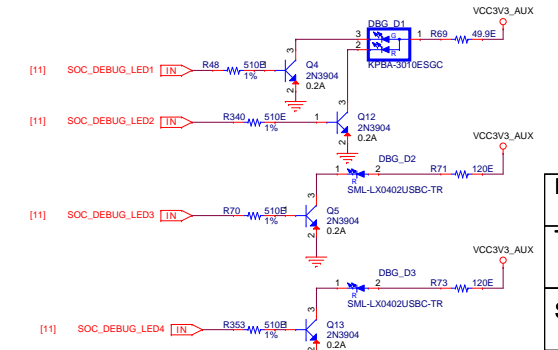
UART 1V8 to 3V3 CONVERTER



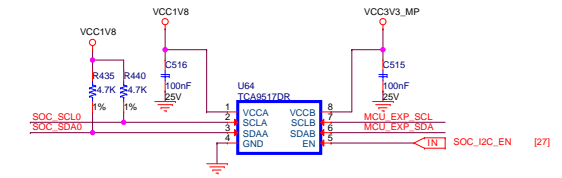
I2C EEPROM



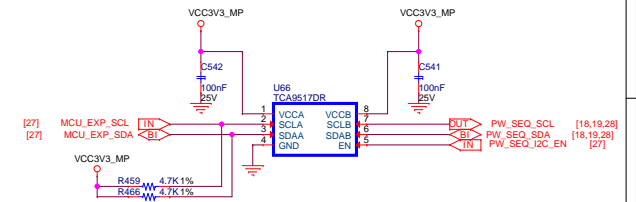
DEBUG LEDs



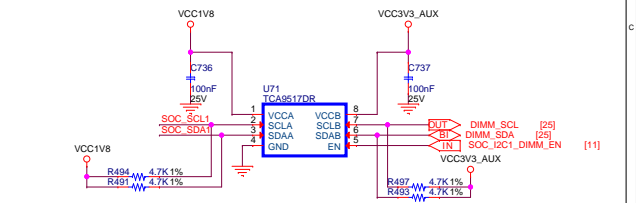
I2C--0 1V8 to 3V3 CONVERTER



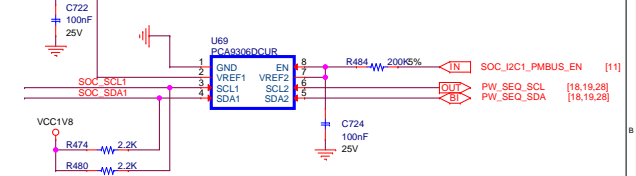
3V3 I2C ISOLATOR



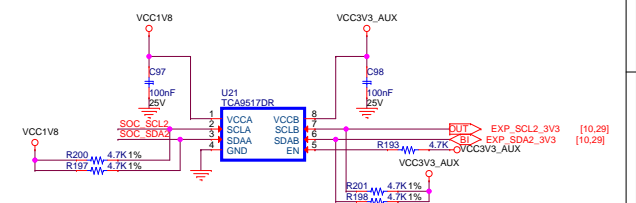
I2C--1 1V8 to 3V3 CONVERTER



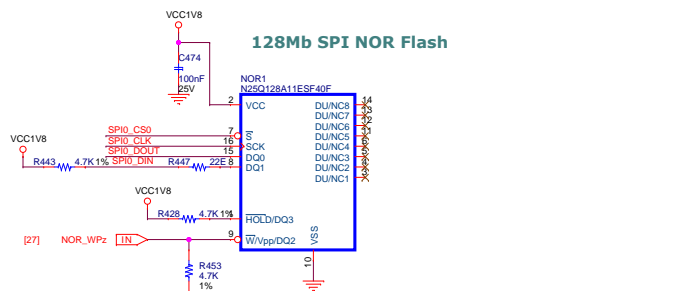
I2C--1 PMBus Connection



I2C--2 1V8 to 3V3 CONVERTER



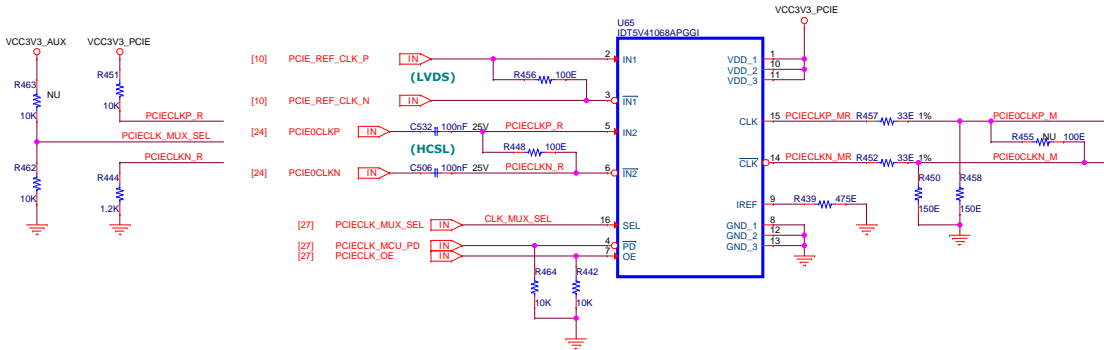
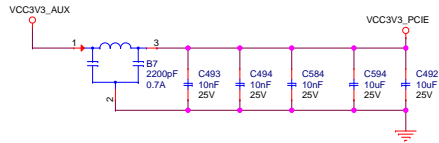
128Mb SPI NOR Flash



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Title		MISC			
Size	Document Number	16_00175_02		Rev	2.01
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PCI CLOCK MUX

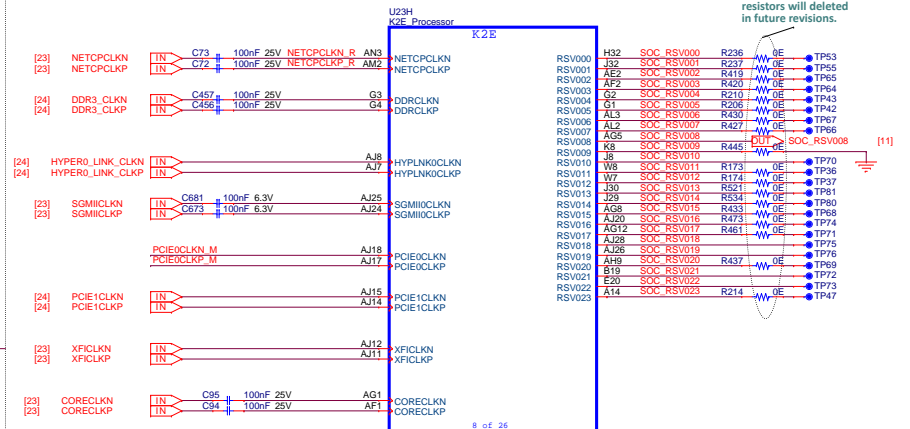
SEL	I/P PAIR SEL
LOW	IN2/IN2#
HIGH	IN1/IN1#



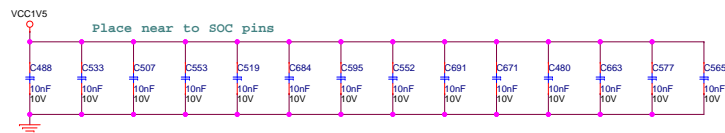
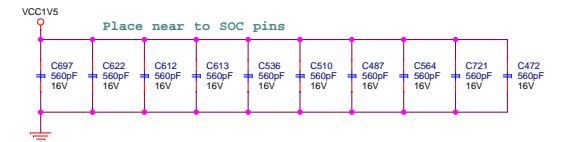
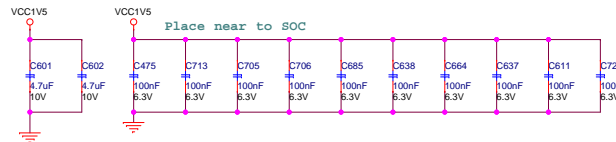
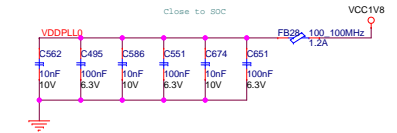
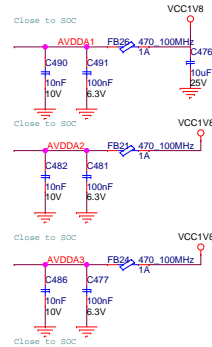
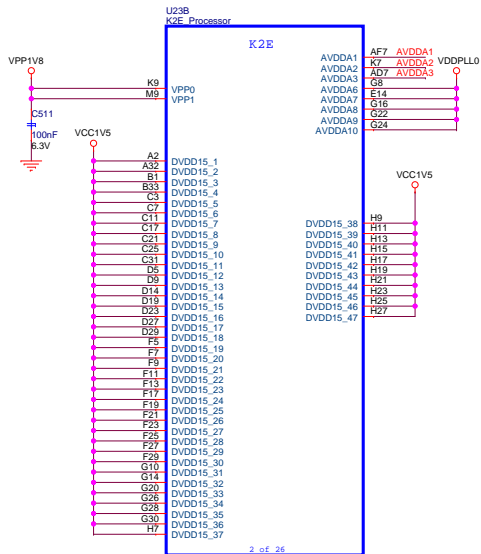
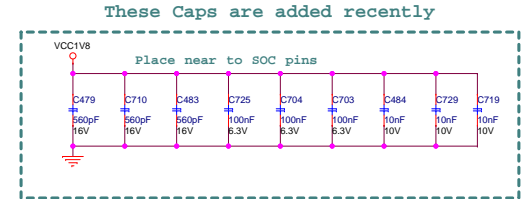
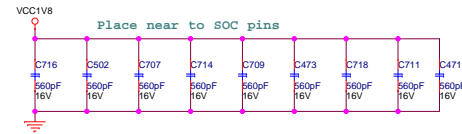
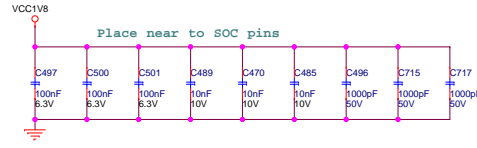
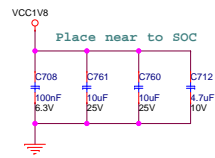
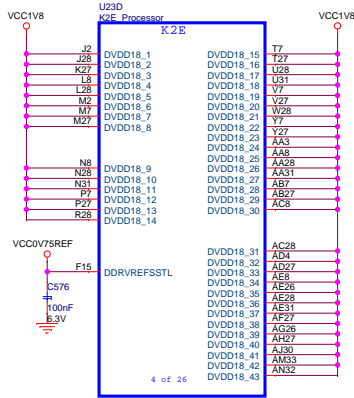
SOC REFERENCE CLOCK

All blocking capacitors should be placed near SOC to keep connecting routes short and minimize parasitics

NOTE: These series resistors will be deleted in future revisions.



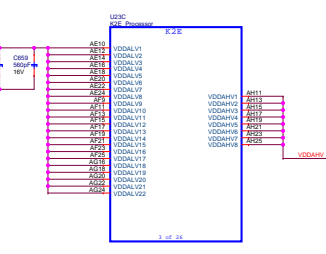
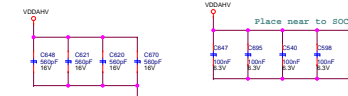
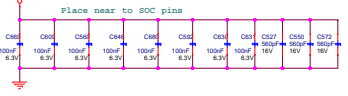
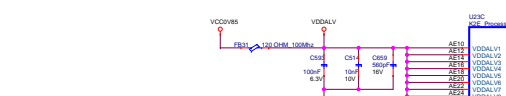
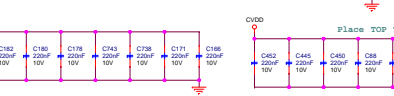
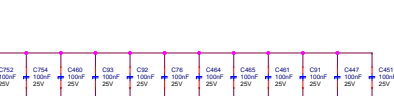
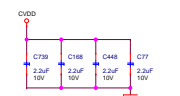
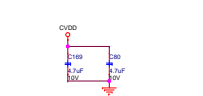
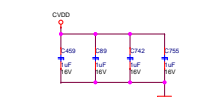
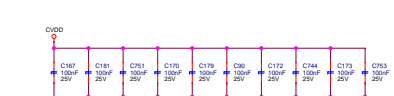
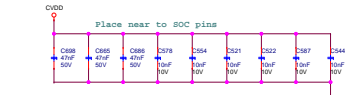
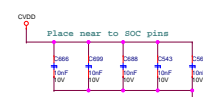
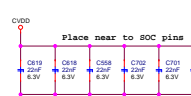
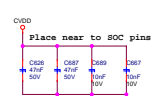
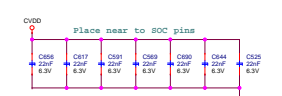
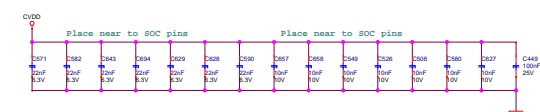
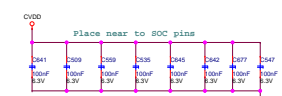
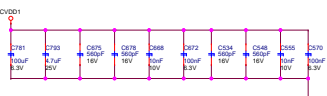
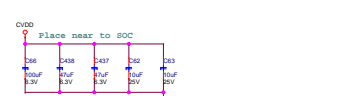
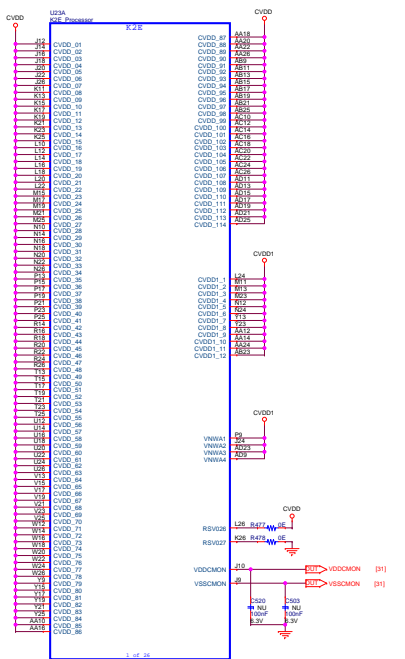
SOC POWER



Project K2E EVM		Designed for TI by einfochips	
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0.85V - 1.05V (CVDD) (Smart Reflex)

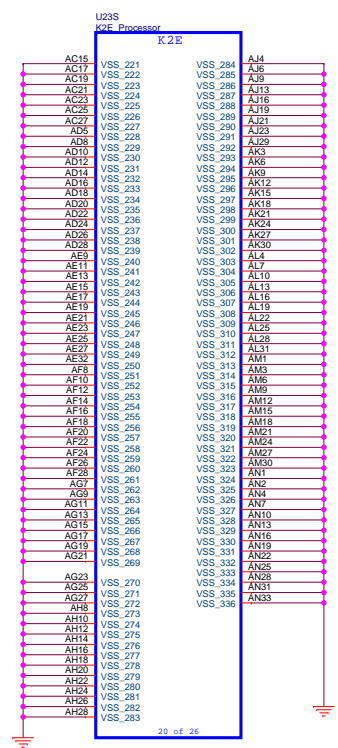
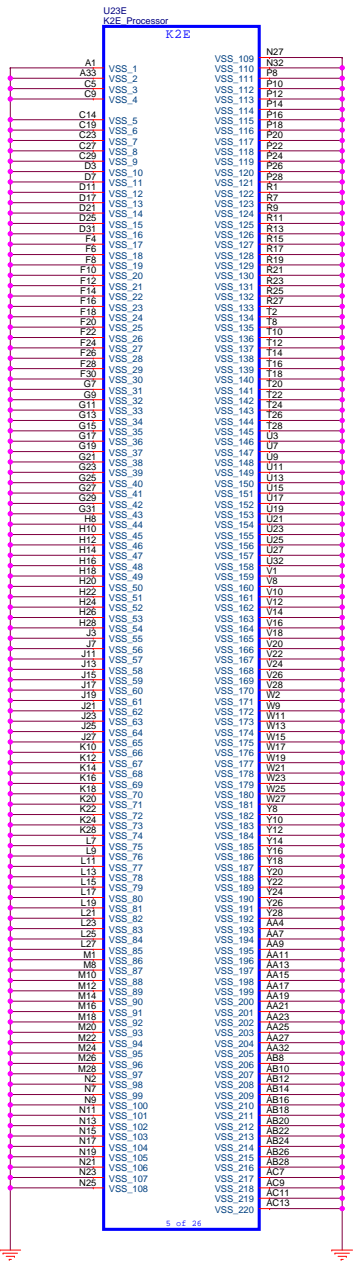
SOC POWER



THESE CAPS ARE ADDED FOR PROVISION ONLY. VALUES CAN BE CHANGED BASED ON PI ANALYSIS RESULT

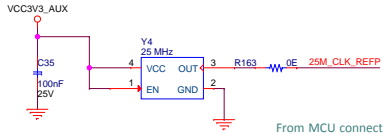
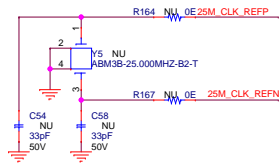
Project		K2E EVM		Designed for TI by efnchips	
Title		SoC_POWERB			
Size D		Document Number		Rev	
		16_00175_02		2.01	
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SOC GROUND

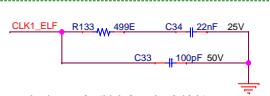
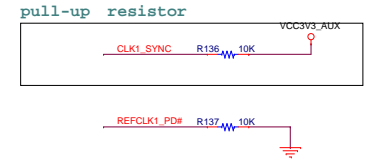
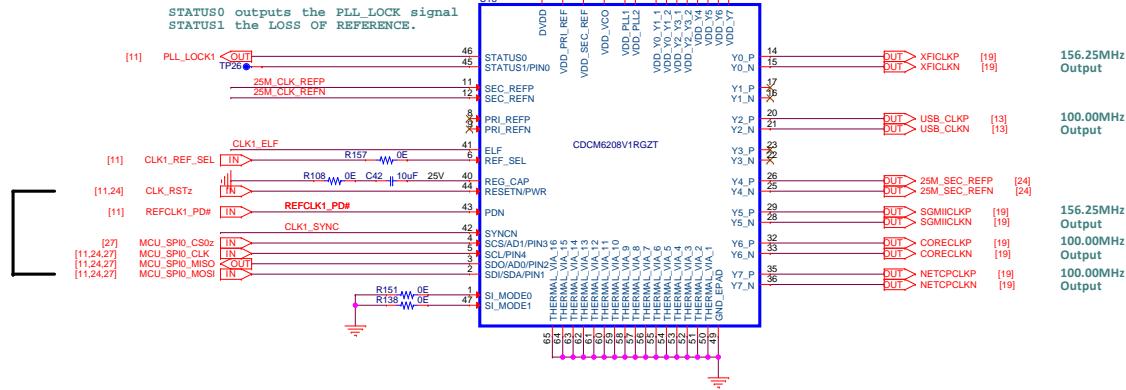


Project K2E EVM		Designed for TI by einfochips	
Title SoC Ground			
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CLOCK SOURCE-- 1



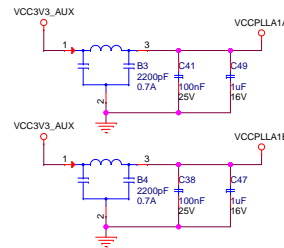
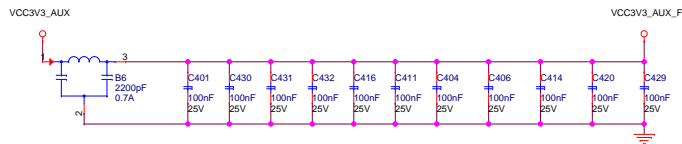
From MCU connect to this signal



Synthesizer mode (high loop bandwidth)
CDCE6208T1:
With C1=100pF, R2=50Ω, C2=22nF and
internal components R3=10Ω, C3=342.5pF,
FPPD=25MHz, and ICP=2.5mA,
loop bandwidth = (337kHz)

Serial Interface Mode or Pin Mode Selection

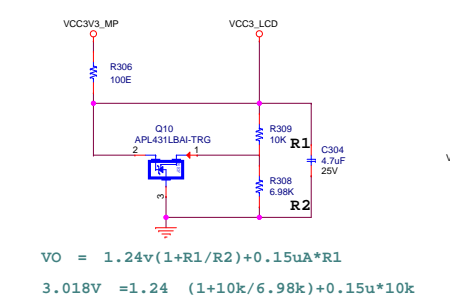
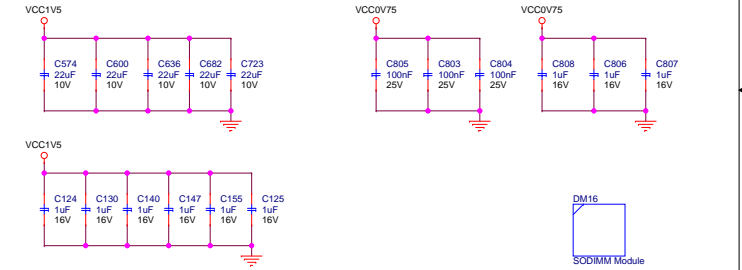
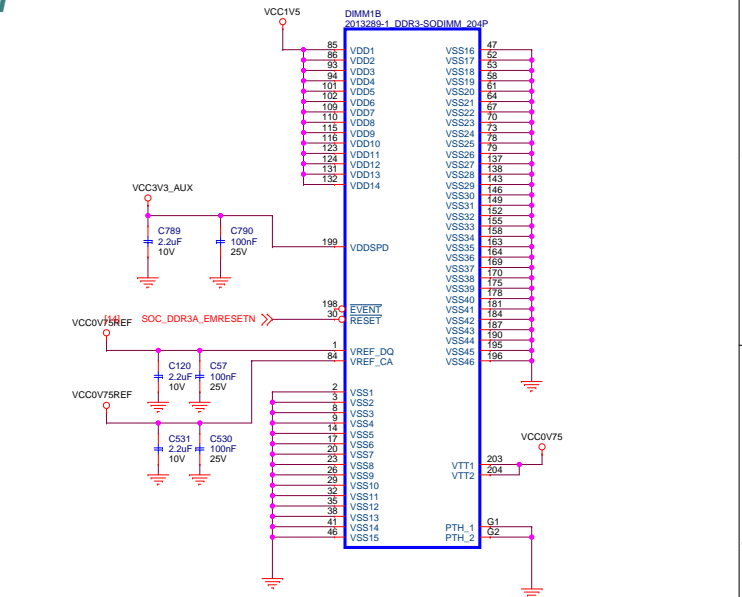
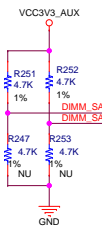
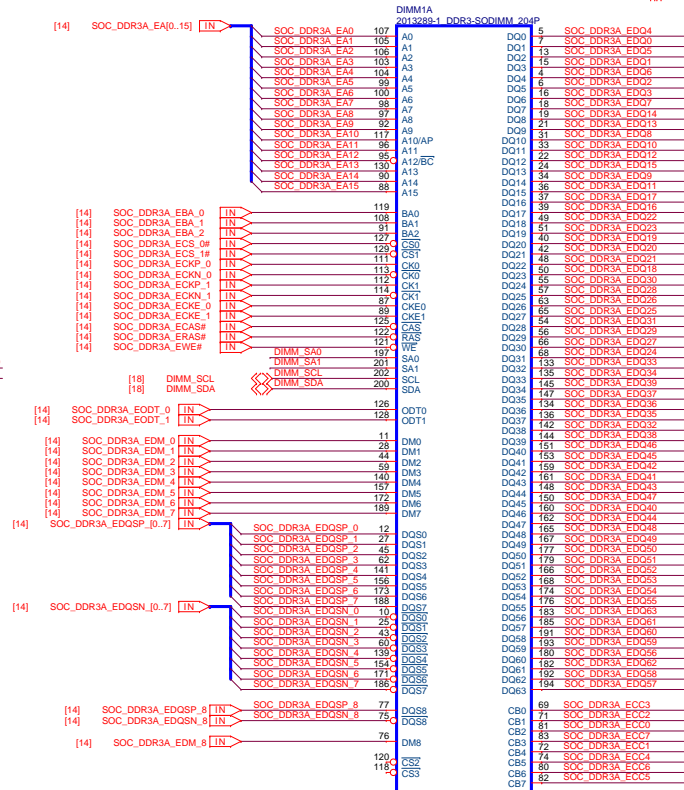
MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEVED



Project K2E EVM		Designed for TI by einfochips	
Title CLOCK SOURCE-- 1			
Size C	Document Number 16_00175_02	Rev 2.01	
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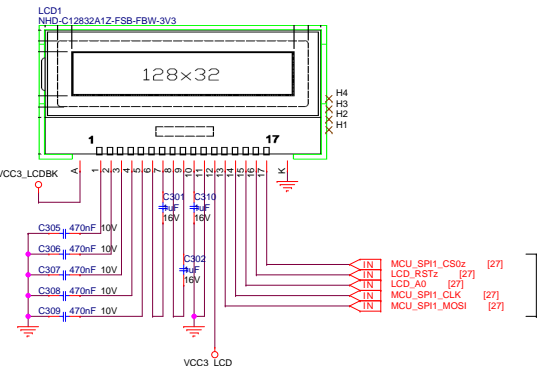
DDR3 SODIMM

<> SOC_DDR3A_EDQ[0..63] [14]
<> SOC_DDR3A_ECC[0..7] [14]

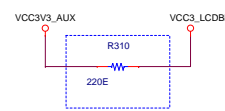


$$VO = 1.24v(1+R1/R2)+0.15uA*R1$$

$$3.018V = 1.24 (1+10k/6.98k)+0.15u*10k$$

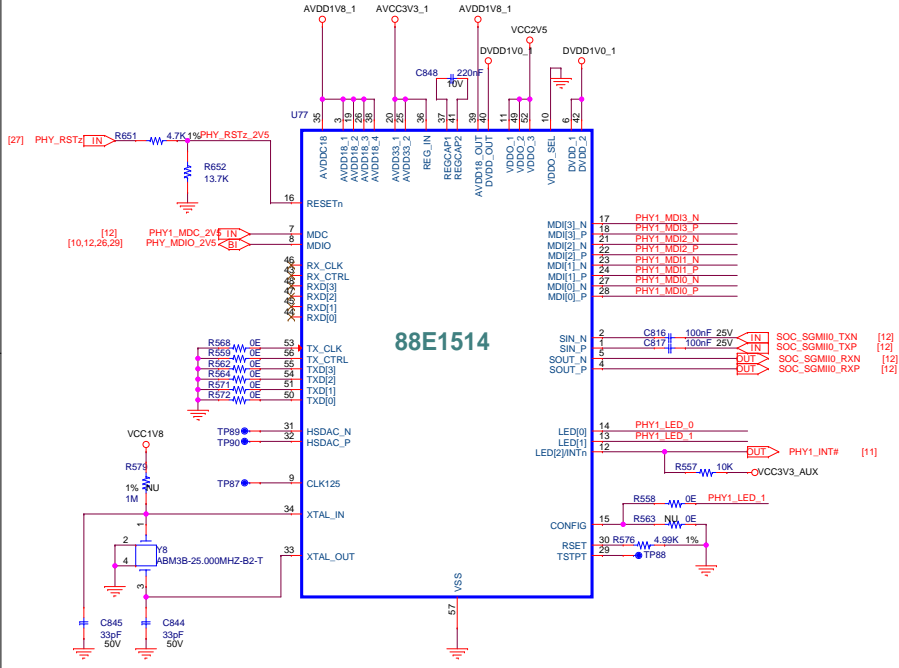


SPI1 CS0
LCD control



Project K2E EVM		Designed for TI by elnfochips	
Title DDR3- SODIMM AND LCD			
Size C	Document Number 16_00175_02	Rev 2.01	
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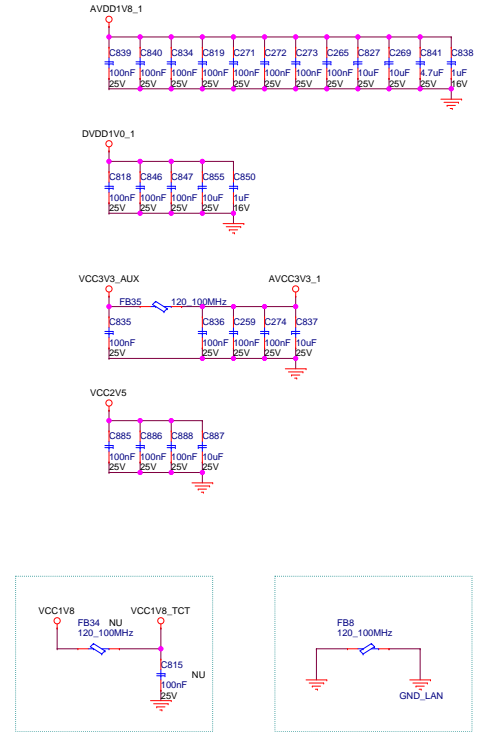
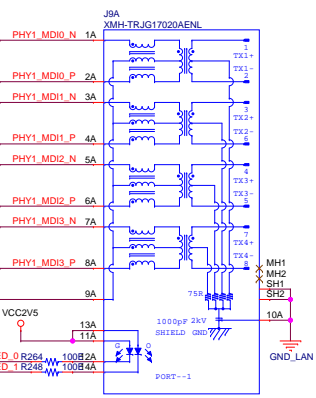
ETHERNET PHY 1



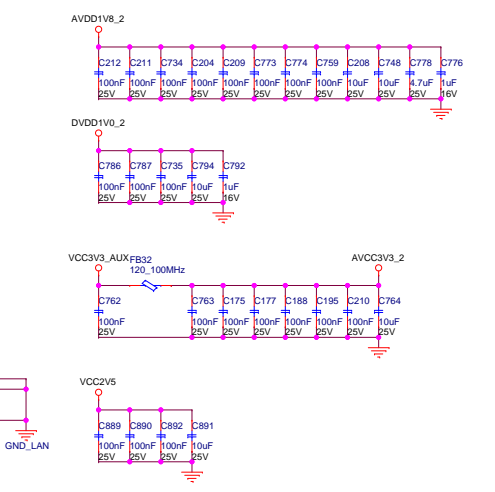
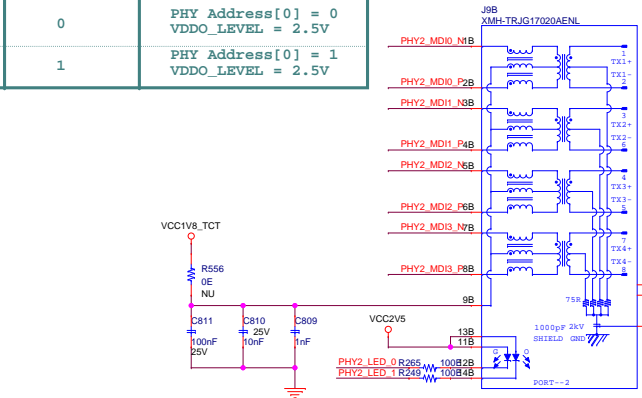
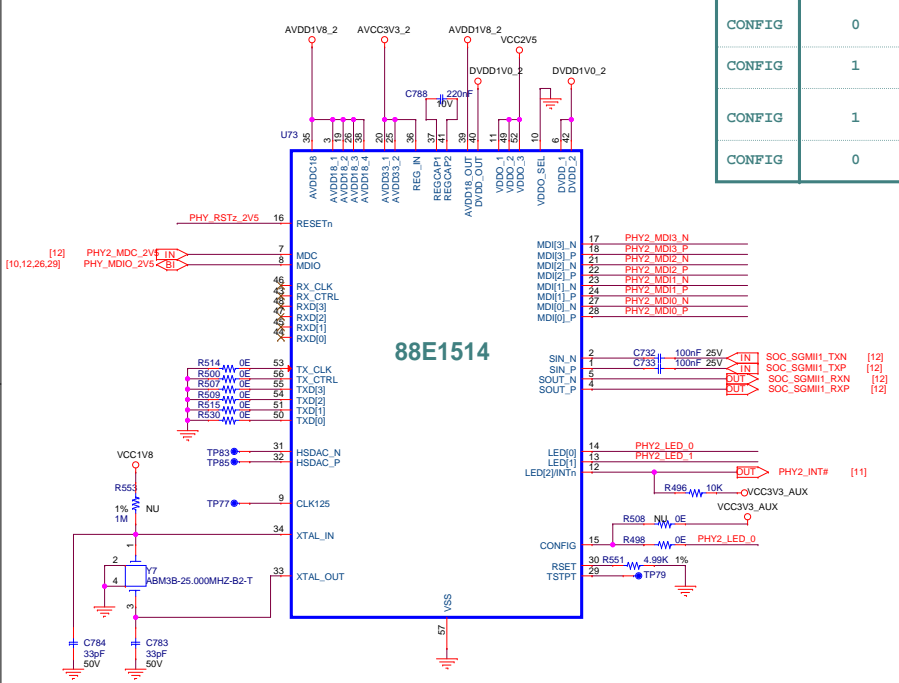
CONFIGURATION MAPPING

PIN	BIT 1,0
VSS	00
LED[0]	01
LED[1]	10
LED[2]	Unused
VDDO	11

PIN	CONFIG Bit1	CONFIG Bit0	Value Assignment
CONFIG	0	0	PHY Address[0] = 0 VDDO_LEVEL = 3.3V
CONFIG	1	1	PHY Address[0] = 1 VDDO_LEVEL = 3.3V
CONFIG	1	0	PHY Address[0] = 0 VDDO_LEVEL = 2.5V
CONFIG	0	1	PHY Address[0] = 1 VDDO_LEVEL = 2.5V



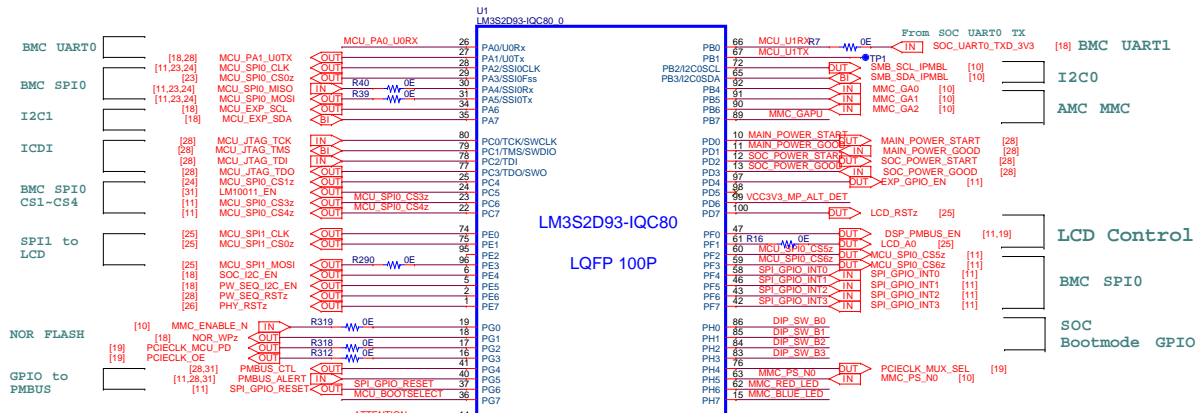
ETHERNET PHY 2



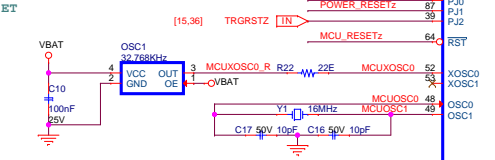
PHY ADDRESS :- 0X1

Project K2E EVM		Designed for TI by infochips	
Title SGMII ETHERNET PHY			
Size C	Document Number 16_00175_02	Rev 2.01	
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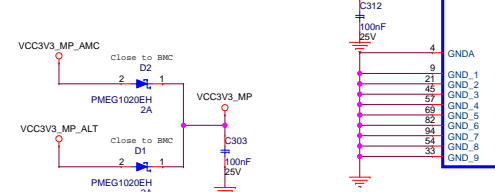
BMC INTERFACE



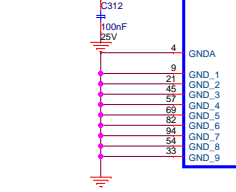
LM3S2D93-IQC80
LQFP 100P



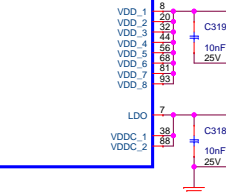
Power for BMC



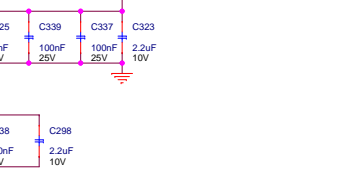
Attention



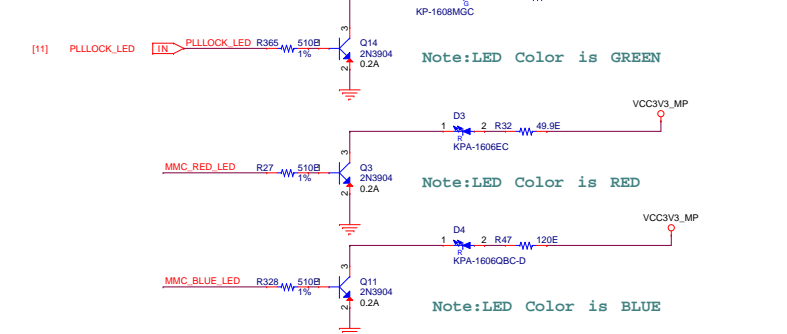
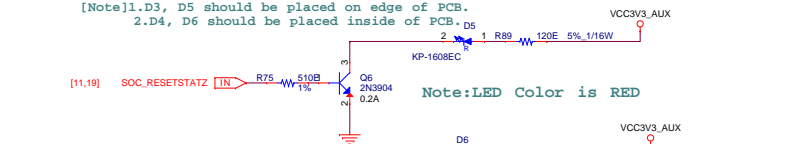
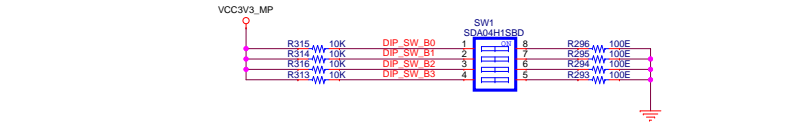
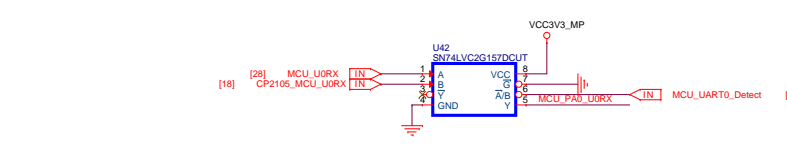
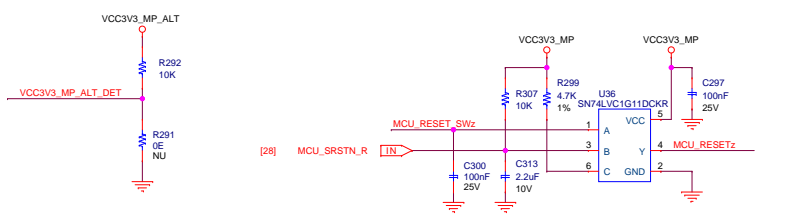
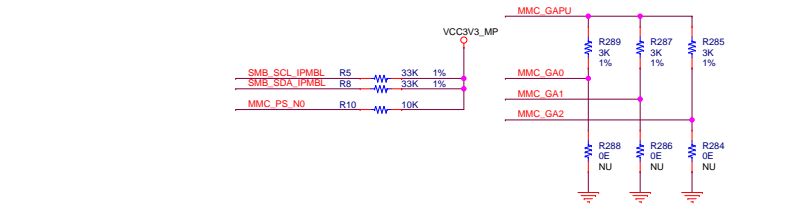
Power RESET



WAKE

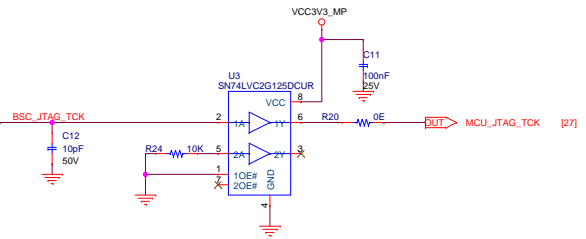
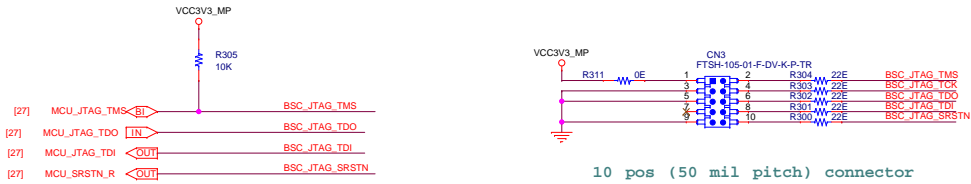


BMC_RESET

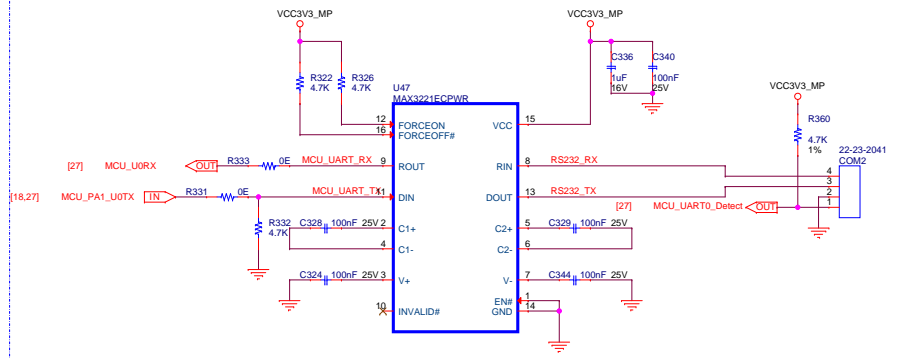


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Title BMC			
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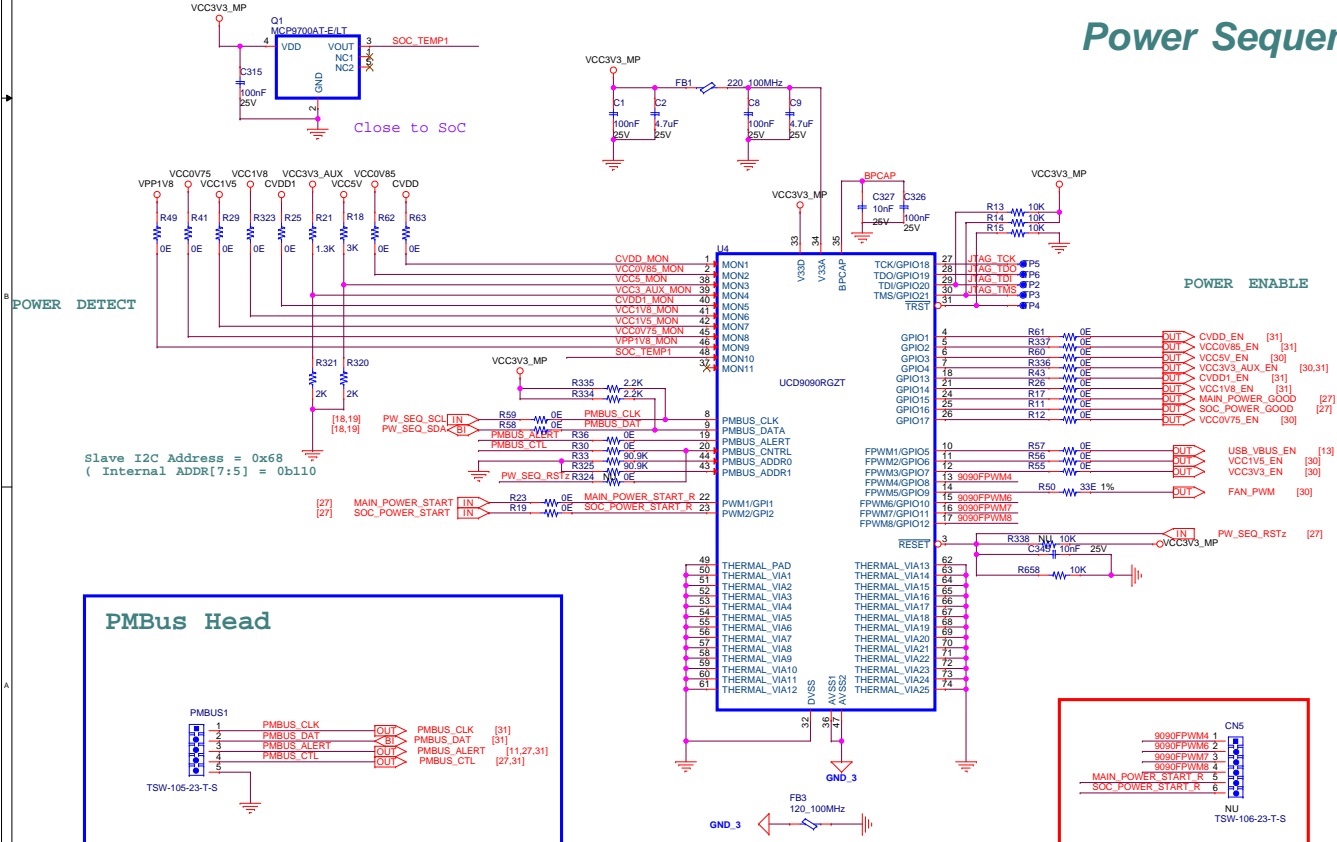
BMC JTAG



BMC UART



Power Sequencing (UCD9090)



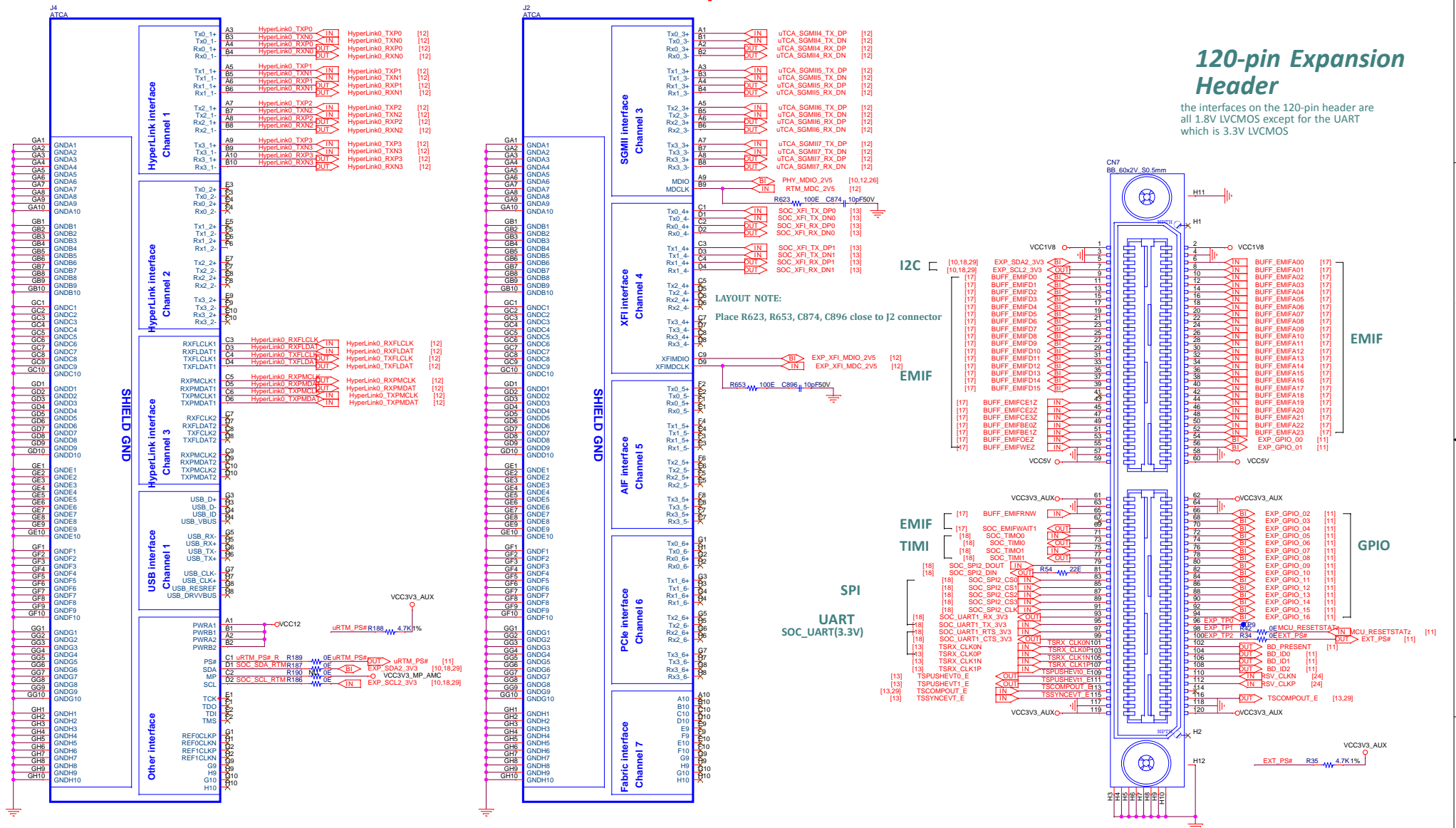
PMBus Address Pins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
SHORT	--

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Note : J4 connector close to AMC Interface.

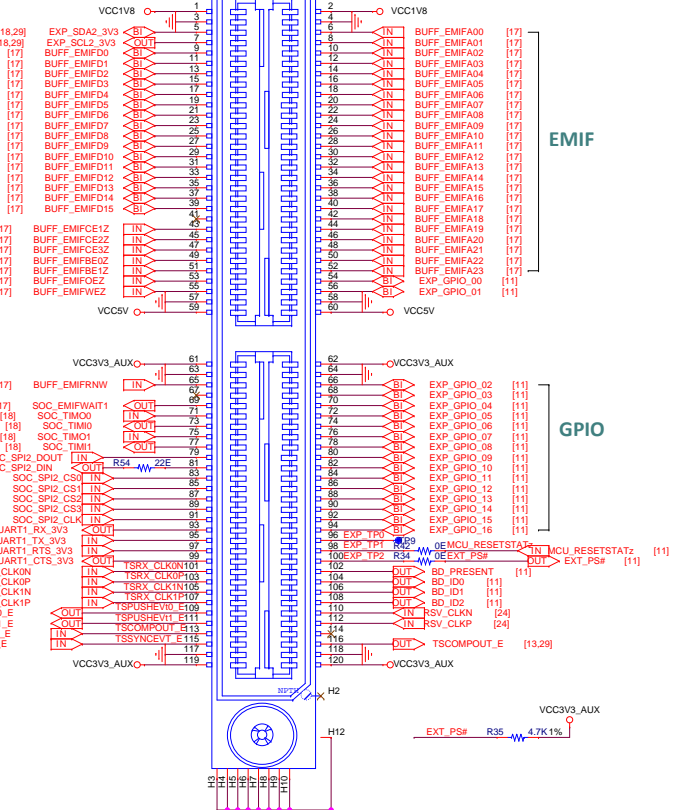
Note : J2 connector close to Key socket.



120-pin Expansion Header

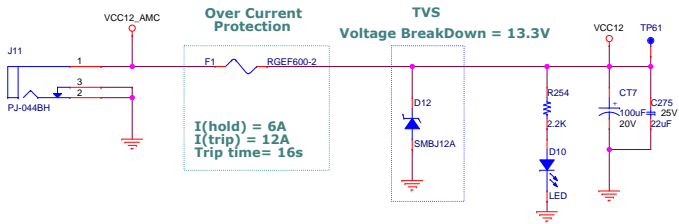
the interfaces on the 120-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS

LAYOUT NOTE:
Place R623, R653, C874, C896 close to J2 connector

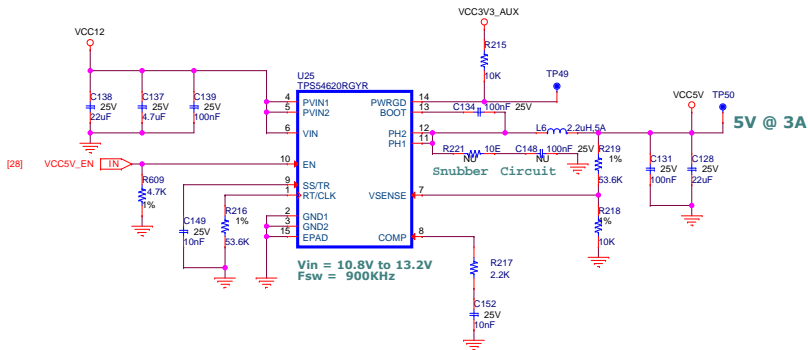


Project	K2E EVM		Designed for TI by elnfochips	
Title	UTCA AND EXPANSION			
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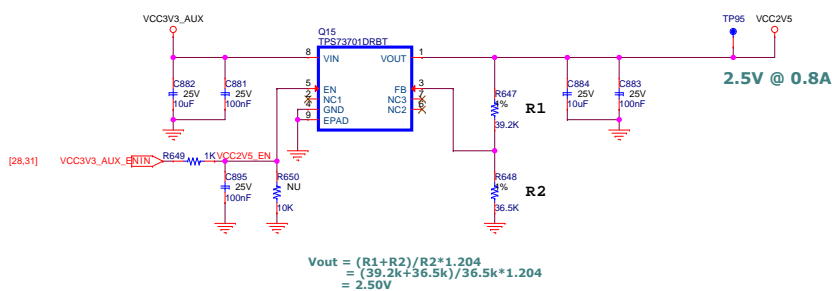
VCC12@5A INPUT



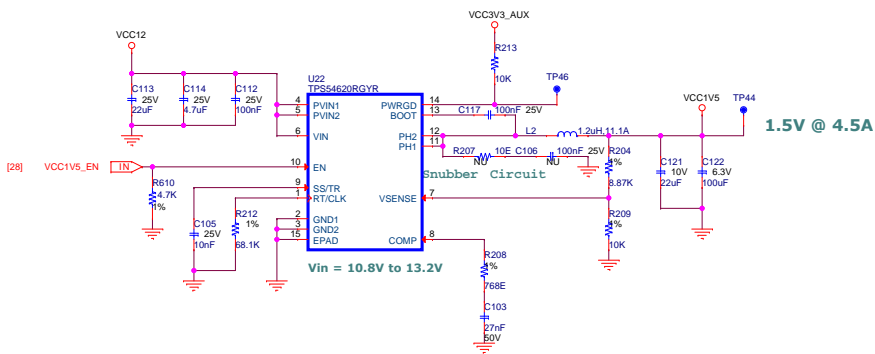
12V to 5V Generation



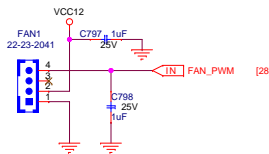
3.3V_AUX to 2.5V Generation



12V to 1.5V Generation



DC FAN Connector for SOC



$$V_{OUT} = 0.8 * (R1/R2 + 1) = 0.8 * (53.6/10 + 1) = \sim 5V$$

$$R_{rt} = 48000 * F_{sw}(kHz)^{-0.997} - 2 = 48000 * 900^{-0.997} - 2 = \sim 52.5 \text{ Kohms}$$

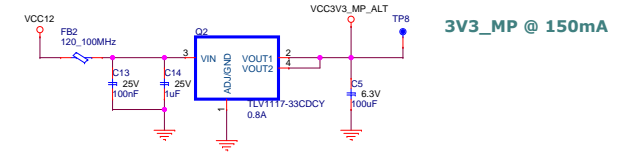
$$\text{OUTPUT CAPACITOR CALCULATION} \\ C_{out} = 2 * \Delta(I_{out}) / (F_{sw} * \Delta(V_{out})) = 2 * 1 / (900kHz * 0.25) = \sim 9\mu F$$

REFERENCE CAPACITOR = 22uF

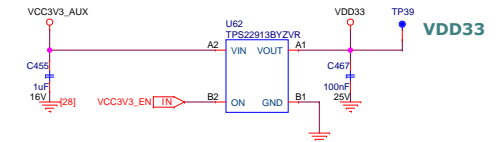
$$\text{INDUCTOR CALCULATION} \\ L = (V_{in} - V_{out}) / (I_{out} * K_{ind}) * (V_{out} / (V_{in} * F_{sw})) = (12 - 5) / (3 * 0.3) * (5 / (12 * 900kHz)) = 7.78 * 0.46\mu = \sim 3.6\mu H$$

REFERENCE CAPACITOR = 2.2uH

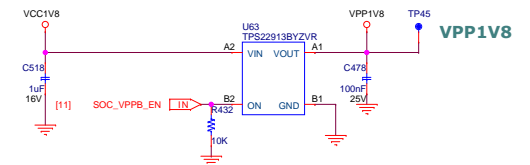
12V to VCC3V3_MP_ALT Generation



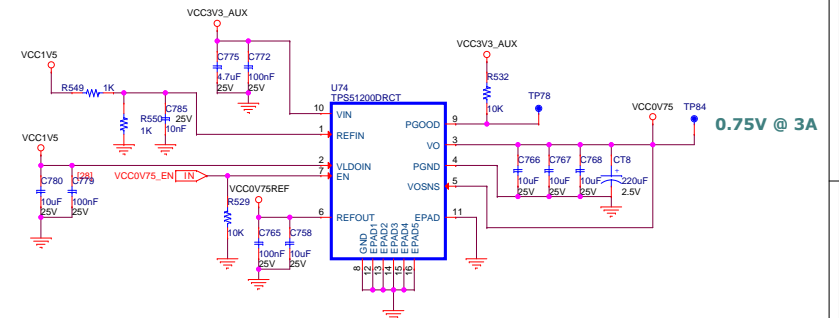
3V3_AUX to VDD33 Generation

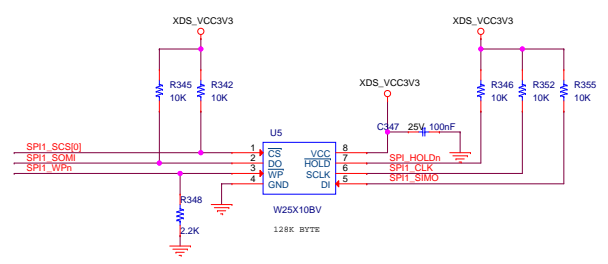
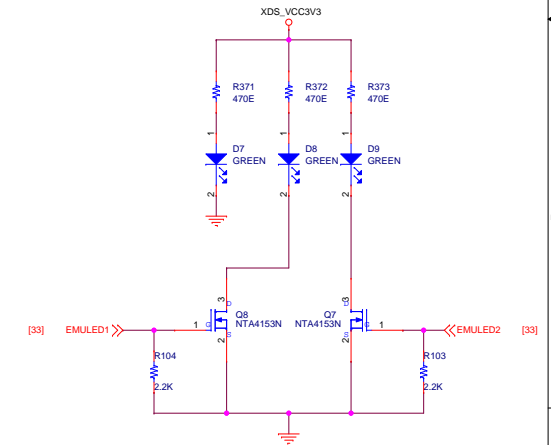
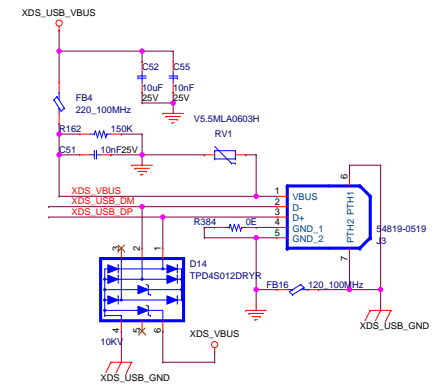
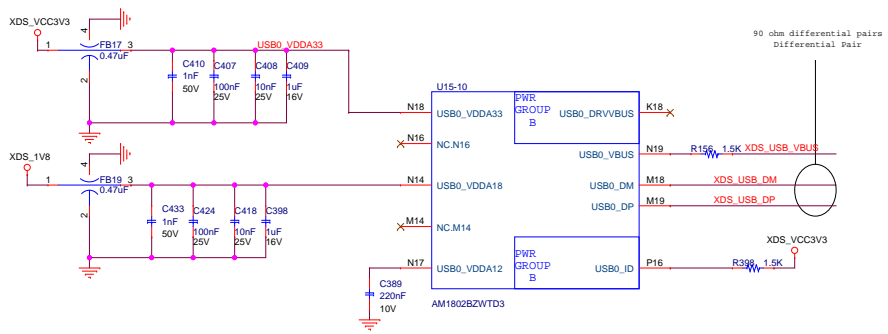
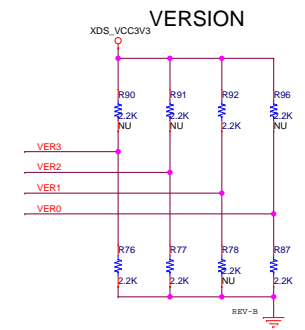
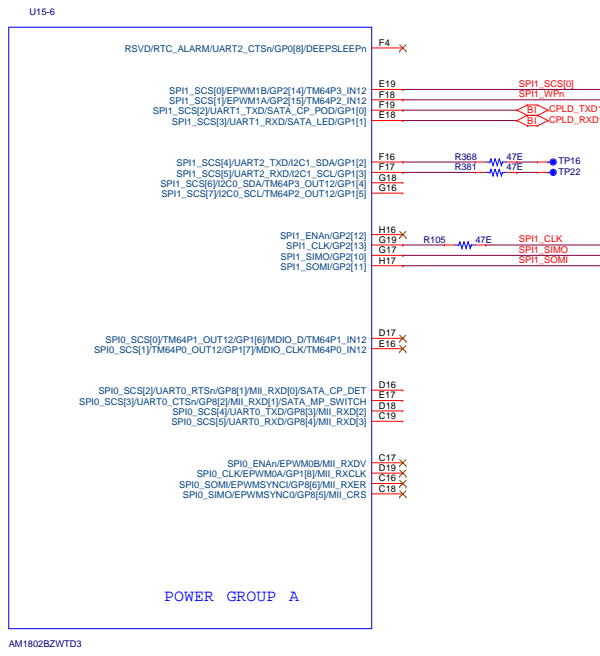
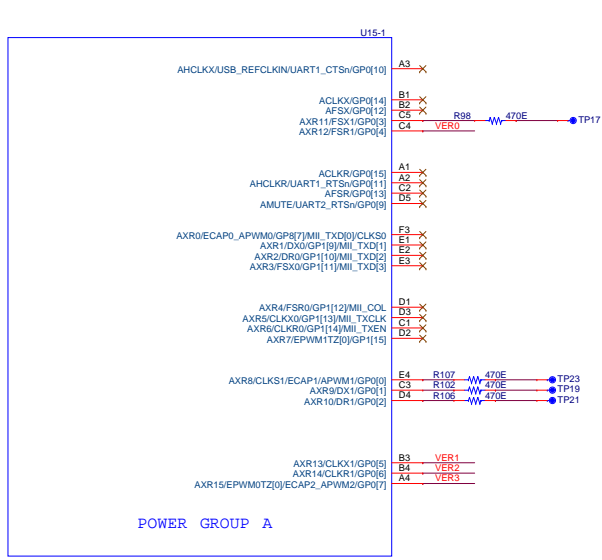


VCC1V8 to VPP1V8 Generation

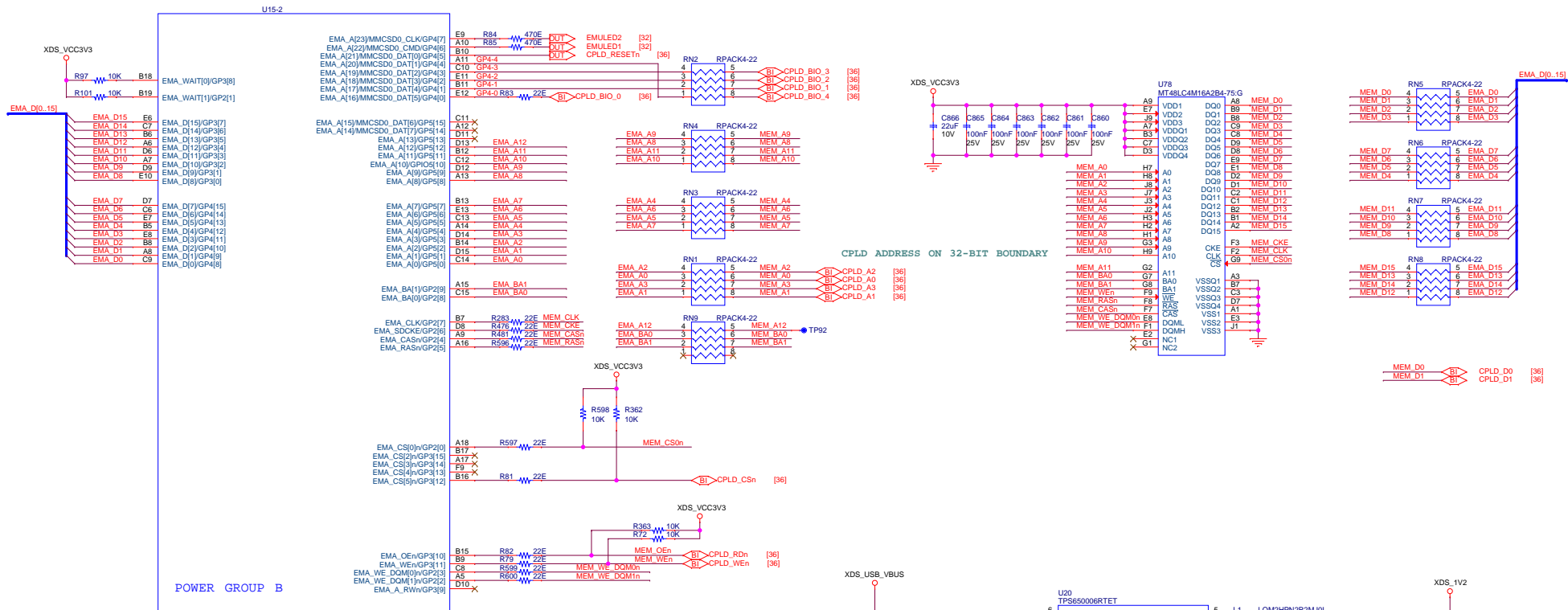


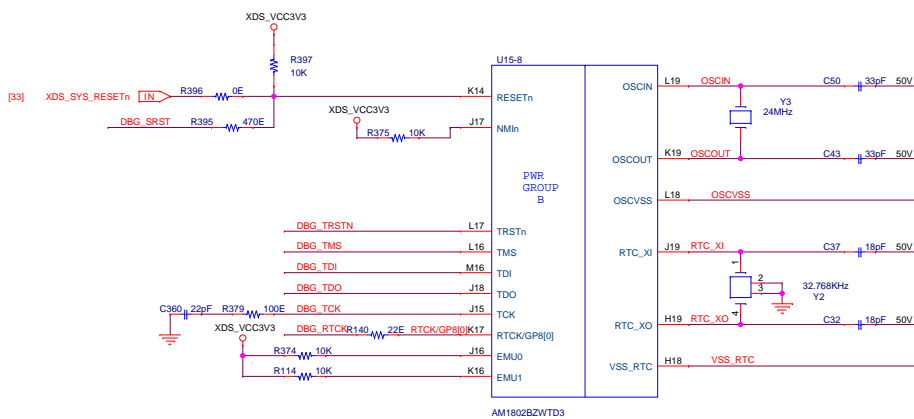
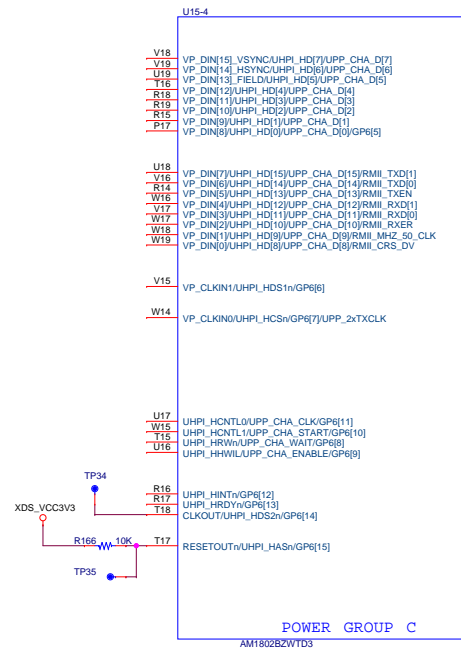
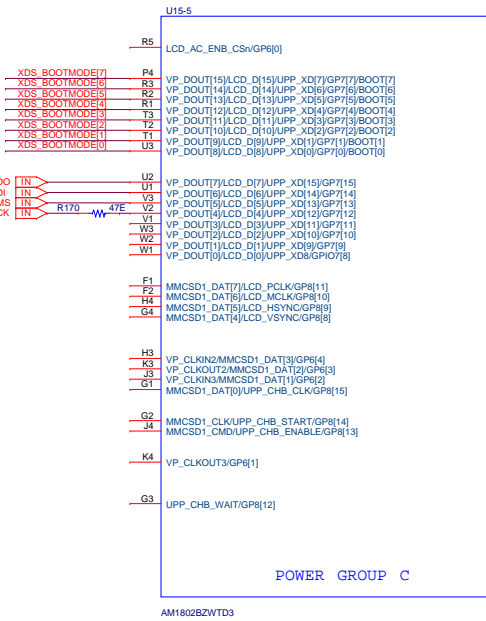
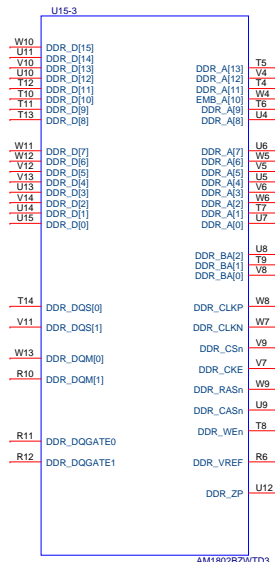
1.5V to 0.75V Generation



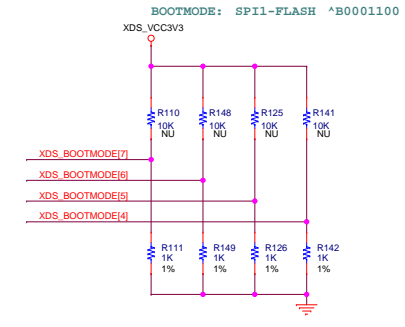
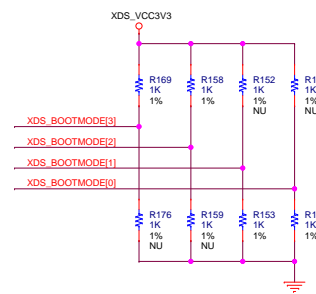


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Size C	Document Number 16_00175_02	Rev 2.01	
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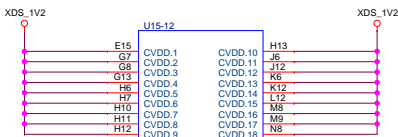
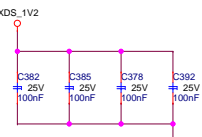
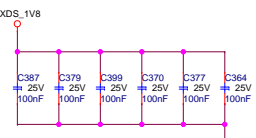
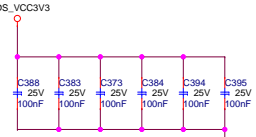
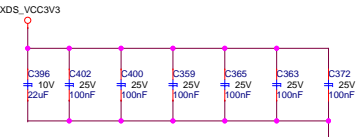
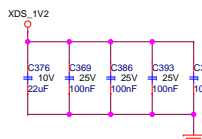
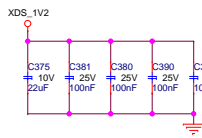




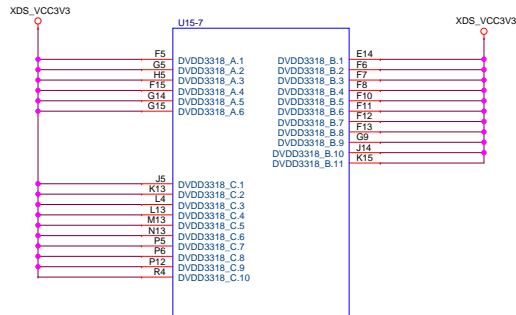
BOOT MODE



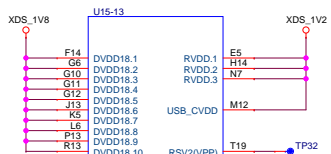
Project K2E EVM		Designed for TI by elnfochips	
Title XDS200_3			
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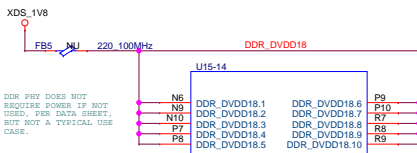
AM1802B2WTD3



AM1802B2WTD3

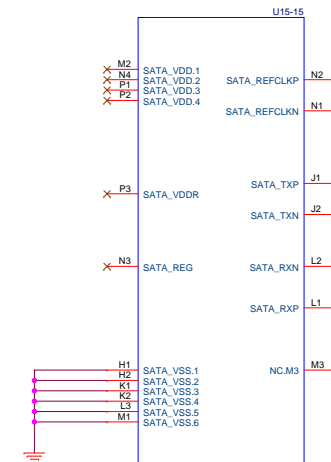


AM1802B2WTD3

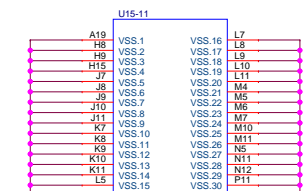


AM1802B2WTD3

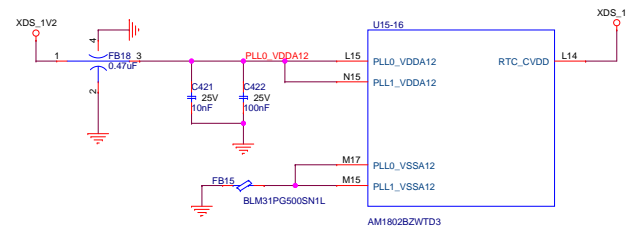
DDR PHY DOES NOT REQUIRE POWER IF NOT USED, PER DATA SHEET, BUT NOT A TYPICAL USE CASE.



NOT USED AM1802B2WTD3



AM1802B2WTD3



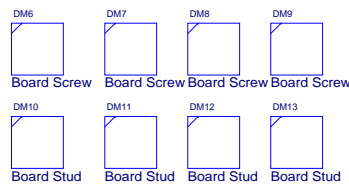
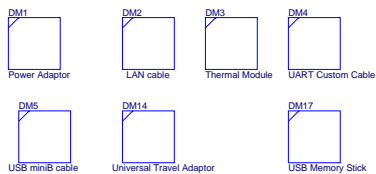
AM1802B2WTD3

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K2E EVM - REVISION HISTORY

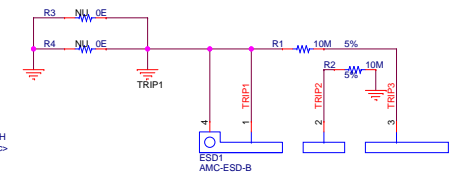
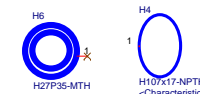
PCB REV.	SCH. REV.	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	1.0	Released to Fabrication	15-NOV-2013	eInfochips
2.0	1.01	1) LM26430: Pin#39 and #44 swapped - R575 marked as NU 2) CDCM6208V1: CLK_RSTz connection near to U17 is corrected - R601/R602 added on U17_Sec input - SGMII_CLKP/N shifted to Y5 from Y1 3) BMC: DSP_PMBUS_EN changed to PF0 from PE2 4) XDS200: Added a SDRAM & related circuitry - U20 part# changed to TPS650006, fixed version of TPS65000, Changed R185, R194, R202 to 0E and Marked R180, R196, R199, C100 as NU 5) Power: R603 added, R604 - R610 added and marked them as NU	03-JAN-2014	eInfochips
	1.02	1) Power: R611, R612 (NU) added on LM10011 Mode pin 2) TA: IC part# changed to TPS544C24 in place of TPS544B24 - R268 changed to 127K, R590 changed to 215K, R587 changed to 6.81K - TP added near to R547 on VSSCMON signal - RC Snubber package size changed 3) LM26430: TP added on CE pin 4) CP2105: Added support for Self-Power operation	21-JAN-2014	eInfochips
	1.03	1) LEDs: R47,R71 and R73 values changed to 120E 2) Added AC termination on MDC and MDIO (NU) signals near AMC EDGE connector and RTM connector 3) Configured PHY1 and PHY2 to operate at 2.5V I/O. 4) Added 2.5V LDO for PHY I/O 5) Added buffer on SGMII and XFI MDC signals and added pull-up on MDIO signals 6) U79 added for PMBUS_ALERT signal connection to SoC 7) SoC RSVxxx pin net names changed	25-FEB-2014	eInfochips
	1.04	- Released for Fabrication	05-MAR-2014	eInfochips
	2.0	- Block Diagram, aesthetical changes made	10-MAR-2014	eInfochips
	2.01	- Added 10K pull up resistor on "MMC_EN_N" signal - Mounted 4.7K pull down resistors on R606,R607,R604,R609,R610,R608 - Removed 10K pull up resistor and added 10K pull down resistor on "uTDIS" signal at XDS200 CPLD. - Added 10K pull down resistor on "MAIN_POWER_GOOD" signal - Changed R590 resistor value to 182K	24-APR-2014	eInfochips

Dummy Components

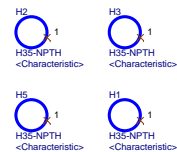


Front panel and ESD Strip

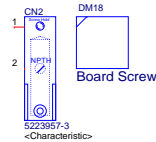
AMC Hole



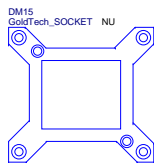
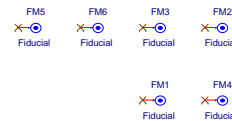
Mounting Holes



KEY ZONE



On Board Fiducials



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