TMDSEVM6657 SCHEMATIC

MAJOR REVISION HISTORY :

PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	0.6	Initial Draft	03-FEB-2012
	1.1	Release for Alpha Boards	20-MAR-2012
2.0	2.5	Release for Beta Boards	26-JUL-2012
	2.9	Redundant pull-up and termination NU on EMU_TCK	28-NOV-2013

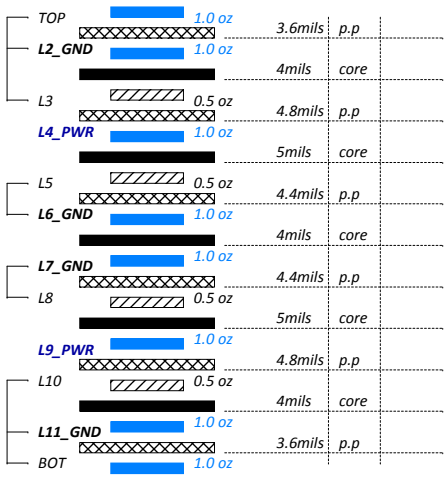
I2C ADDRESS TABLE :

REF DES	DESCRIPTION	7 BIT ADDRESS
EEPROM1	DSP EEPROM	0x50, 0x51
U264	ETHERNET EEPROM	0x50

PCB MECHANICAL DETAILS :

1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. PCB MATERIAL: FR4_IT168G
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

PCB LAYER STACK-UP DETAILS :



NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.

DISCLAIMER: THIS CIRCUIT DESIGN IS PROVIDED AS REFERENCE ONLY, WITHOUT WARRANTY EXPRESSED OR IMPLIED. THE USER IS ENCOURAGED TO PERFORM ALL DUE DILIGENCE WITH RESPECT TO DESIGN AND ANALYSIS. FOR COMMITTED PERFORMANCE AND FUNCTIONALITY OF THE xxxx DEVICE, PLEASE REFER TO THE DEVICE DATA MANUAL.

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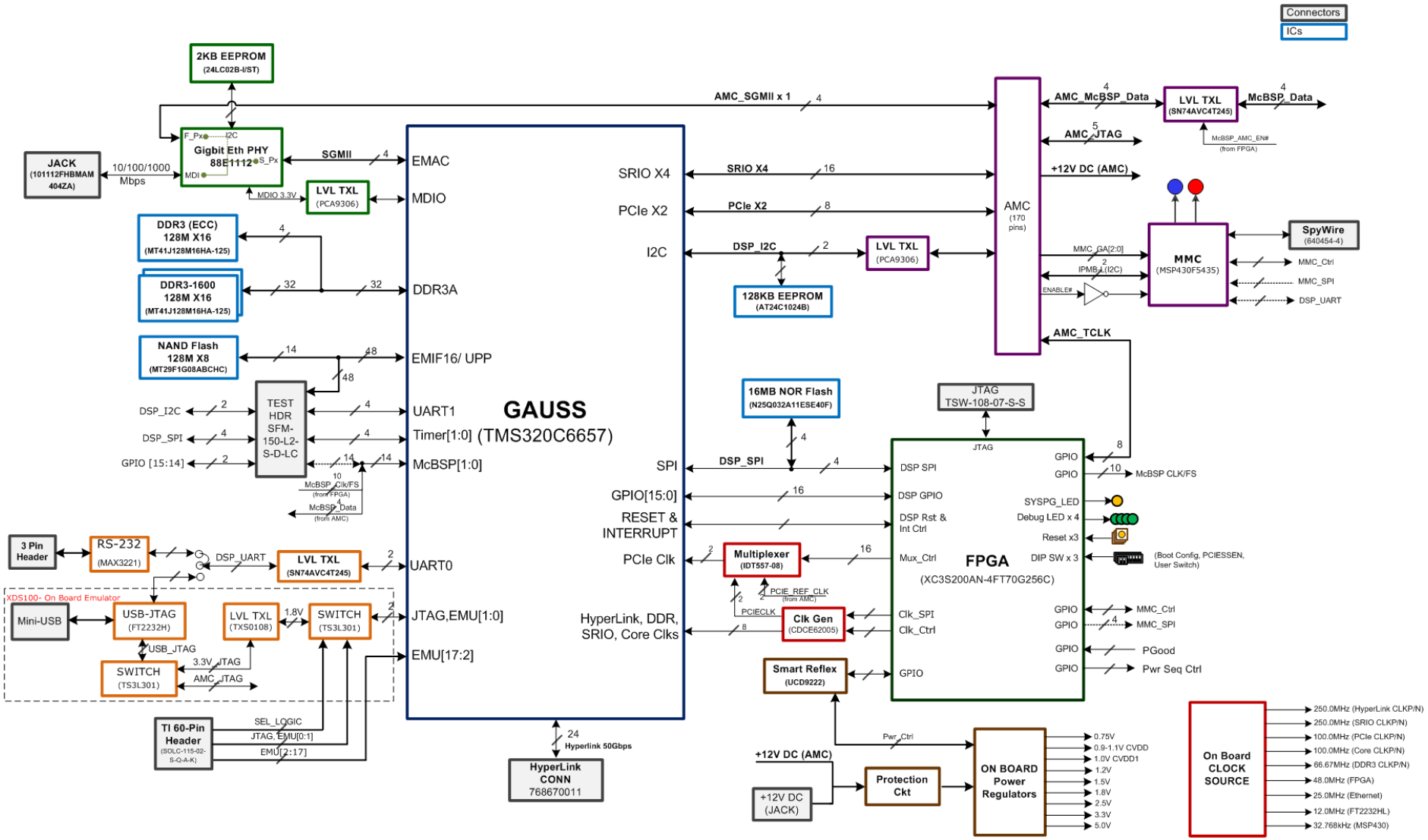
SCHEMATIC PAGE DESCRIPTION :

01 : COVER PAGE
02 : TABLE OF CONTENTS
03 : SYSTEM BLOCK DIAGRAM
04 : PLACEMENT
05 : POWER CONSUMPTION
06 : POWER SEQUENCE
07 : POWER DISTRIBUTION
08 : CLOCK DIAGRAM
09 : FPGA INTERFACE CONTROL
10 : MANAGEMENT MAP
11 : AMC CONNECTOR
12 : MMC, HYPERLINK COMM
13 : DSP - SERDES PORTS
14 : DSP - DDR3
15 : DDR3 & ECC
16 : DSP - EMIF & JTAG
17 : DSP - MISC
18 : DSP - CLOCK & SMART REFLEX
19 : CLOCK GENERATION
20 : USB - JTAG
21 : GIGABIT ETHERNET
22 : FPGA - POWER, RESET CTRL, McBSP
23 : FPGA - BOOT_MODE & SMART REFLEX
24 : DSP - POWER 1
25 : DSP - POWER 2
26 : SMART REFLEX & CORE VOLT
27 : POWER SUPPLY 1
28 : POWER SUPPLY 2
29 : REVISON HISTORY

BLOCK DIAGRAM



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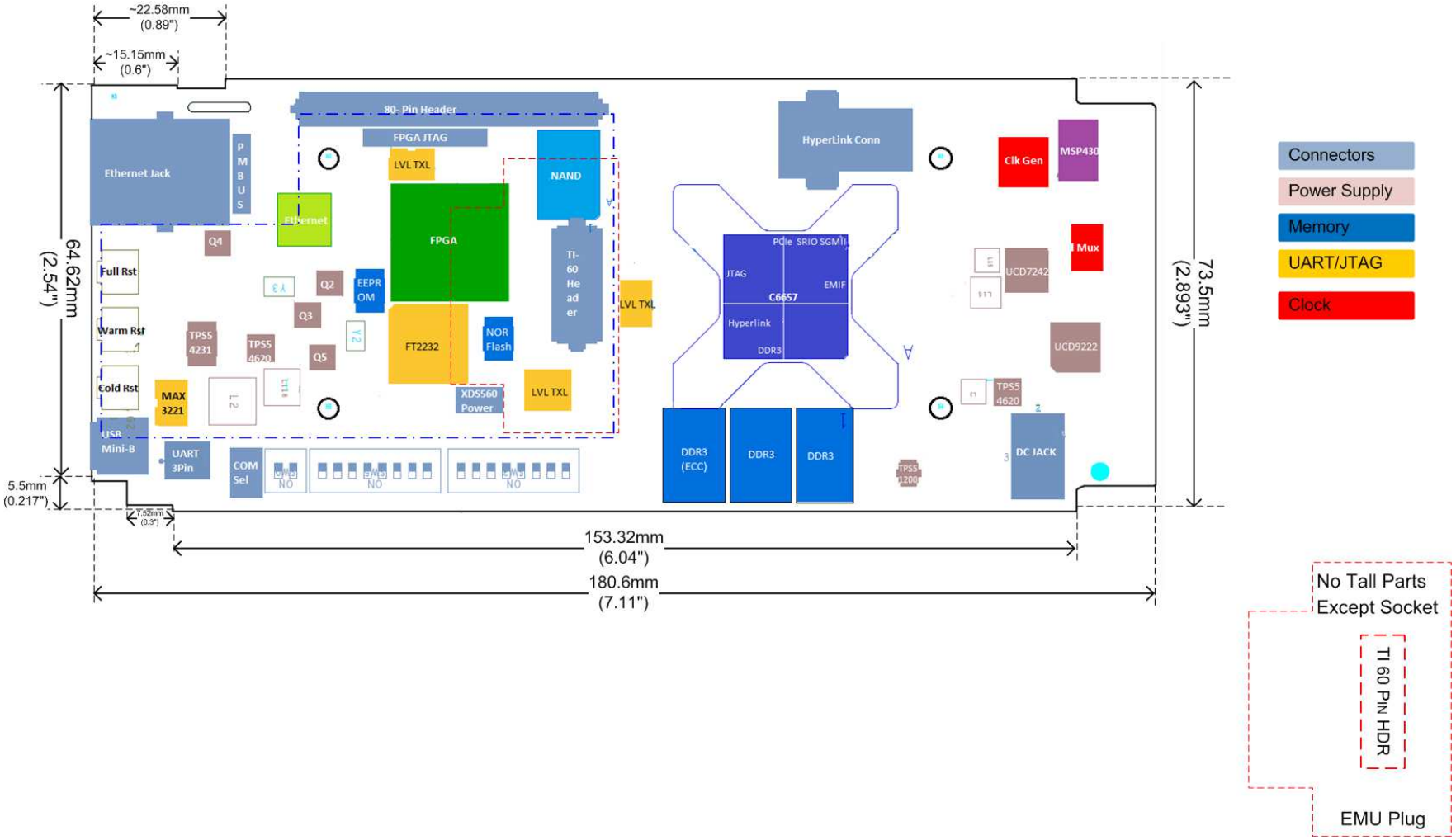
PLACEMENT



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POWER CONSUMPTION

Components Part No.	Description	Quantity Per Board	Current Consumed by corresponding device on power supply (mA)											Total Power (mW)
			0.75V	1.00V	1.00V	1.20V	1.50V	1.80V	1.80V	2.50V	3.30V	3.30V	5.00V	
				CVDD	CVDD1			AUX	VCC		AUX	AMC		
TMS320C6657	CPU	1		2500.00	1000.00		350.00		50.00					4115.00
XC3S200AN-4FTG256C	FPGA	1				125.00		200.00			24.00			589.20
MT41J128M16HA-125	DDR3 SDRAM	2	50.00				525.00							1650.00
MT41J128M16HA-125	DDR3 ECC	0	50.00				525.00							0.00
NAND512R3A2SZA6E	NAND Flash (64MB)	1							15.00					27.00
AT25128B	SPI EEPROM	1									10.00			33.00
FT2232H	USB to JTAG convertor	1							70.00		210.00			819.00
88E1112	Ethernet	1				320.00				338.00				1229.00
MSP430	MMC	1										48.00		158.40
CDCE62005	Clock Generator	1									500.00			1650.00
XDS560v2	XDS560v2 Mezzanine	1									300.00		600.00	3990.00
	Misc	1						100.00			300.00			1170.00
Total Current on individual power supply (mA)			**100.00**	**2500.00**	**1000.00**	**445.00**	**1400.00**	**300.00**	**135.00**	**338.00**	**1344.00**	**48.00**	**600.00**	
5% margin added over design (mA)			**105.00**	**2625.00**	**1050.00**	**467.25**	**1470.00**	**315.00**	**141.75**	**354.90**	**1411.20**	**50.40**	**630.00**	
Power Consumption in (mW)			**78.75**	**2625.00**	**1050.00**	**560.70**	**2205.00**	**567.00**	**255.15**	**887.25**	**4656.96**	**166.32**	**3150.00**	**16202.13**

Vin		
3.3V	TPS73701 -- 3.3V_Aux to 2.5V regulation	372.65 mA
3.3V	TPS73701 -- 3.3V Aux to 1.8V Aux regulation	330.75 mA
3.3V	TPS73701 -- 3.3V Aux to 1.8VCC regulation	148.84 mA
3.3V	TPS73701 -- 3.3V Aux to 1.2V regulation	490.61 mA
1.5V	TPS51200 -- 1.5V to 0.75V regulation	110.25 mA
12.0V	UCD7242 -- 12V to 1V CVDD regulation	243.06 mA
12.0V	UCD7242 -- 12V to CVDD1 regulation	97.22 mA
12.0V	TPS54620 -- 12V to 1.5V regulation	219.48 mA
12.0V	TPS54620 -- 12V to 3.3V AUX regulation	946.70 mA
12.0V	TPS54231 -- 12V to 5V regulation	328.13 mA
	Total Current @12V	1.83A
	Total Current @3.3V AMC	0.05A
	Total Power Consumption	22.18W

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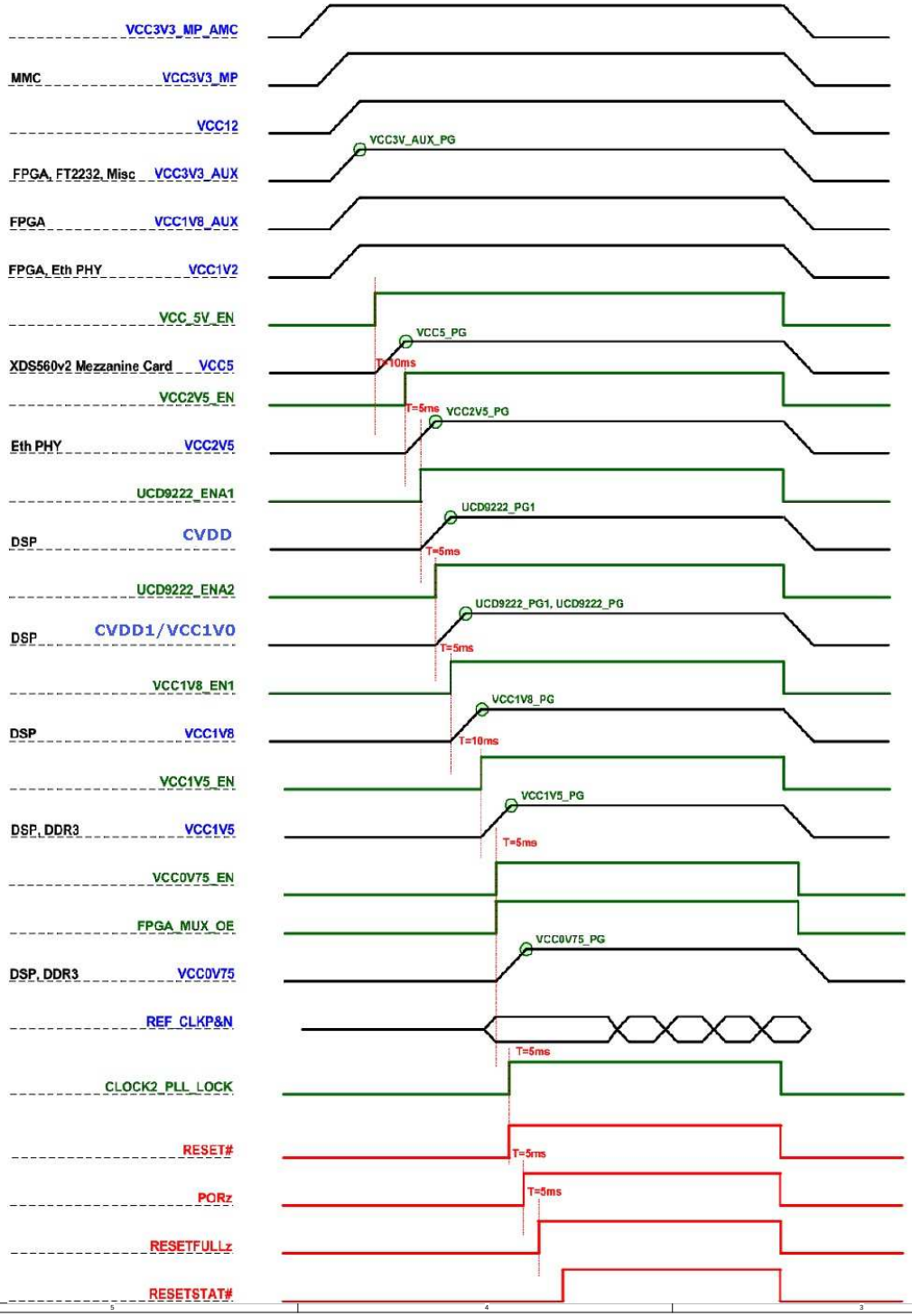
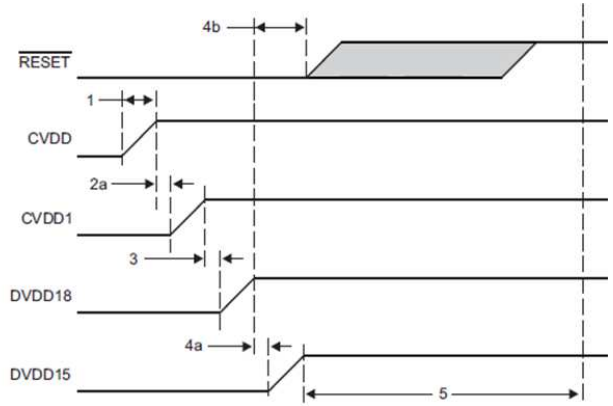
POWER SEQUENCE





C6657 Design :

1) CVDD1 should ramp at the same time or shortly following CVDD. Although simultaneous ramping is permitted, CVDD1 must never exceed CVDD until after CVDD has reached a valid voltage.

2) DVD15 supply is ramped up following DVDD18. Although ramping DVDD18 and DVDD15 simultaneously is permitted, DVDD15 must never exceed DVDD18.

3) There is no specific power-up nor power-down sequence defined for FPGA.

4) FPGA is first to come up and it generates ENABLE signal for all power supplies using PGOOD signals.

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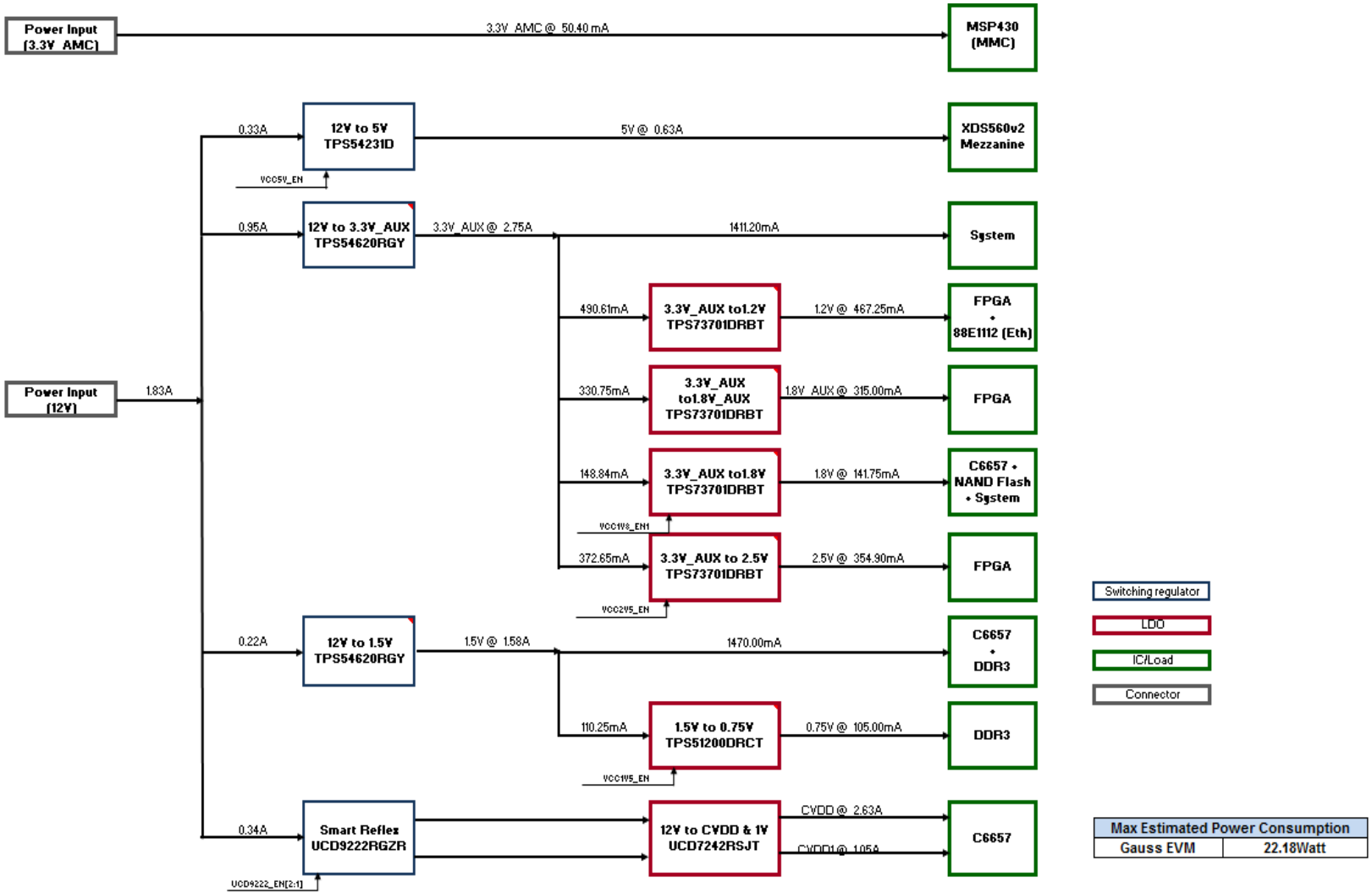
POWER DISTRIBUTION



Max Estimated Power Consumption	
Gauss EVM	22.18Watt

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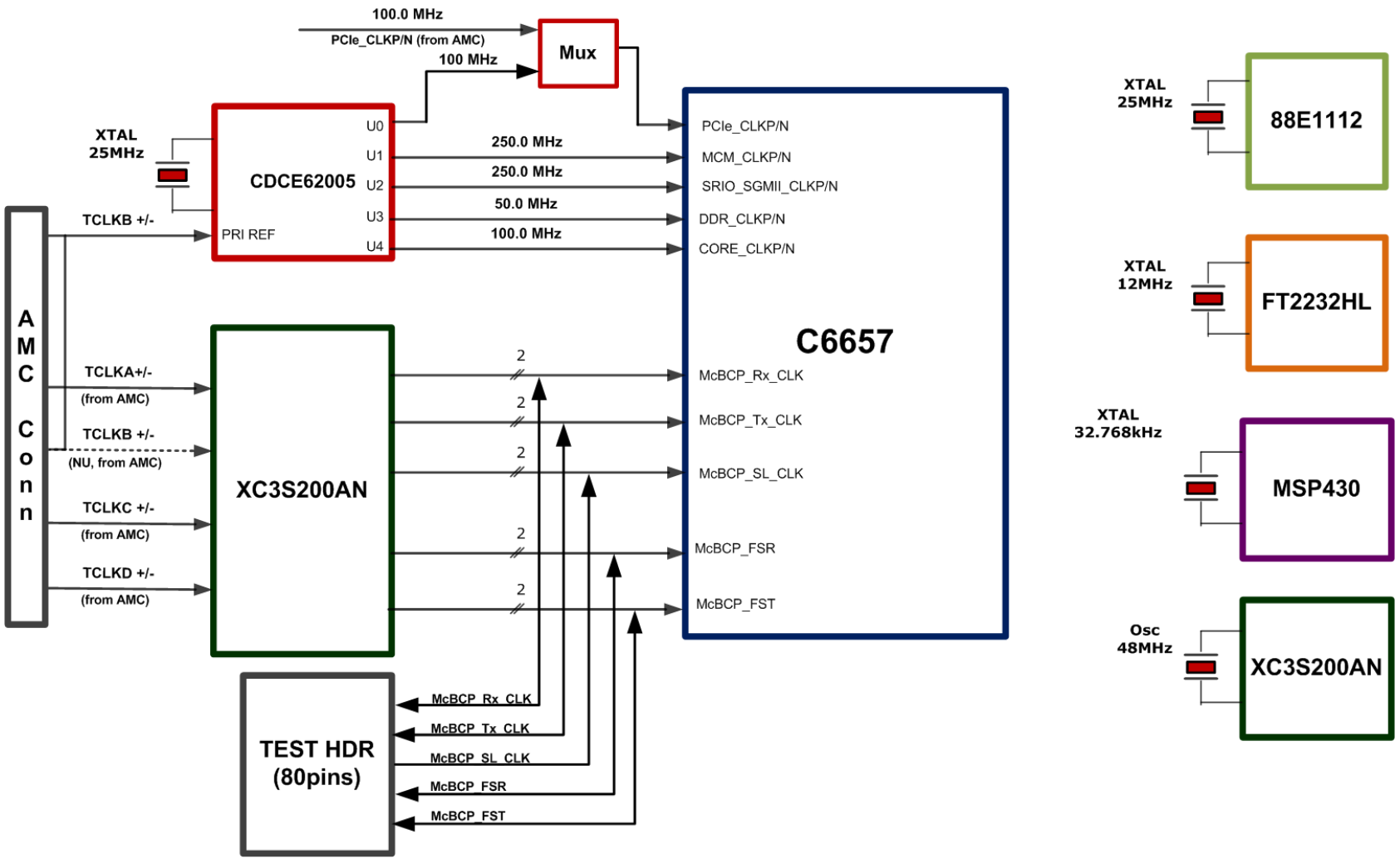
CLOCK DIAGRAM



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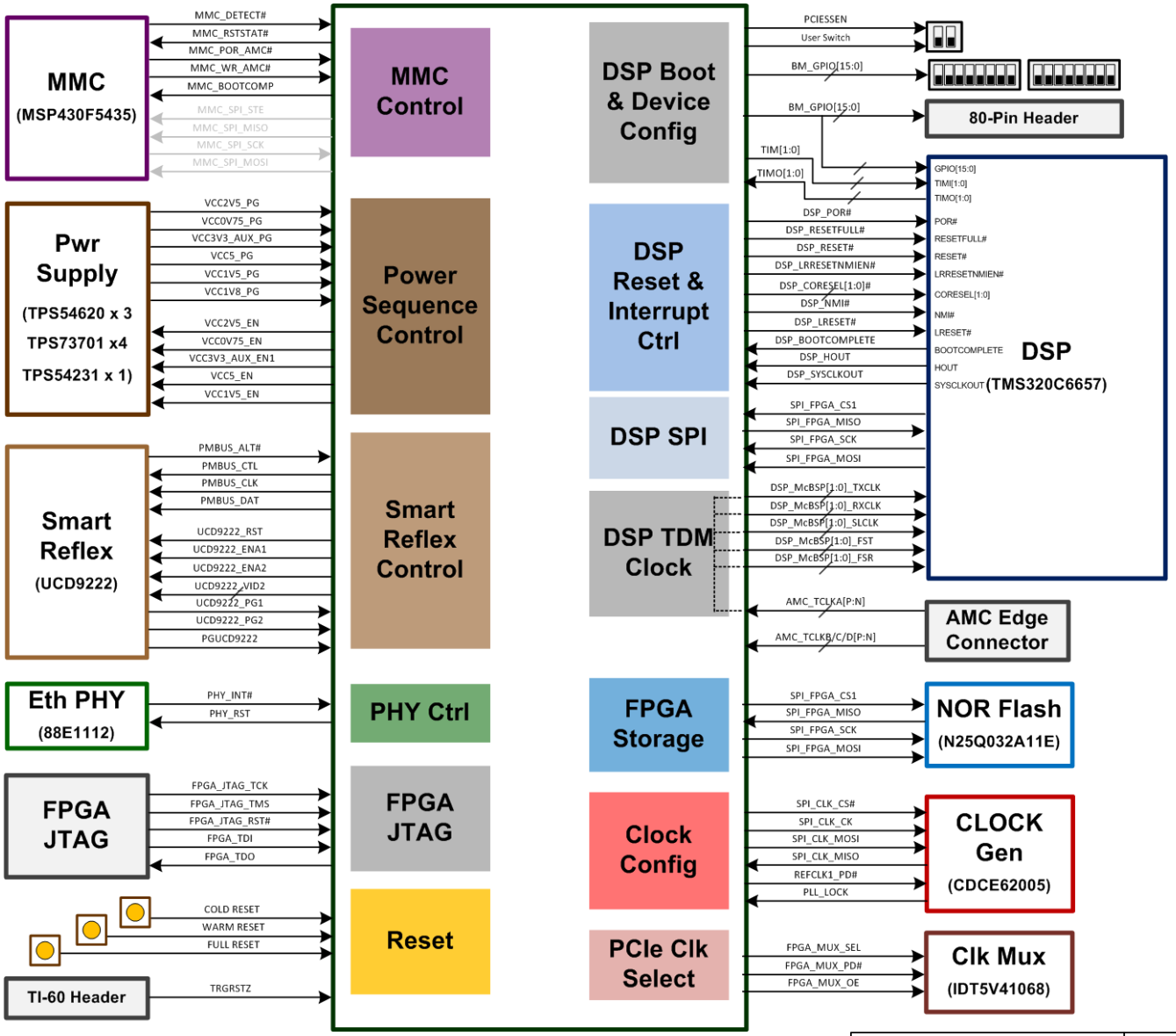
FPGA INTERFACE CONTROL DIAGRAM



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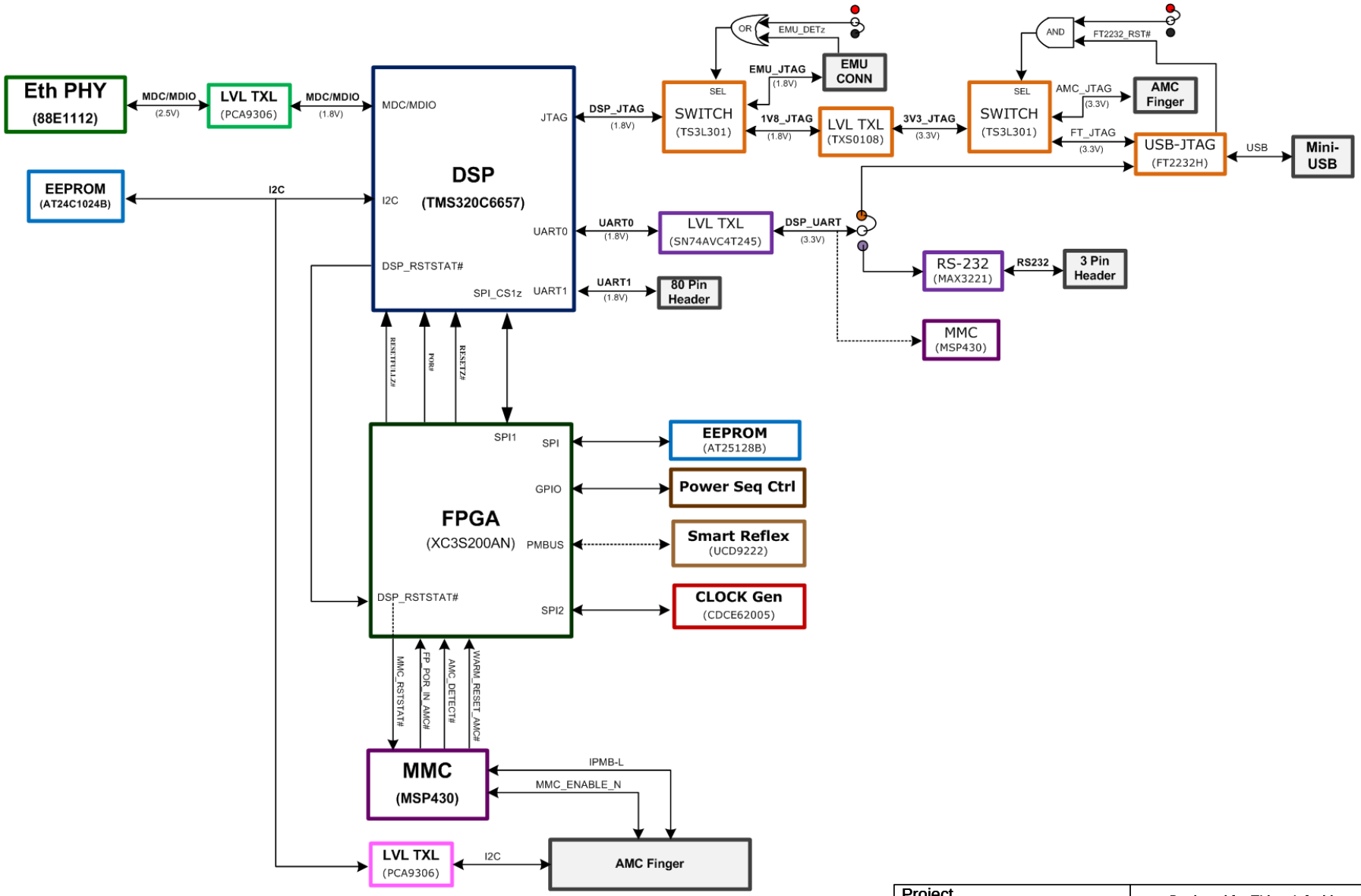
MANAGEMENT MAP



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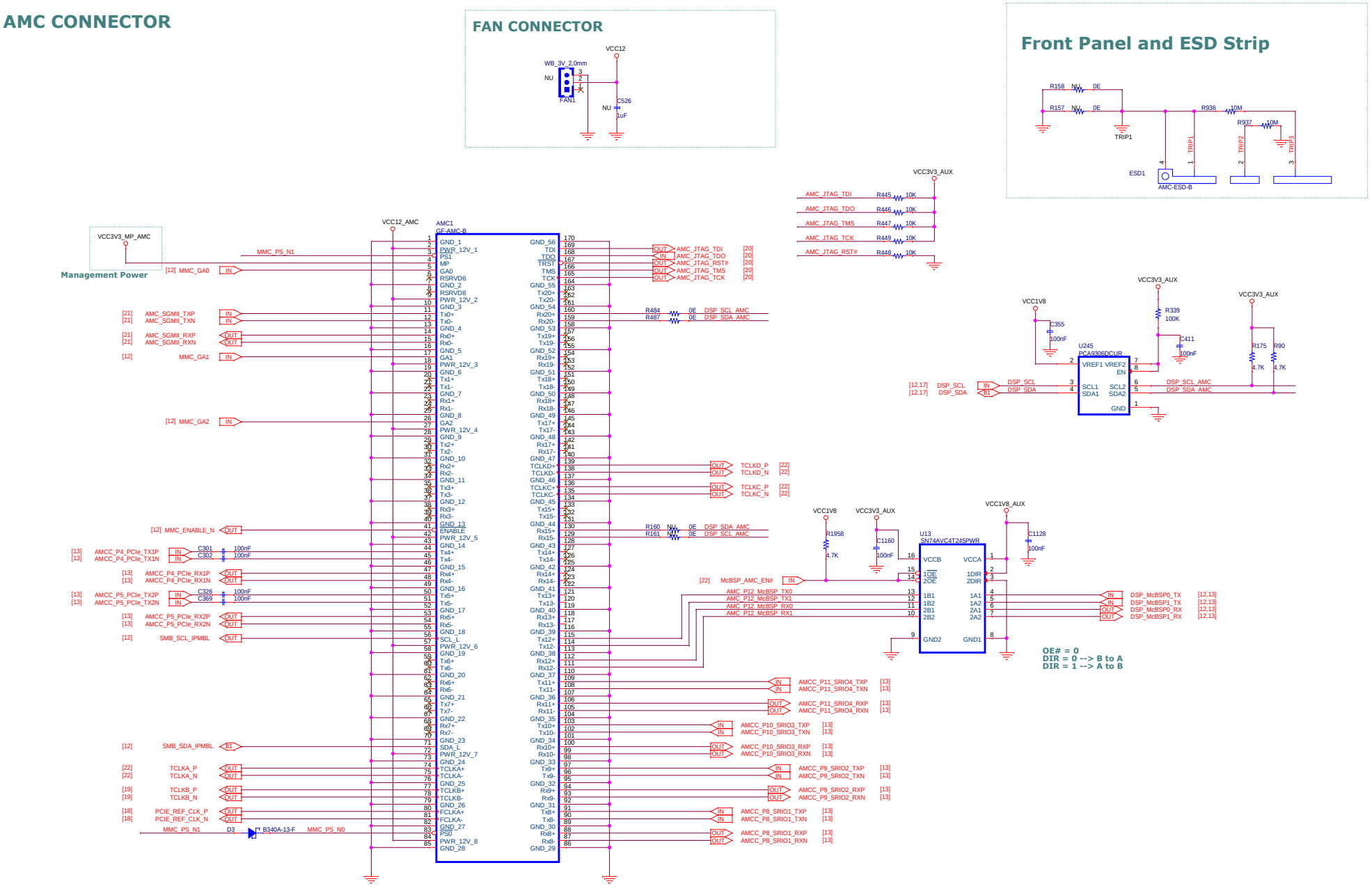
AMC CONNECTOR



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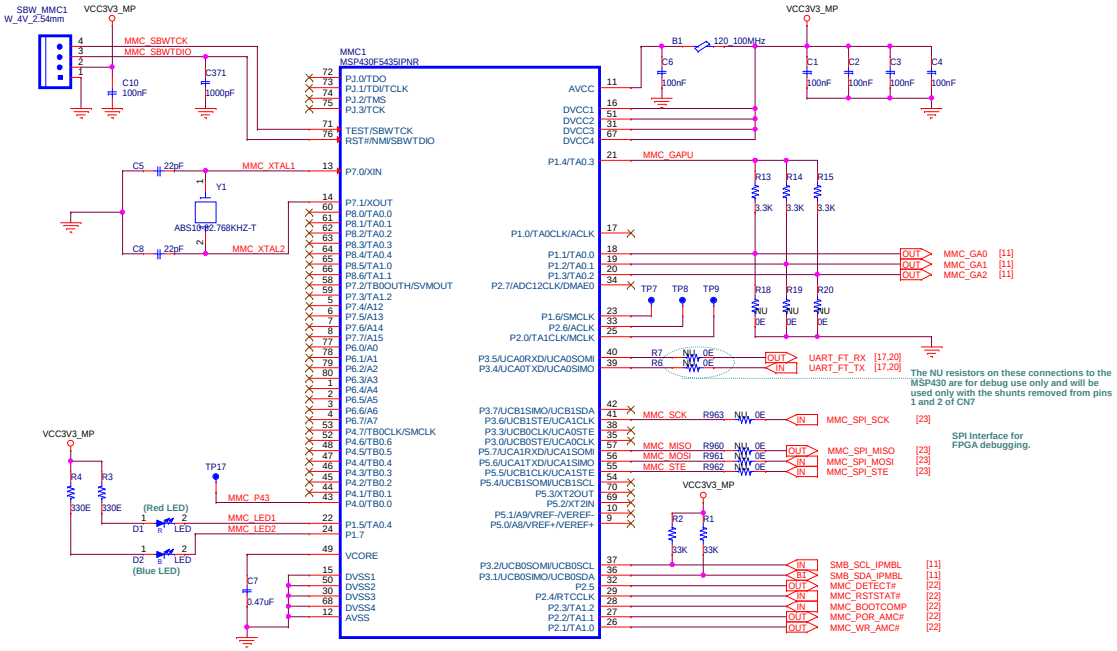
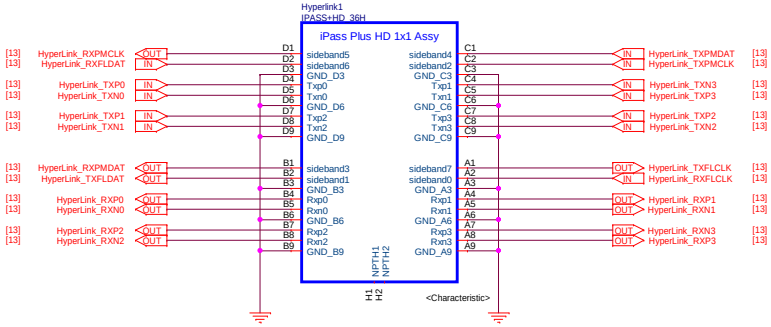
MMC INTERFACE

MSP430 Power

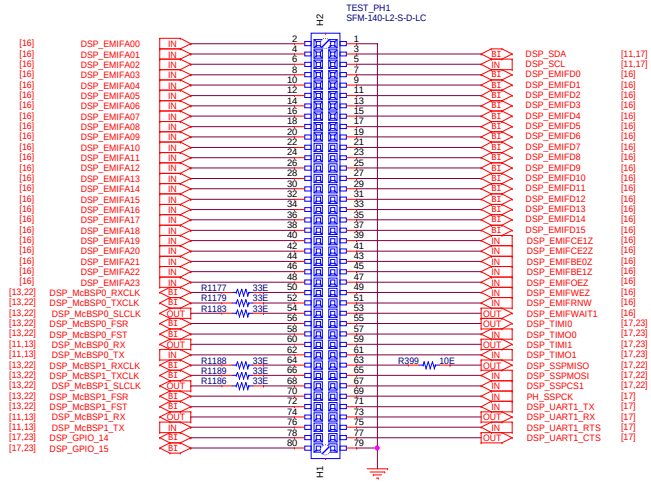
SpyBiWire



IPASS+HD for HyperLink



DEBUG HEADER



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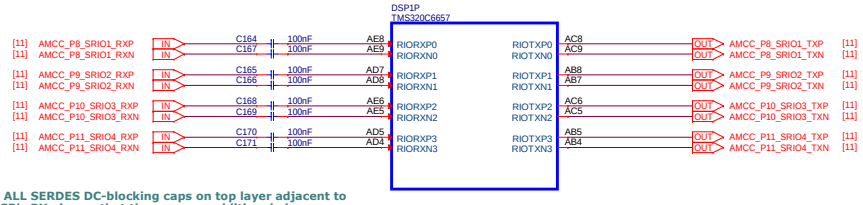
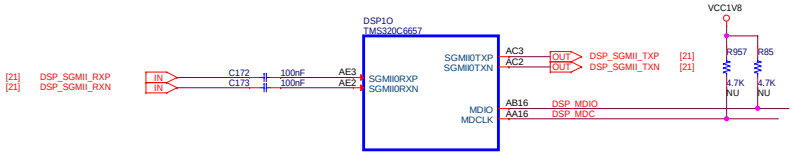
SRIO

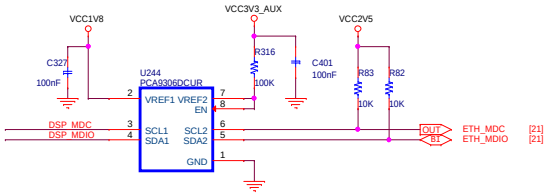


Place ALL SERDES DC-blocking caps on top layer adjacent to the DSP's RX pins so that there are no additional vias

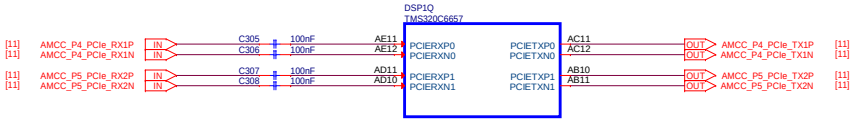
SGMII



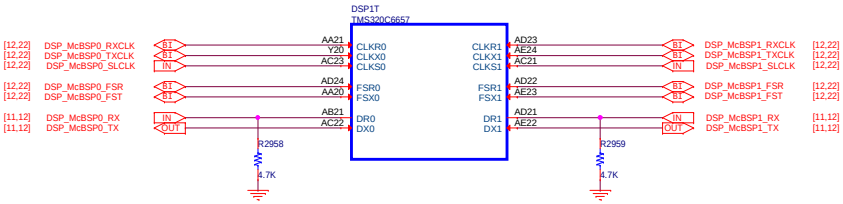
VOLTAGE LEVEL TRANSLATOR



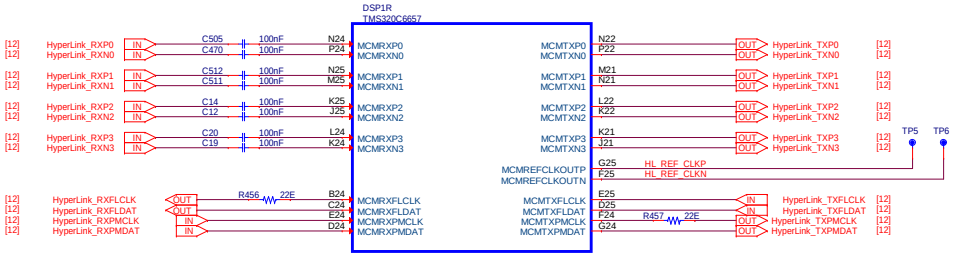
PCIE



McBSP



HYPERLINK



The HyperLink routes must have a max of 2 vias and no via stubs (Outer layer routing recommended)

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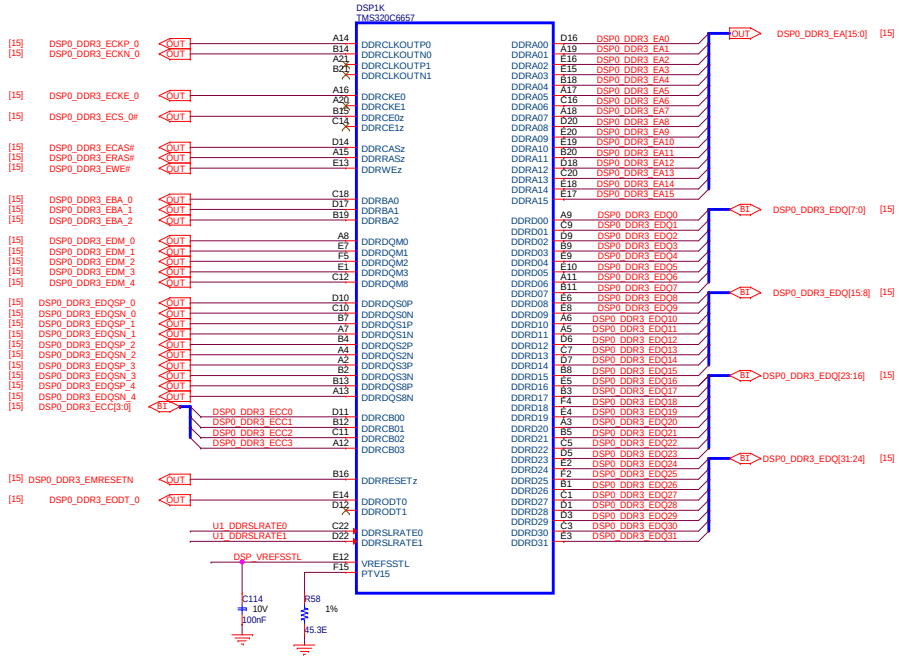
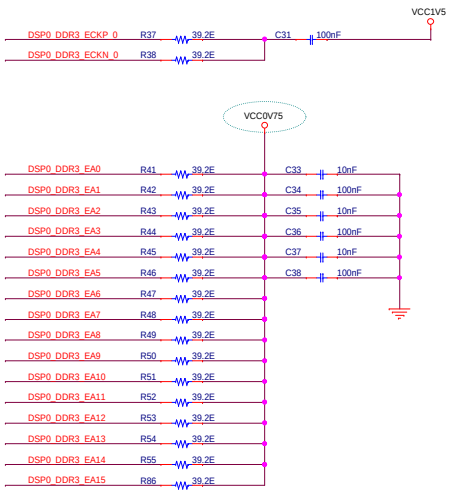
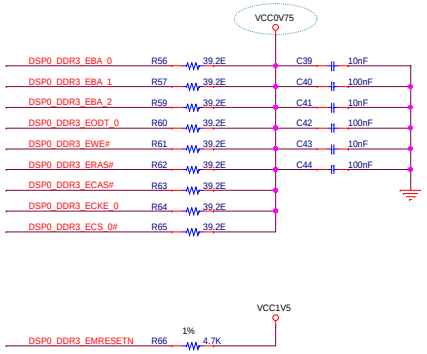
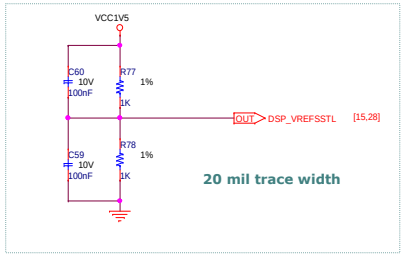
DDR3 INTERFACE



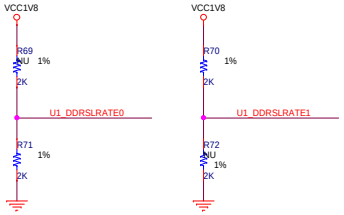


Place these resistors at the end of the trace.





20 mil trace width



DDR3 Slew-Rate Setting (DDRSLRATE[1:0]):

00 Fastest
01 Fast
10 Slow
11 Slowest

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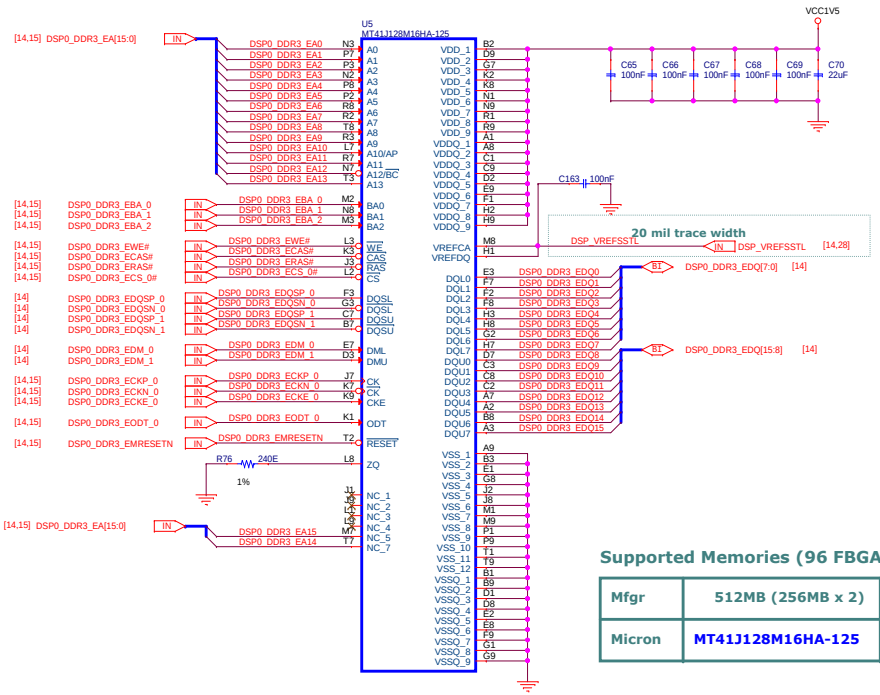
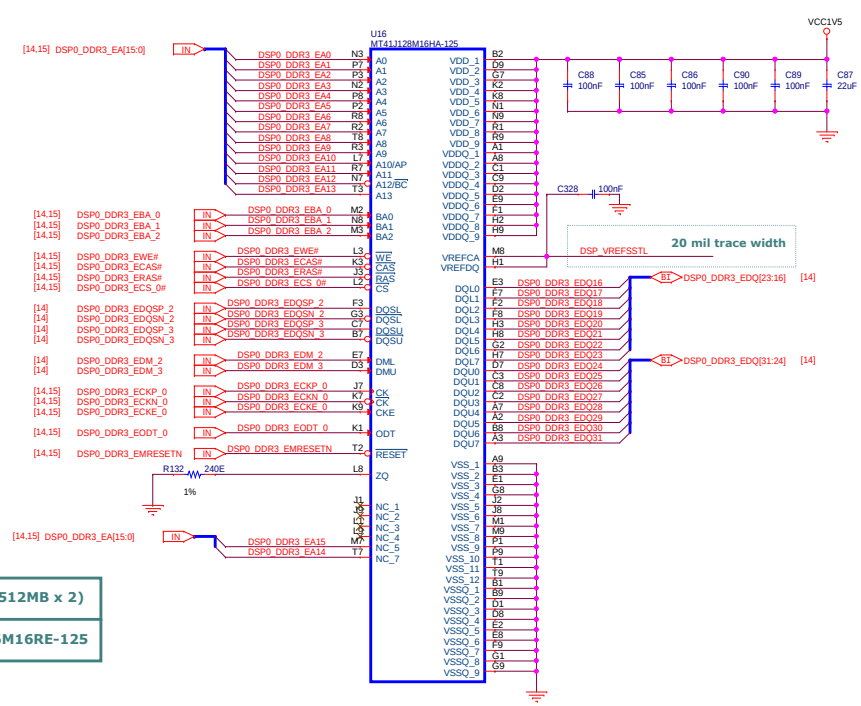
DDR3 MEMORY INTERFACE

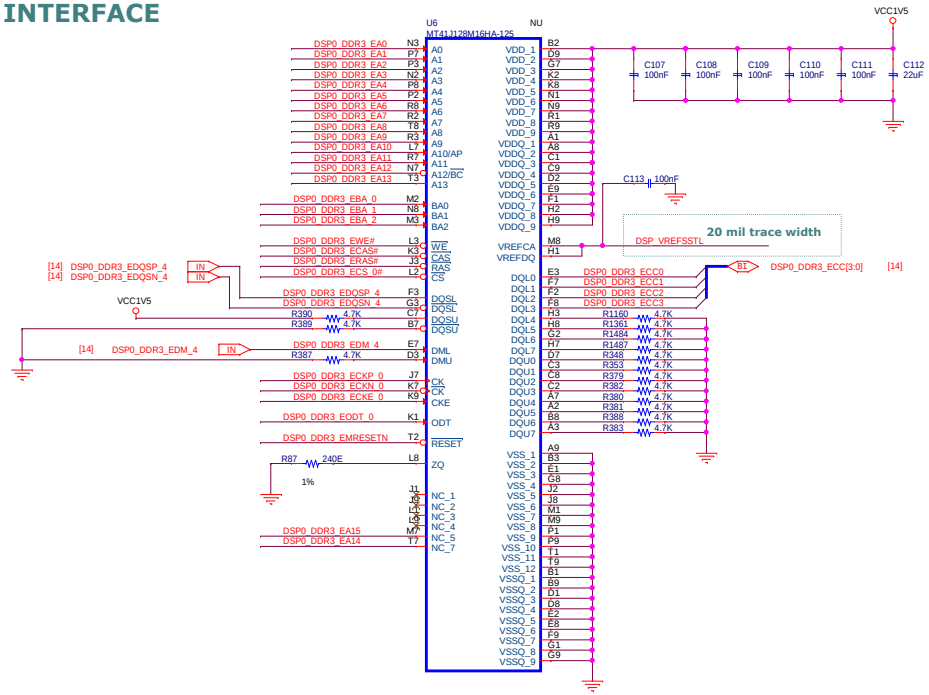




Supported Memories (96 FBGA) :

Mfgr	512MB (256MB x 2)	1024MB (512MB x 2)
Micron	MT41J128M16HA-125	MT41J256M16RE-125

DDR3 ECC INTERFACE



- Data bits can be swapped within the byte lane to ease routing.

- Address/Command/Control/Clock routing must be Fly-By in byte order ECC, 0, 1, 2, 3.

Supported ECC Chip (96 FBGA) :

Mfgr	256MB	512MB
Micron	MT41J128M16HA-125	MT41J256M16RE-125

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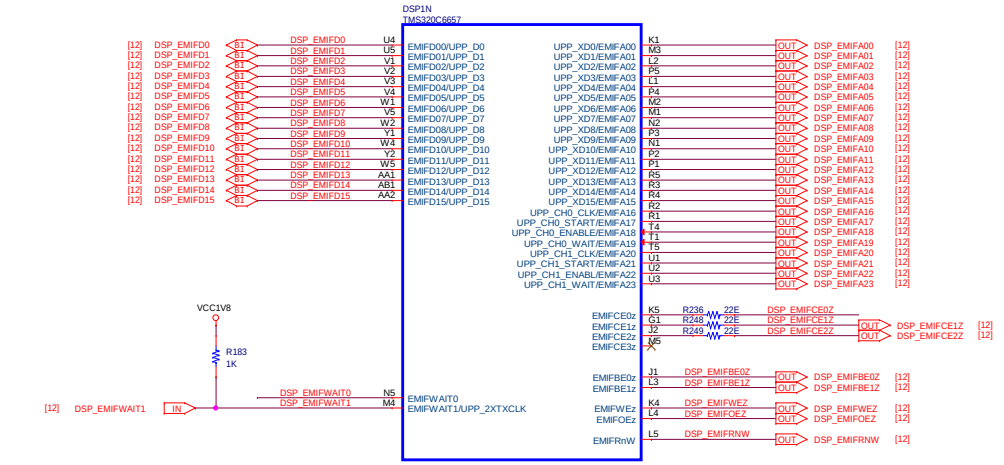
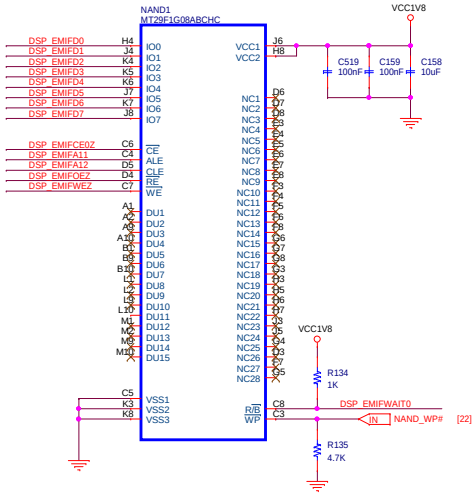
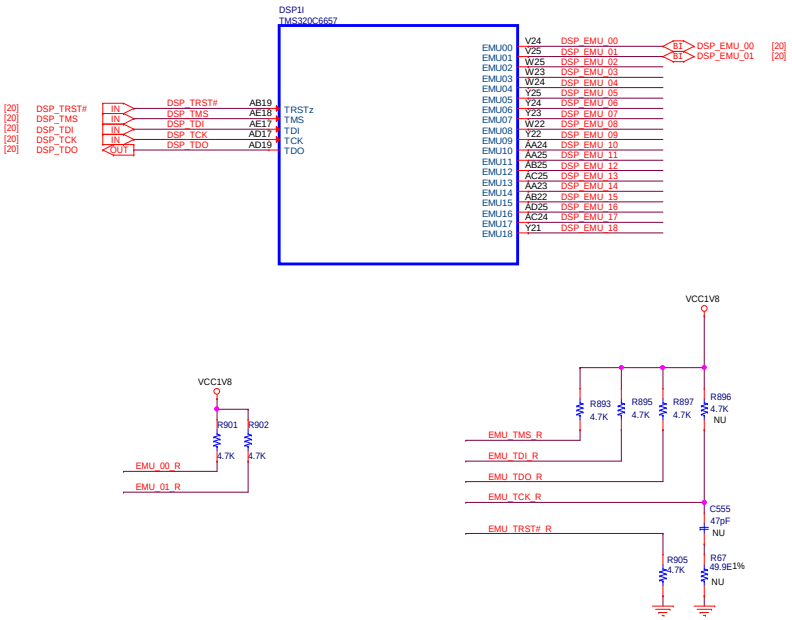
C6657 - EMIF



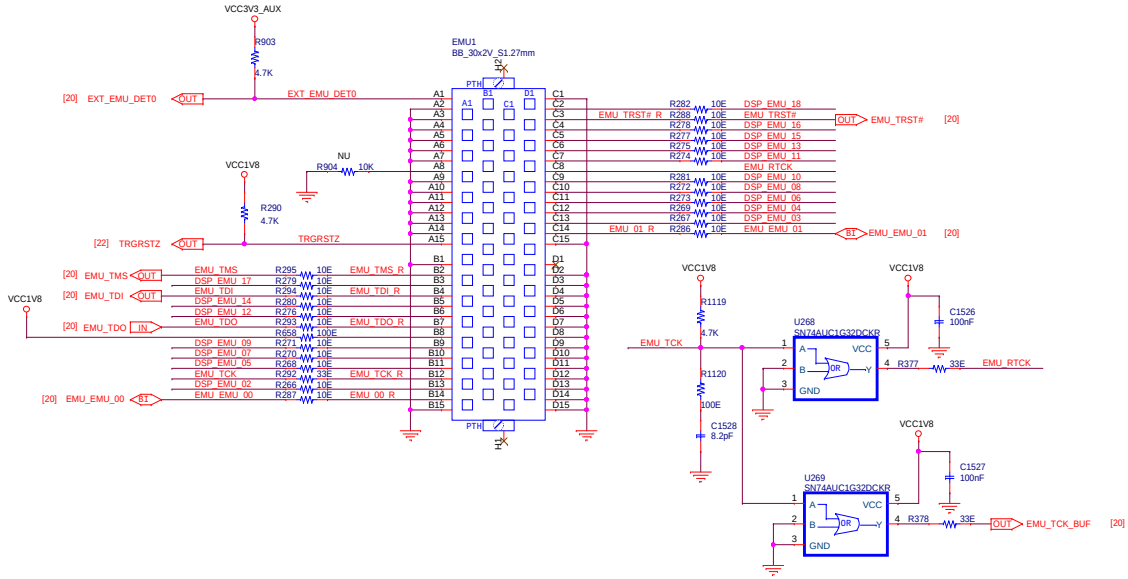
NAND FLASH



C6657 - JTAG & EMU



TI-60 Header



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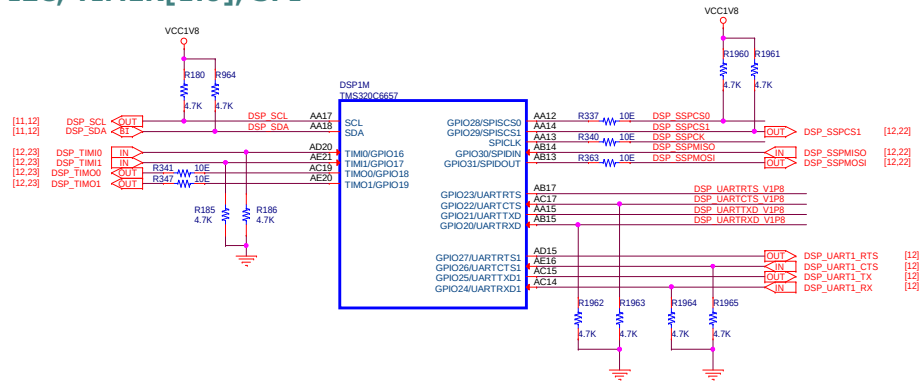
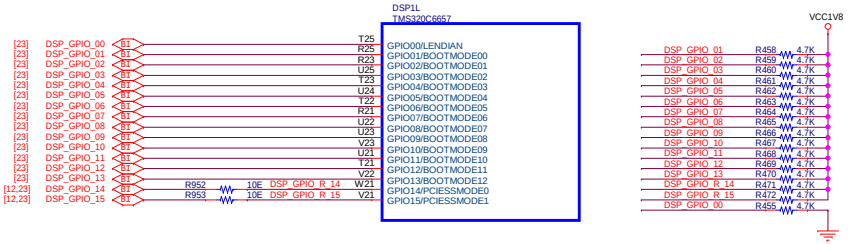
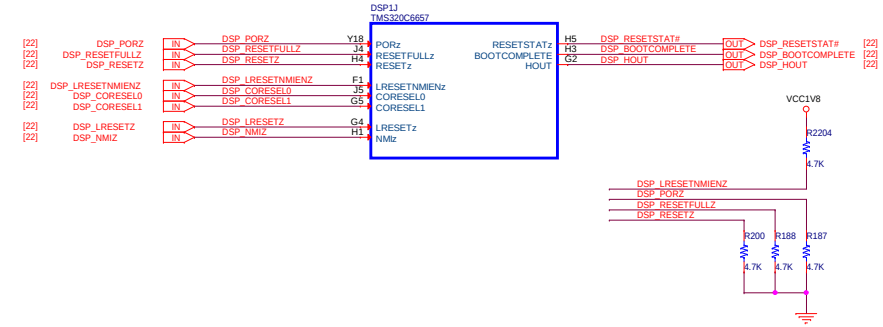
I2C, TIMER[1:0], SPI



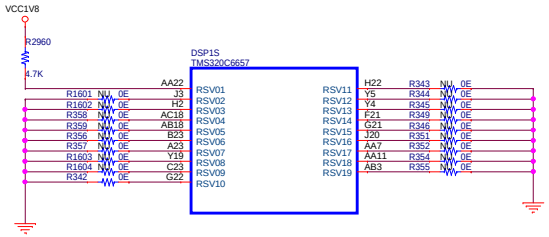
GPIO



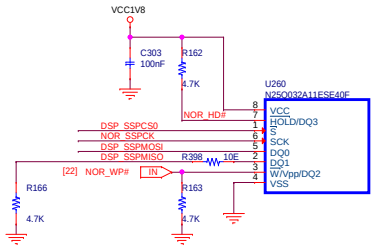
Reset Control



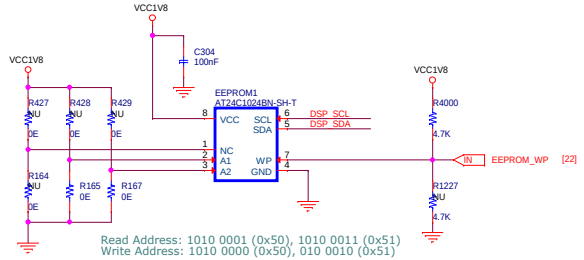
Reserved

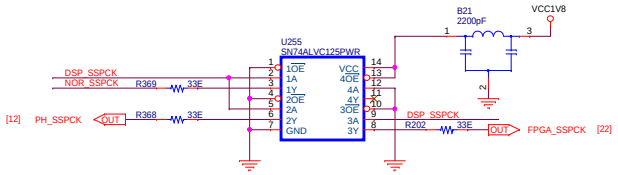


32Mb SPI NOR Flash

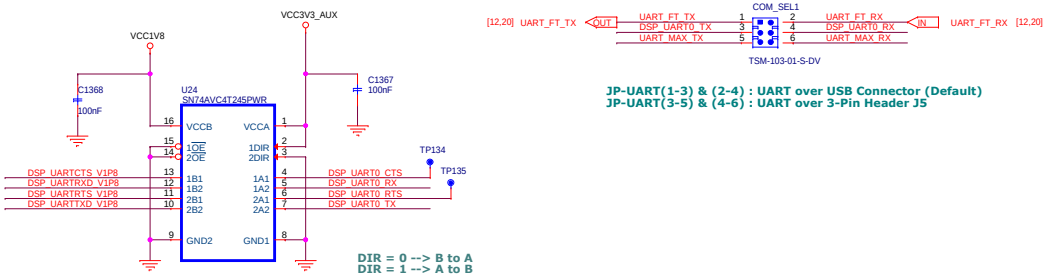


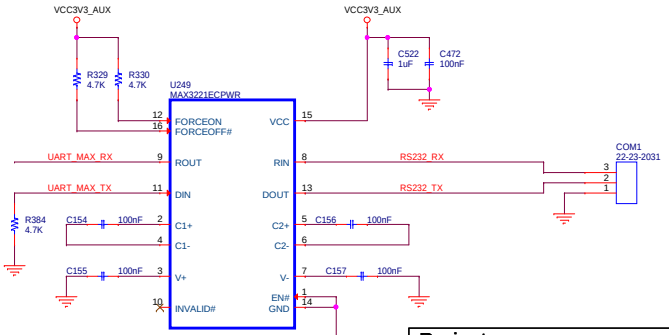
1Mb I2C EEPROM





UART to RS232





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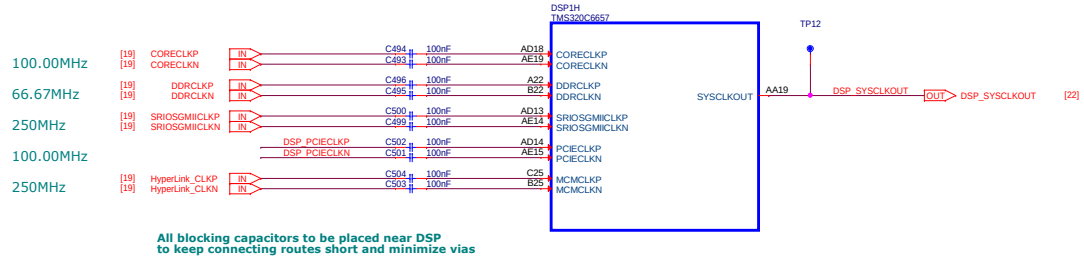
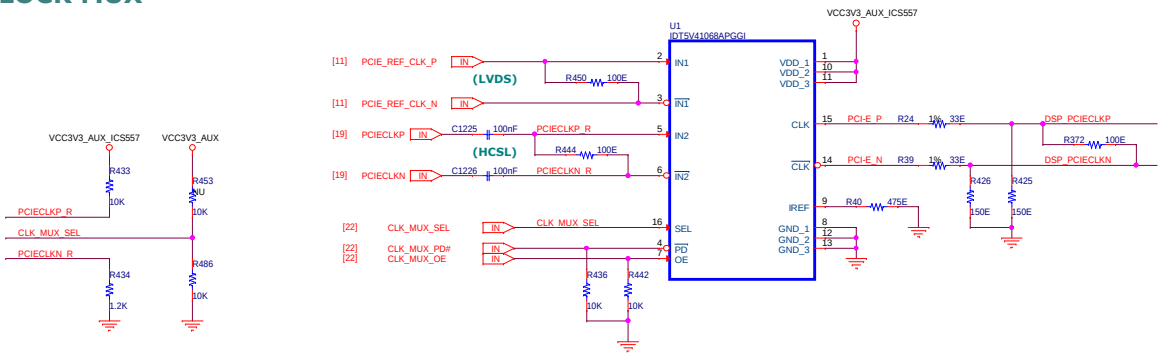
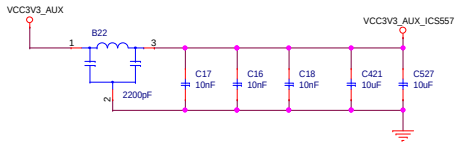
DSP CLOCK



All blocking capacitors to be placed near DSP
to keep connecting routes short and minimize vias

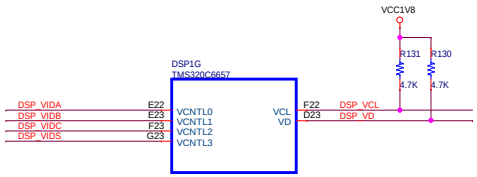
PCI CLOCK MUX

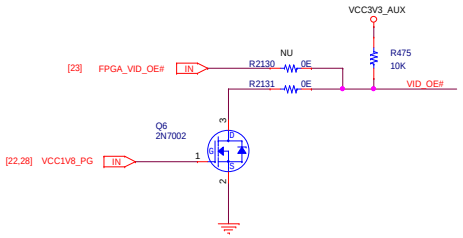


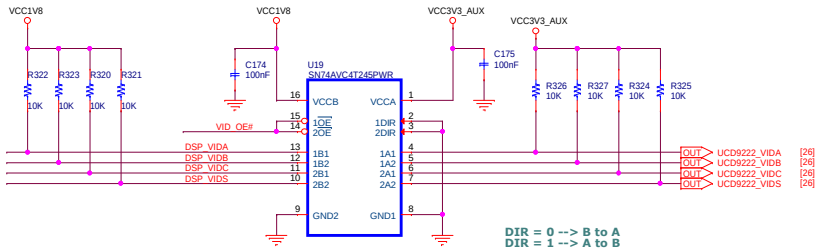


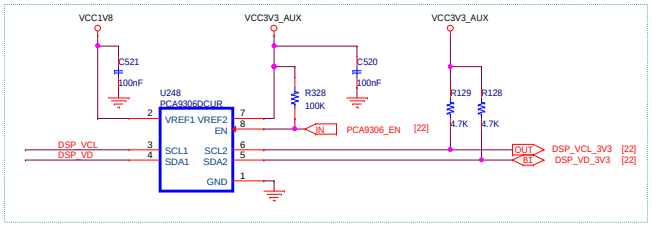
SEL	I/p PAIR SEL
LOW	IN2/IN2#
HIGH	IN1/IN1#

SMART REFLEX









Reserved for future use
Not supported at this time

Project TMDSEVM6657	Designed for TI by eInfochips	
Title DSP-CLOCK & SMART REFLEX		
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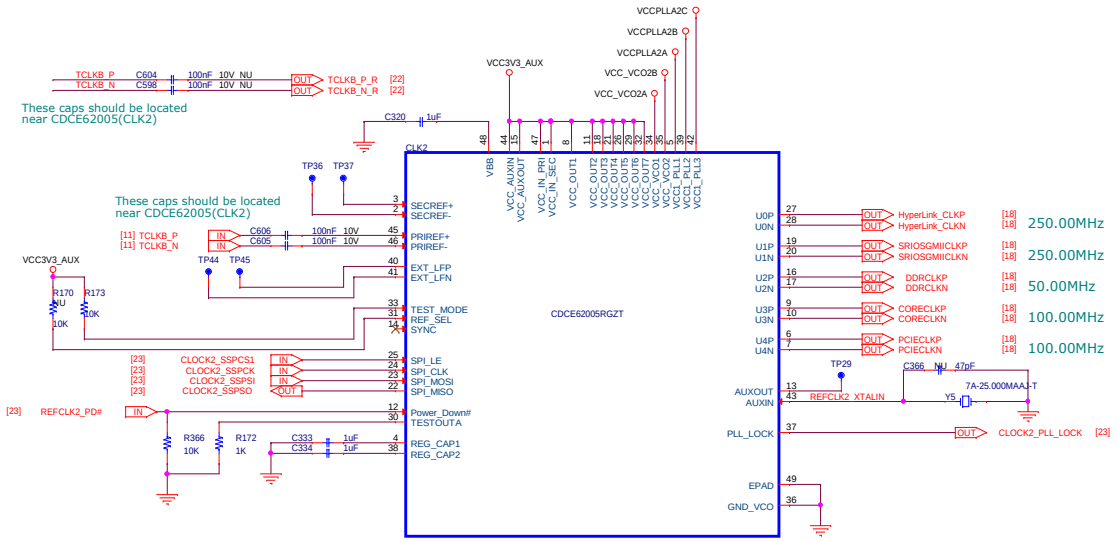
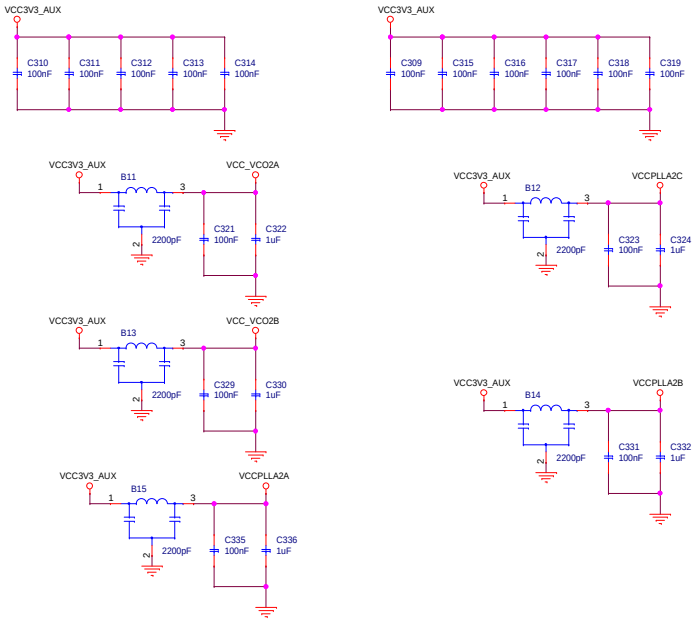
CLOCK GEN2





Project TMDSEVM6657	Designed for TI by eInfochips	
Title CLOCK GENRATION	Texas Instruments / eInfochips The Solutions People	
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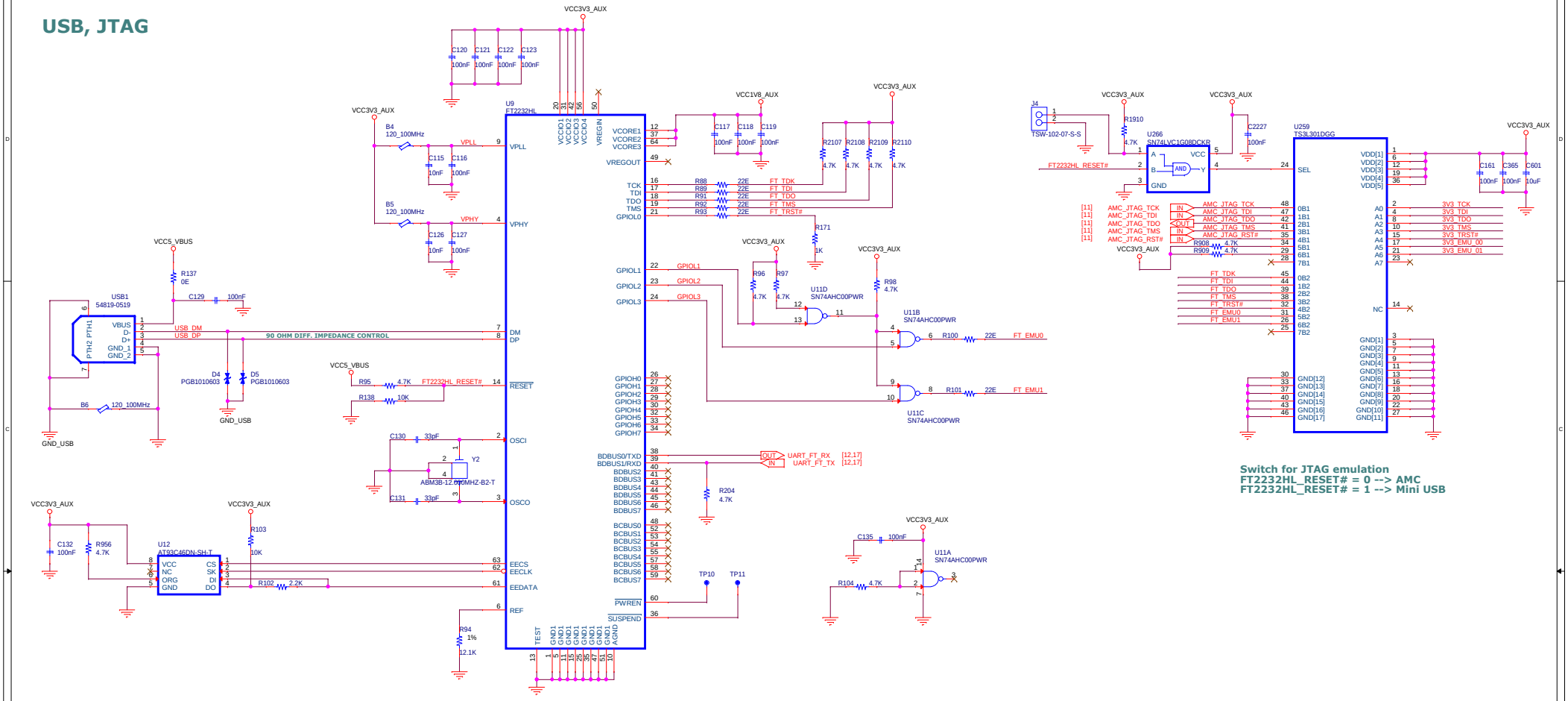
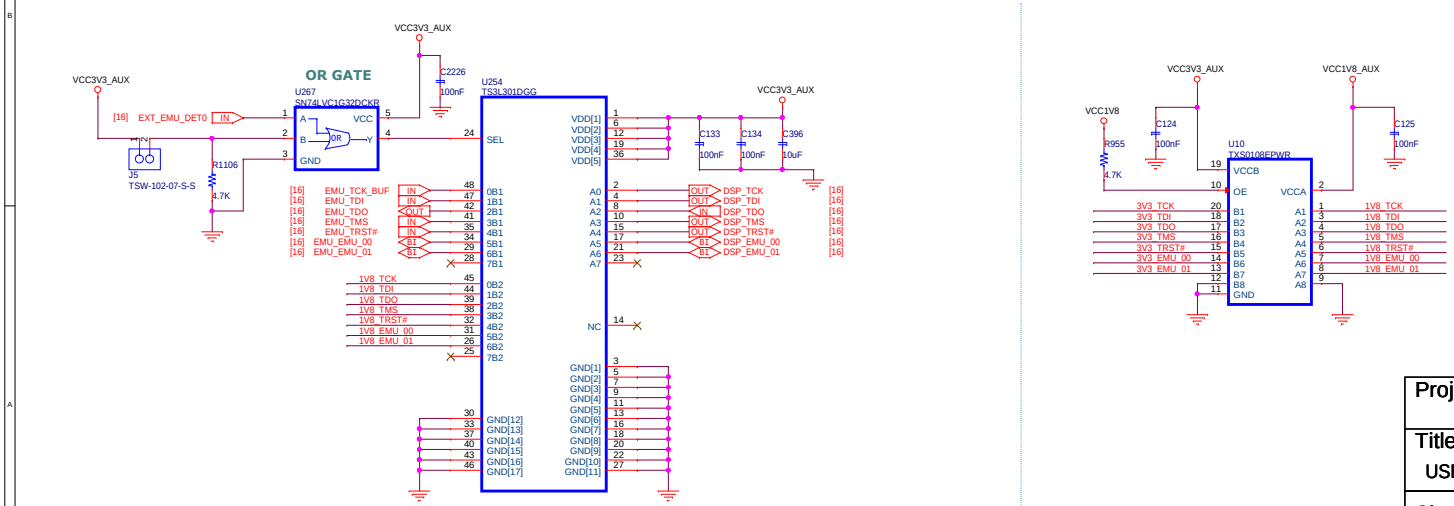
USB, JTAG





Project TMDSEVM6657	Designed for TI by eInfochips	
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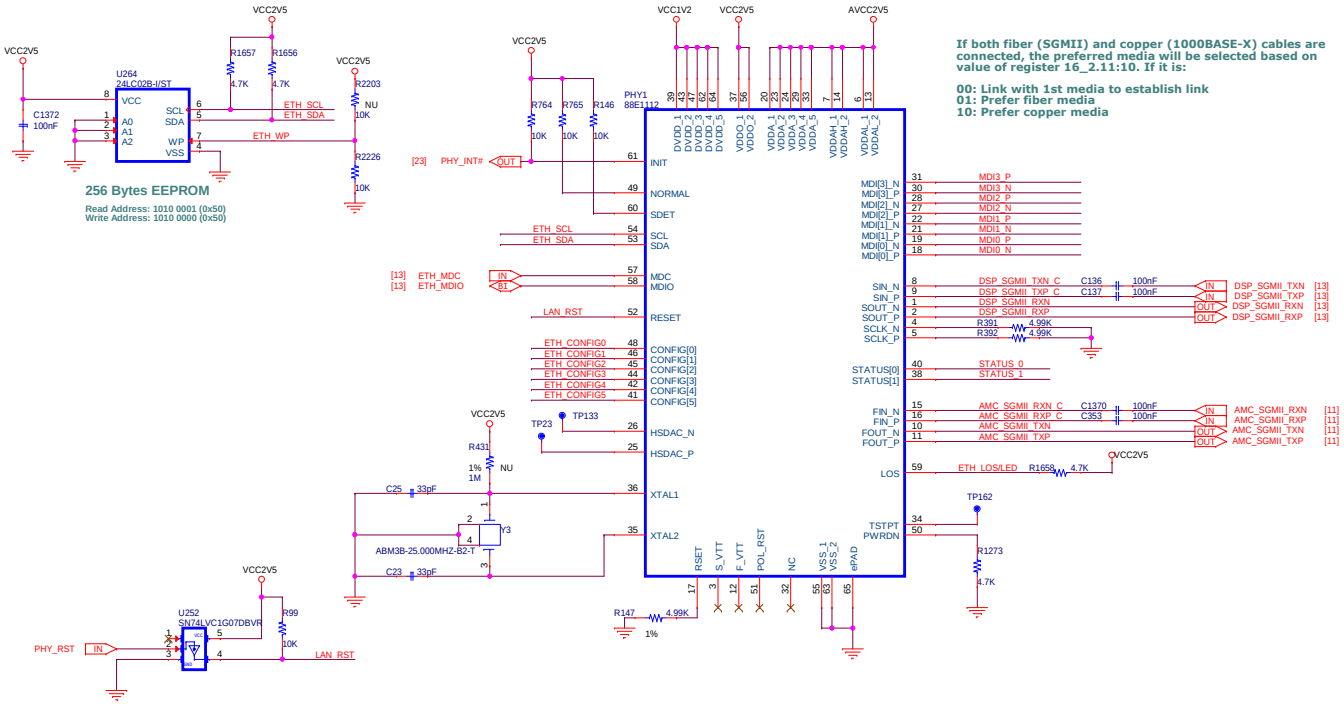
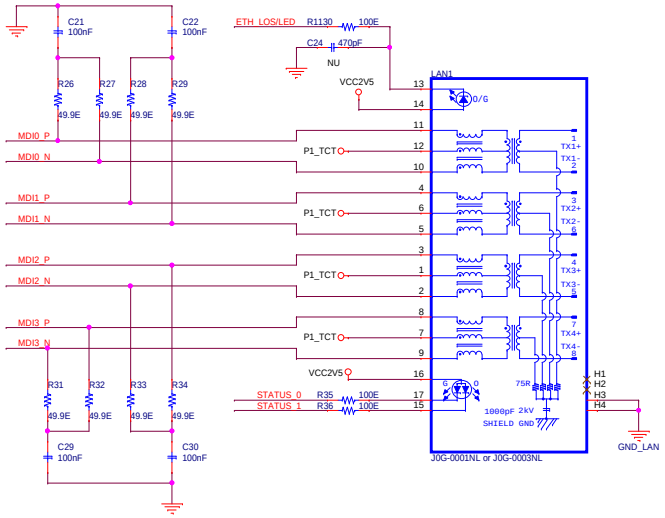
ETHERNET PHY

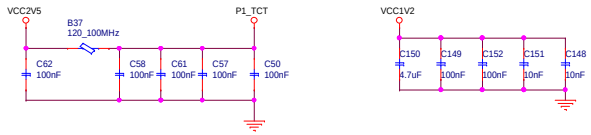


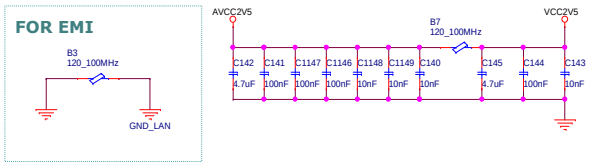
ETHERNET JACK

LED (Colour)	Link	No Link
LOS (Orange/Green)	ON	OFF



LED (Colour)	1Gbps		100Mbps		10Mbps	
	Activity	No Activity	Activity	No Activity	Activity	No Activity
Status 0 (Green)	BLINK	SOLID ON	BLINK	SOLID ON	OFF	OFF
Status 1 (Orange)	OFF	OFF	BLINK	SOLID ON	BLINK	SOLID ON





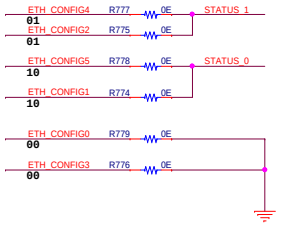
Pin to Configuration Bit Mapping

PIN	BIT[1]	BIT[0]
CONFIG0	PHYADR[1]	PHYADR[0]
CONFIG1	PHYADR[3]	PHYADR[2]
CONFIG2	SGMII_CLK	PHYADR[4]
CONFIG3	SEL_TWSI	SEL_VTT
CONFIG4	EEPROM[1]	EEPROM[0]
CONFIG5	MODE[1]	MODE[0]

PIN	VALUE
VDD0	11
STATUS[0]	10
STATUS[1]	01
VSS	00

POL_RST	RESET=0	RESET=1
0	Reset	Normal
1 or Floating	Normal	Reset

PIN	VALUE	CONNECTION	INTERPRETATION
CONFIG0	00	VSS	PHY Address[1:0] is 00
CONFIG1	10	STATUS[0]	PHY Address[3:2] is 10
CONFIG2	01	STATUS[1]	SGMII_CLK not supplied; PHY Address[4] is 1
CONFIG3	00	VSS	MDC/MDIO mode; S_VTT & F_VTT int supplied
CONFIG4	01	STATUS[1]	Start reading from address 0
CONFIG5	10	STATUS[0]	SGMII MAC Int to Auto Media select (Cu/SGMII)



Project	TMDSEVM6657
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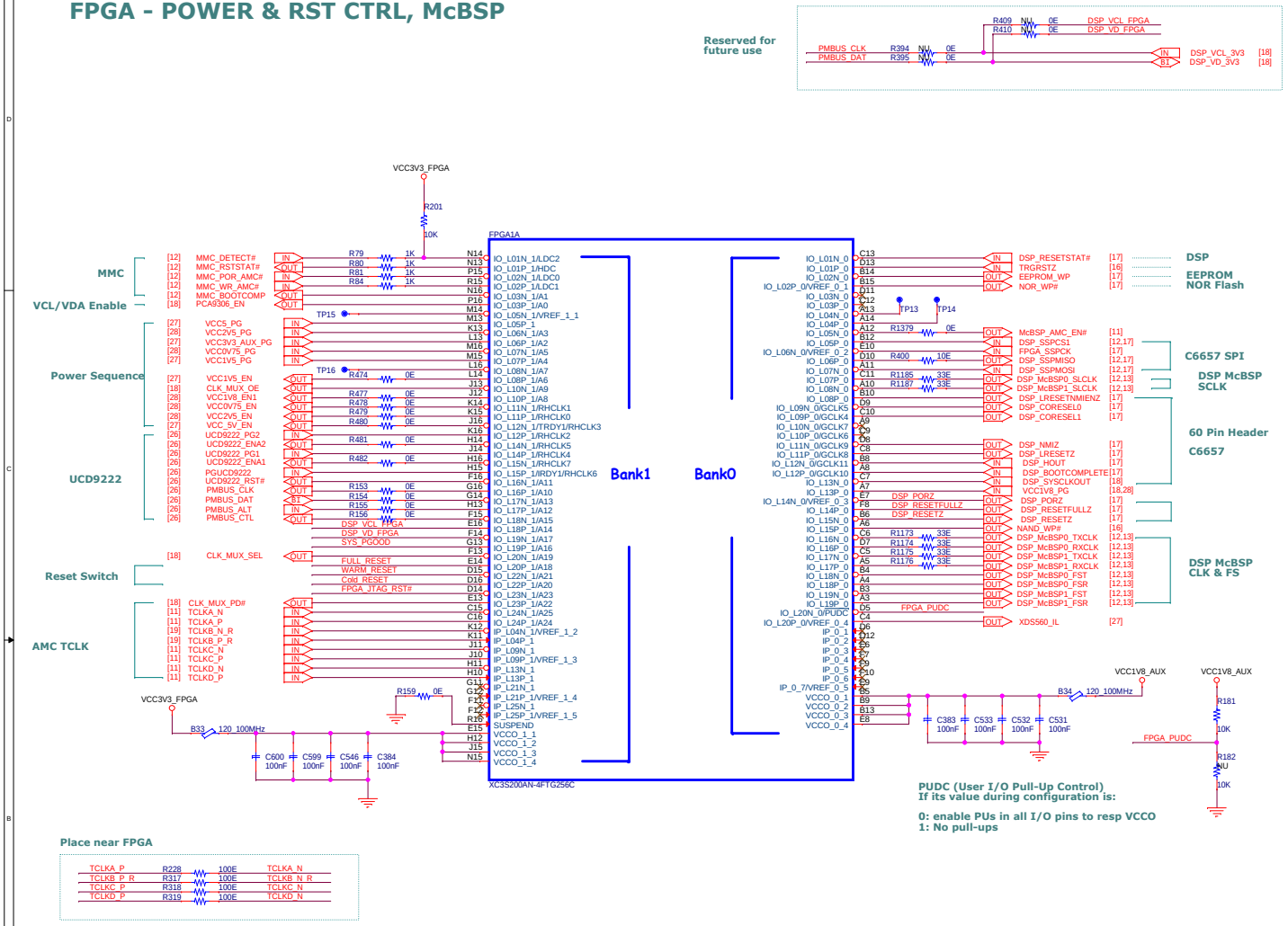
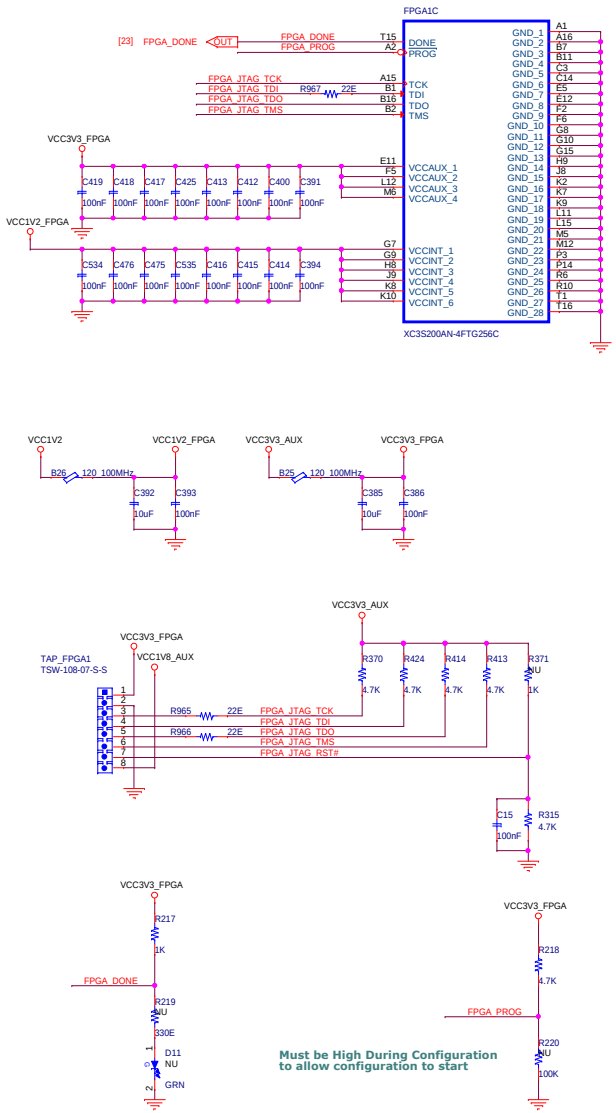
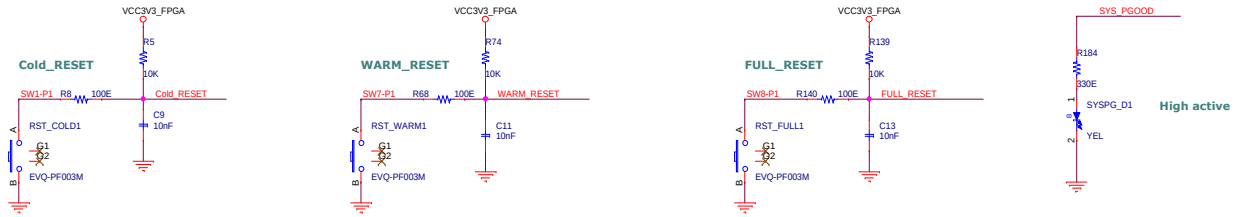
FPGA - POWER & RST CTRL, McBSP



FPGA - POWER, JTAG





Project	Designed for TI by eInfochips
TMDSEVM6657	Texas Instruments · eInfochips The Solutions People
Title: FPGA-POWER,RESET,McBSP	
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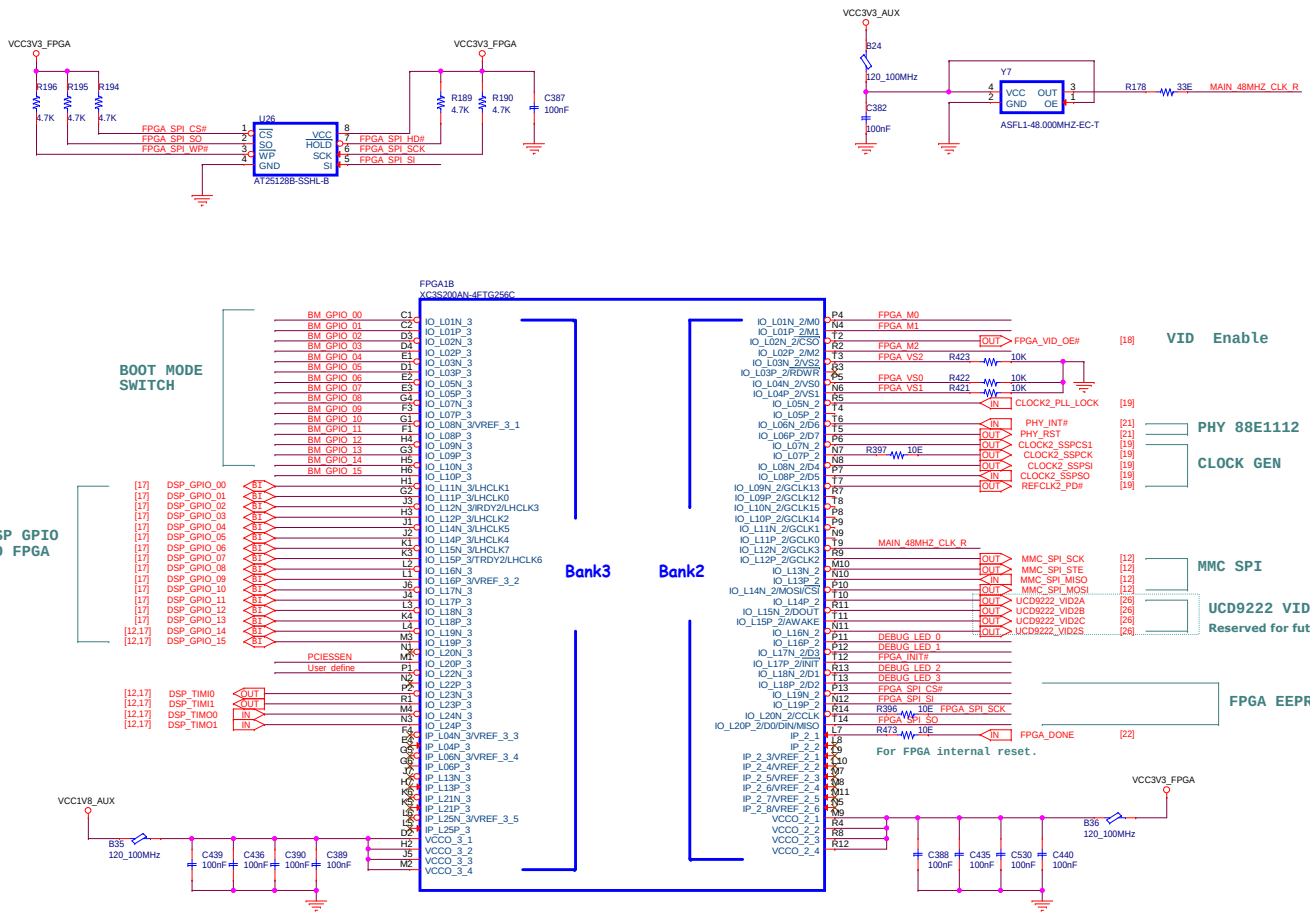
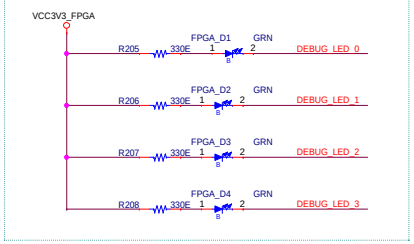
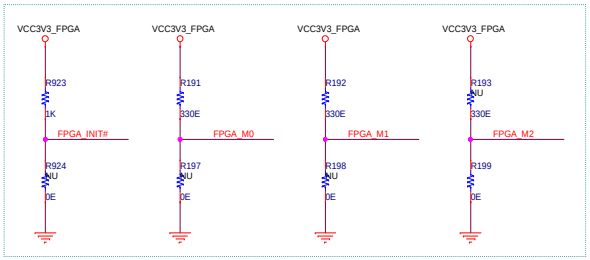
FPGA, BOOT MODE & SMART REFLEX

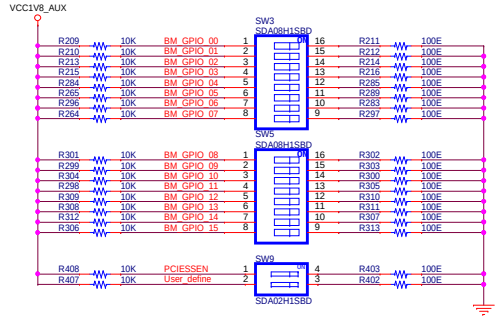


DEBUG_LED





BOOT STRAP CONFIGURATION



Boot Configuration

DIP Switch	DSP	BM_GPIO	Primary Function
BM_GPIO0	GPIO0	ENDIANESS	0 - Big Endian 1 - Little Endian
BM_GPIO[4:1]	GPIO[4:1]	BOOTMODE[3:0]	Boot Device
BM_GPIO[10:5]	GPIO[10:5]	BOOTMODE[9:4]	Boot Device Config
BM_GPIO[13:11]	GPIO[13:11]	BOOTMODE[12:10]	PLL Multiplier/I2C
BM_GPIO[15:14]	GPIO[15:14]	PCIESSMODE[1:0]	Endpt/RootComplex

Boot Device

BM_GPIO [4:1]	Boot Device	BM_GPIO [4:1]	Boot Device
0 0 0 0	Sleep/EMIF16	X 1 0 1	I2C Master
0 0 0 1	SRIO	0 1 0 1	I2C Slave
X 0 1 0	Ethernet	X 1 1 0	SPI
0 0 1 1	NAND	0 1 1 1	Hyperlink
0 1 0 0	PCIe	1 0 0 0	UART

Note: GPIO[10:5] bit definitions depend on the boot mode.

Boot PLL Settings

BM_GPIO [13:11]	Input Clock (in MHz)	BM_GPIO [13:11]	Input Clock (in MHz)
0 0 0	50.00	1 0 0	156.25
0 0 1	66.67	1 0 1	250.00
0 1 0	80.00	1 1 0	312.50
0 1 1	100.00	1 1 1	122.88

PCIe Mode Selection PCIESSMODE[1:0]

BM_GPIO [15:14]	PCIe Mode
0 0	End-point mode
0 1	Legacy End-point mode (support for legacy INTx)
1 0	Root complex mode
1 1	Reserved

PCIESSEN

BM_GPIO16	PCIe Status
0	PCIe module disabled
1	PCIe module enabled

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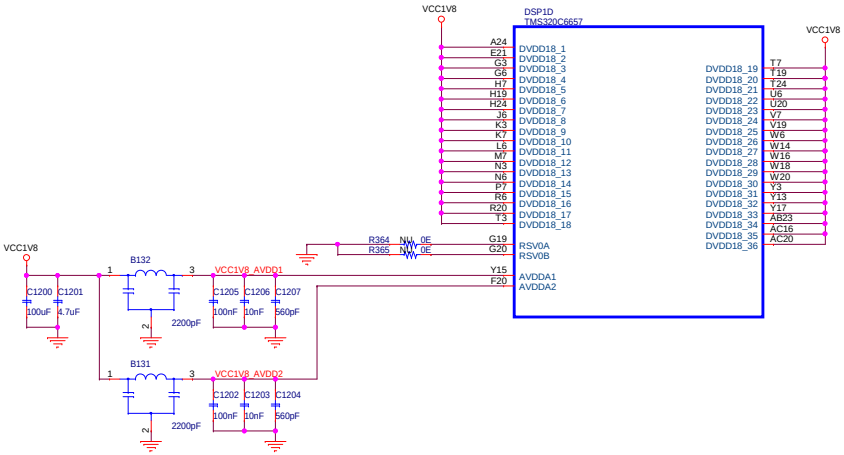
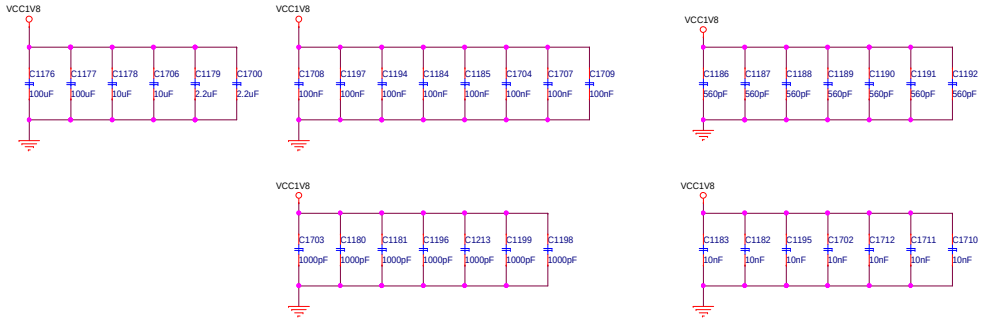
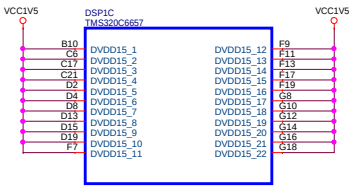
1.8V



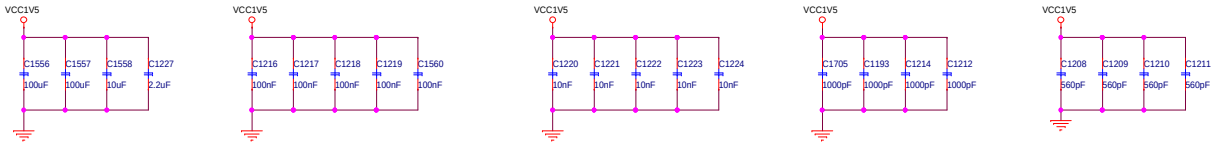
Place near to DSP



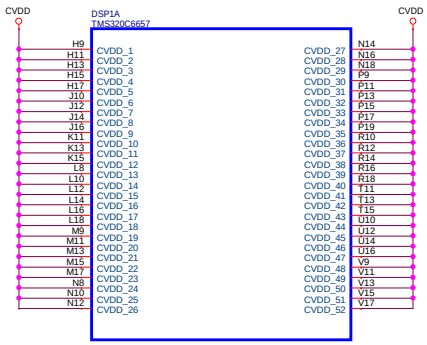
1.5V



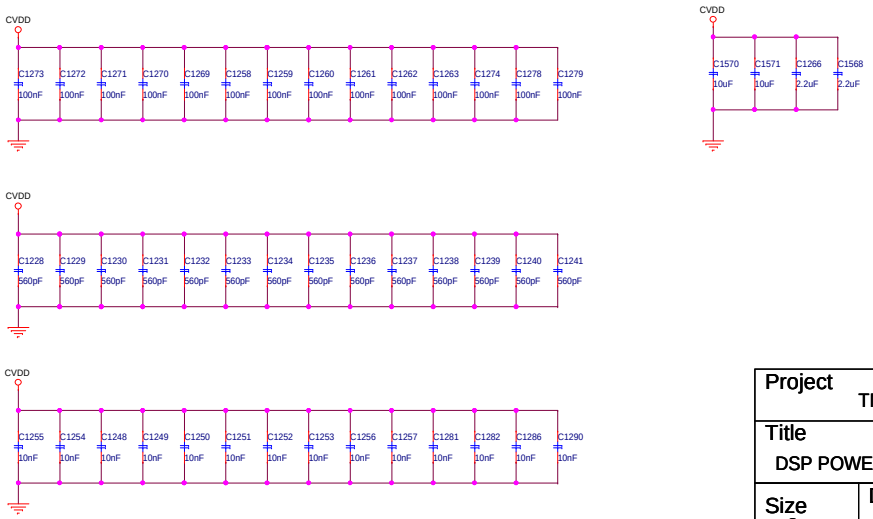
Place near to DSP



0.9V - 1.1V (SMART REFLEX)



Place near to DSP



Project TMDSEVM6657	Designed for TI by eInfochips	
Title DSP POWER 1	Texas Instruments / eInfochips The Solutions People	
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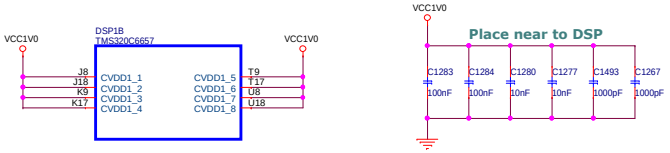
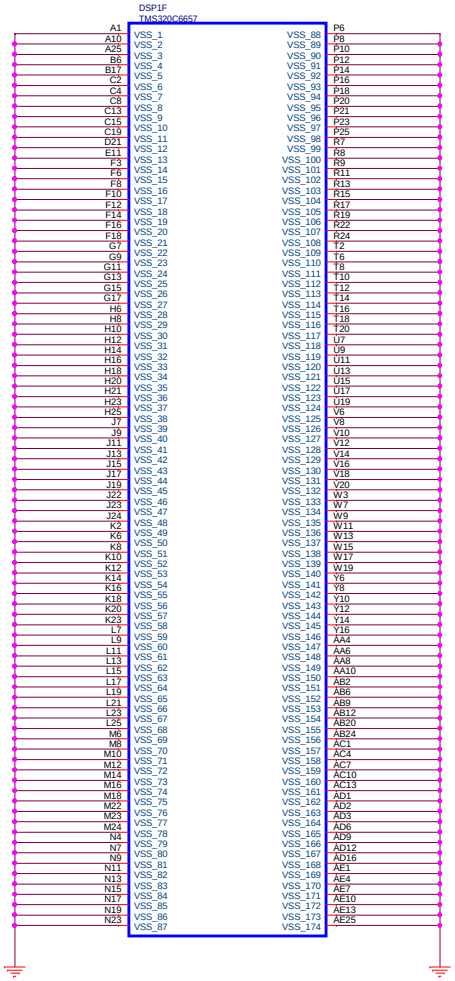
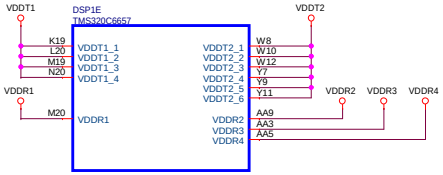
1.0V

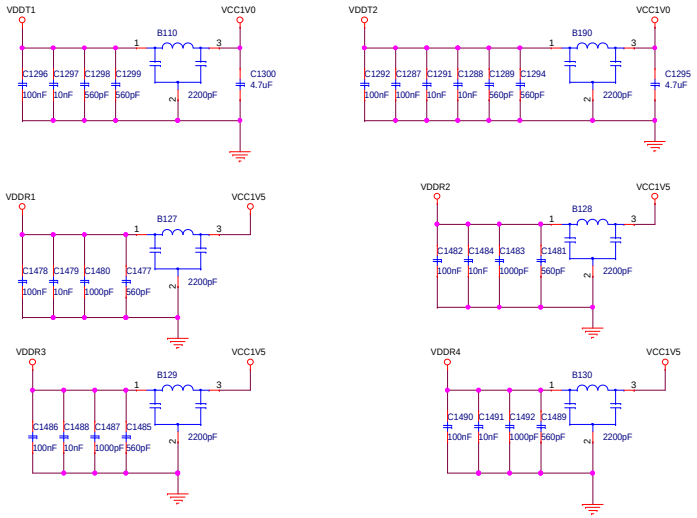


GROUND



1.0V & 1.5V for SERDES





Project TMDSEVM6657	Designed for TI by eInfochips	
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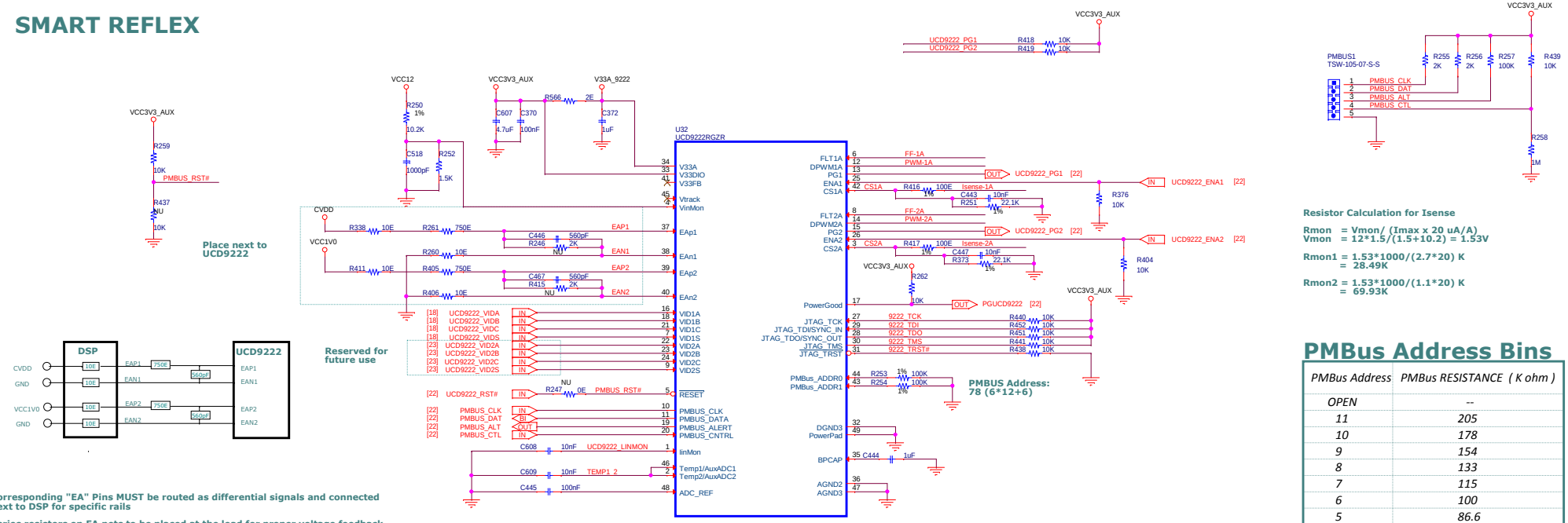
SMART REFLEX



Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

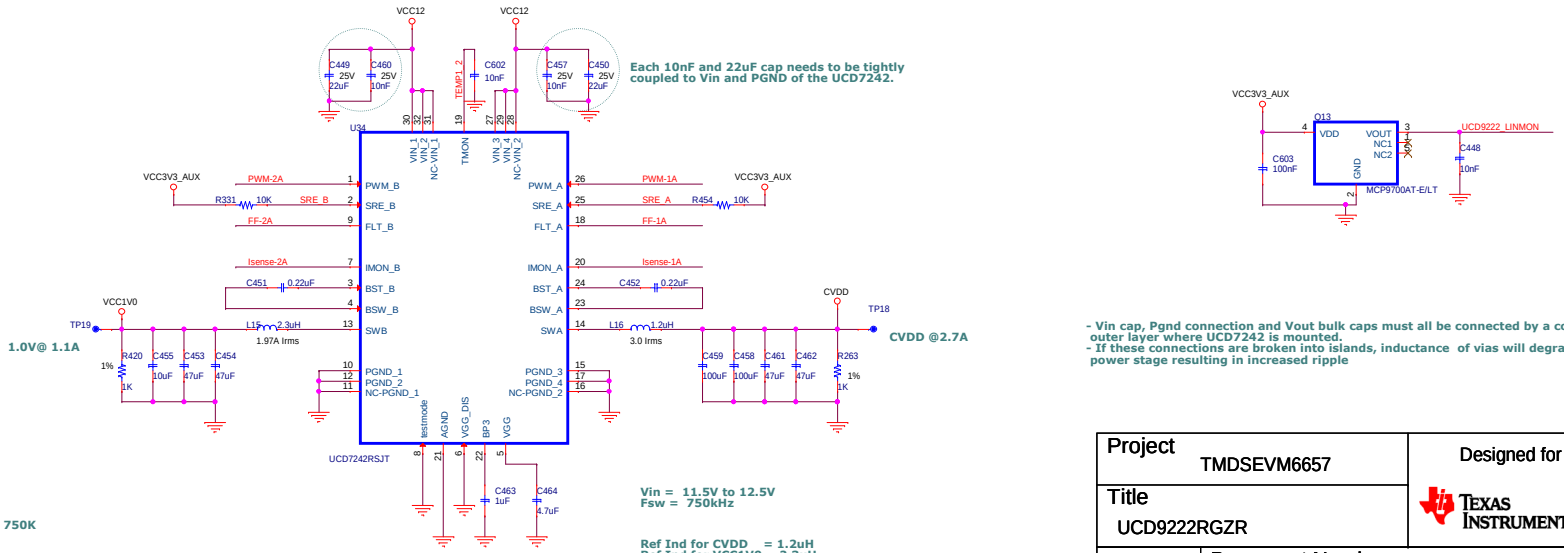
Provide min 25 thermal vias for IC

- C444 and C372 should be mounted adjacent to UCD9222 and connected without a via
- Components related to Isense pins should be located adjacent to UCD9222 with tightly coupled gnds.

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--

CVDD/CVDD1



$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \frac{D}{fs}$$

Inductor Calculation for CVDD

L= (12.5 - 1) / (2.7) * (1/12.5) / 750K
= 0.46 uH

Inductor Calculation for CVDD1

L= (12.5 - 1) / (1.1) * (1/12.5) / 750K
= 1.11 uH

- Vin cap, Pgnd connection and Vout bulk caps must all be connected by a continuous copper pour on outer layer where UCD7242 is mounted.
- If these connections are broken into islands, inductance of vias will degrade the performance of power stage resulting in increased ripple

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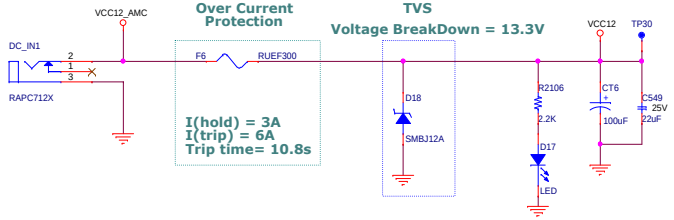
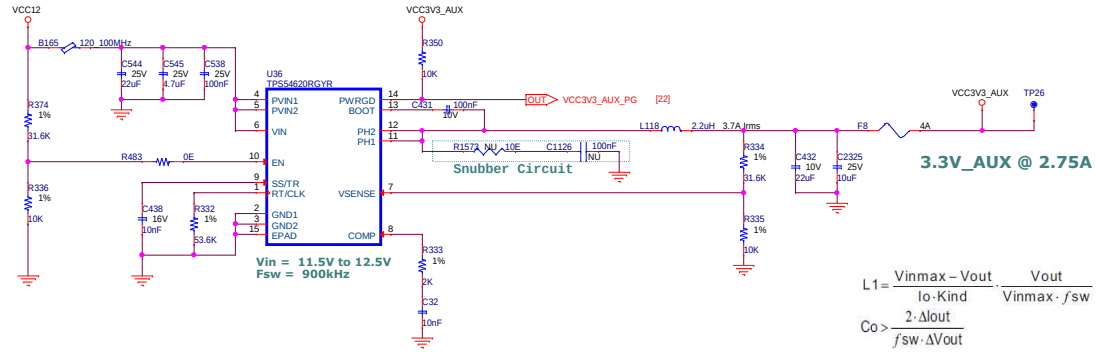
VCC12



12V to 3.3_AUX Generation



$$Rrt(k\Omega) = 48000 \cdot Fsw(kHz)^{-0.997} - 2$$

Rrt = 48000 x 900^(-0.997) - 2
= 53.6K

$$L1 = \frac{Vinmax - Vout}{Io \cdot Kind} \cdot \frac{Vout}{Vinmax \cdot fsw}$$

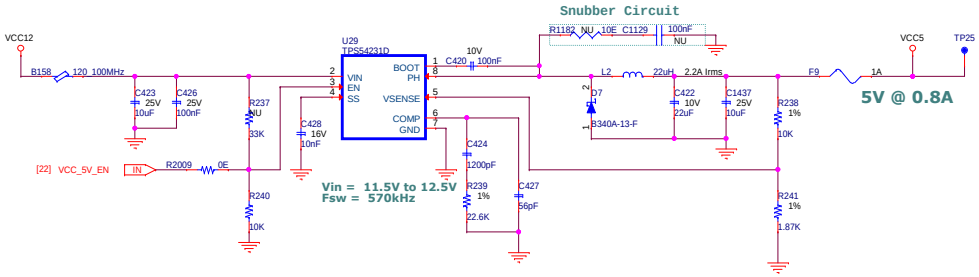
$$Co > \frac{2 \cdot \Delta Iout}{fsw \cdot \Delta Vout}$$

Ref Ind = 2.2uH
Ref Cap = 32uF

Lmin = ((12.5 - 3.3)/(3 * 0.3) * (3.3 / (12.5 * 900kHz))
= 2.96uH

Co_min = (2*1) / (900kHz*0.0825)
= 2.69uF

12V to 5V Generation



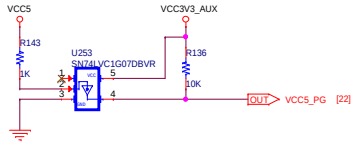
$$L_{MIN} = \frac{V_{OUT(MAX)} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW}}$$

$$C_{O_min} = 1/(2 \times \pi \times R_O \times F_{CO_max})$$

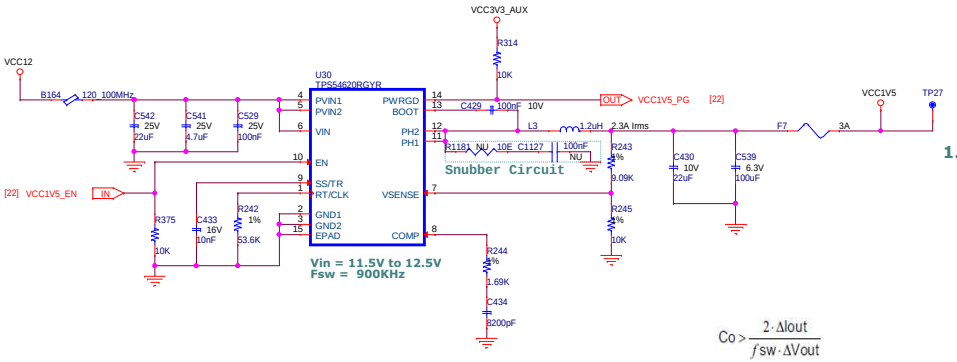
Ref Ind = 22uH
Ref Cap = 32uF

Lmin = ((12.5 - 5)/(0.8 * 0.3) * (5 / (12.5 * 570kHz))
= 21.87uH

Co_min = 1/(2 * 3.14 * (5/0.8)* 570kHz)
= 44.7nF



12V to 1.5V Generation



$$Rrt(k\Omega) = 48000 \cdot Fsw(kHz)^{-0.997} - 2$$

Rrt = 48000 x 900^(-0.997) - 2
= 53.6K

$$Co > \frac{2 \cdot \Delta Iout}{fsw \cdot \Delta Vout}$$

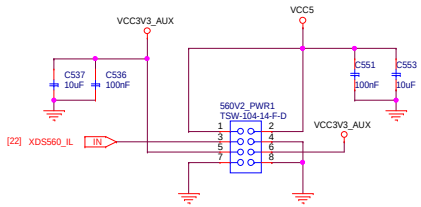
$$L1 = \frac{Vinmax - Vout}{Io \cdot Kind} \cdot \frac{Vout}{Vinmax \cdot fsw}$$

Ref Ind = 1.2uH
Ref Cap = 122uF

Lmin = ((12.5 - 1.5)/(2 * 0.3)) * (1.5 / (12.5*900kHz))
= 2.44uH

Co_min = (2*1)/(900kHz*0.075)
= 29.62uF

XDS560 v2 Mezzanine Power



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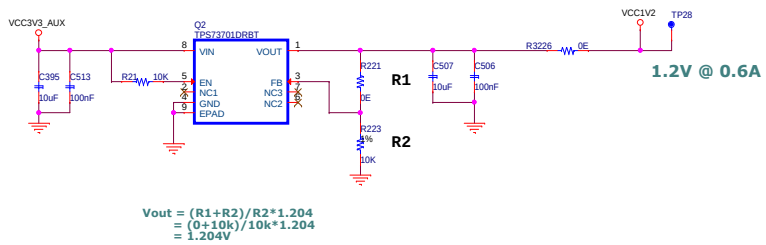
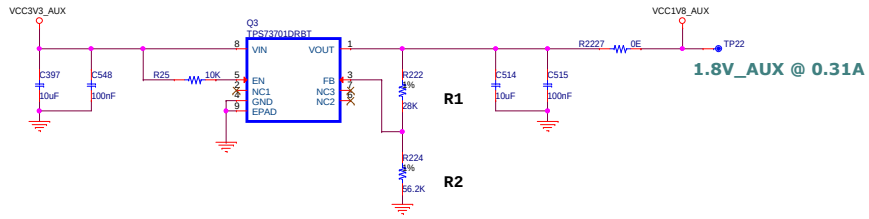
3.3V_AUX to 1.2V Generation



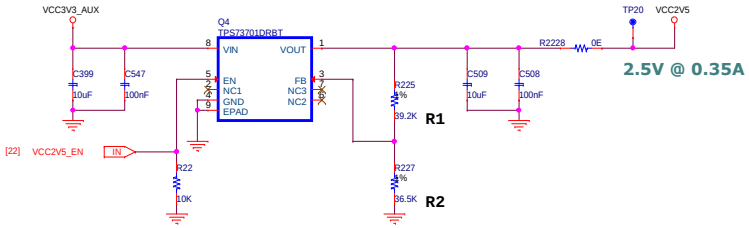
Vout = (R1+R2)/R2*1.204
= (0+10k)/10k*1.204
= 1.204V

3.3V_AUX to 1.8V_AUX Generation

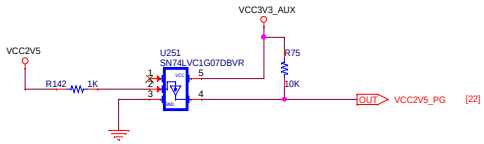


Vout = (R1+R2)/R2*1.204
= (28k+56.2k)/56.2k*1.204
= 1.804V

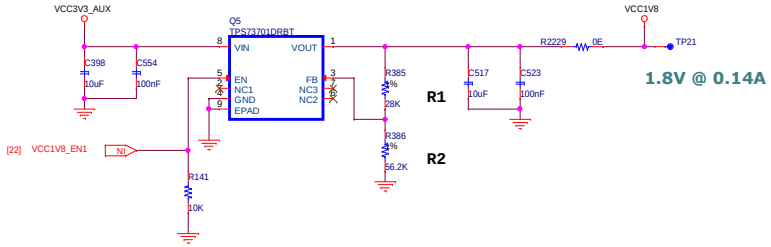
3.3V_AUX to 2.5V Generation



Vout = (R1+R2)/R2*1.204
= (39.2k+36.5k)/36.5k*1.204
= 2.50V

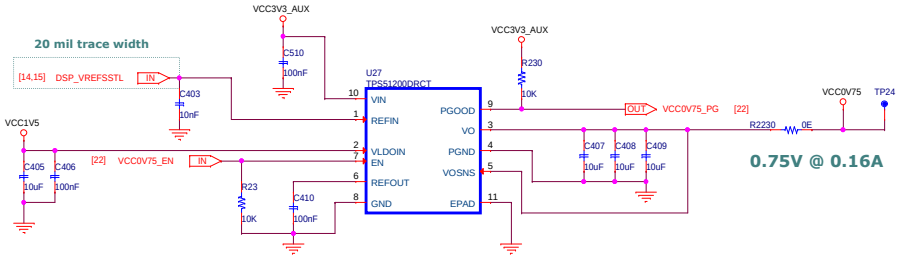


3.3V_AUX to 1.8V Generation

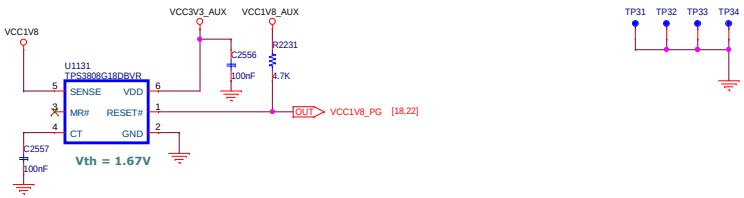


Vout = (R1+R2)/R2*1.204
= (28k+56.2k)/56.2k*1.204
= 1.804V

3.3V_AUX to 0.75V Generation



1.8V Superviser Circuit



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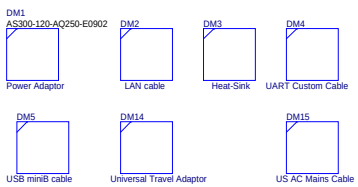
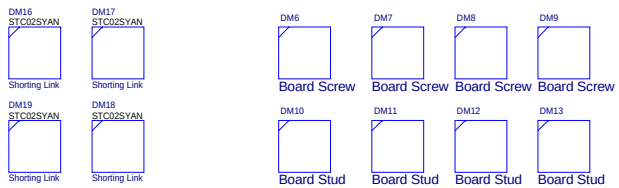
TMDSEVM6657 - REVISION HISTORY

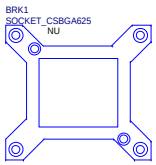
PCB REV.	SCH. REV.	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	0.6	- CLK3 removed - Series Termination removed from GPIO0 to GPIO13 lines	3-FEB-2012	eInfochips
	1.1	- D9 and D10 part changed with one with higher current capacity. - R134 changed to 1K from 4.7K - NU resistors R433 and R434 changed to 10K and 1.2K resp. They are to be mounted. - R12 and R17 replaced by 100nF caps C1225 and C1226 - R70 and R71 mounting status changed from NU to populated. - U6 (DDR3 ECC chip) made NU. - DDR3 Clock frequency from Clock Gen changed to 50 MHz (software change only).	20-MAR-2012	eInfochips
2.0	0.1	- Clock buffer U1132 removed. 2 OR gates (U268, U269) and the corresponding circuitry to buffer EMU_TCK added. - 4 Test Points for Gnd added. - ETH_SCK net renamed to ETH_SDA - SIGDETunconnected with LOS; its directly pulled high. R145 and R146 removed - SYSPG_D1 LED changed to Yellow colour from Green	02-APR-2012	eInfochips
	0.2	- 10 nF capacitors (C457 and C460) added on VCC12 input rail of U34. - Capacitors on CVDD rail optimized from two 220uF, two 100uF and four 47uF to two 100uF and two 47uF. - Capacitors on VCC1V0 rail optimized from one 220uF, three 47uF and one 10uF to two 47uF and one 10uF. - An additional 22uF cap (C549) added on VCC12 input for U29. C426 changed from 10nF to 100nF. - R183 changed to 1K from 4.7K. - SIGDET connected to VCC2V5 using R146. - R1273 changed to 4.7K from 10K.	02-MAY-2012	eInfochips
	0.3	- L15 and L16 changed to 2.3uH and 1.2uH respectively - R251 and R373 changed to 22.1K - C549 moved before B158 on 12V plane - C2325 changed from 100nF to 10uF - R2203 made NU and R2226 to be mounted	07-MAY-2012	eInfochips
	0.4	- NOR Flash density label corrected to 32 Mb from 16MB.	20-JUL-2012	eInfochips
	0.5	- DISCLAIMER Changed	26-JUL-2012	eInfochips
	0.6	- Asthetical Change Name swap between LVDS and HCSL on page 18	06-DEC-2012	eInfochips
	0.7	- Asthetical Change Note for DDR3 Slew-Rate setting corrected on page 14	29-JAN-2013	eInfochips
	0.8	- R82 and R83 changed to 10K - R85 and R957 made NU	22-FEB-2013	eInfochips
	0.9	- The Resistors R896,R67 and capacitor C555 are redundant components on EMU_TCK and can be NU from design. - Pull-up resister R1119 on EMU_TCK change from 10K to 4.7K	28-NOV-2013	eInfochips

Dummy Components

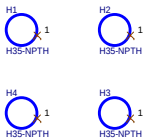




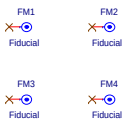
AMC Hole



Mounting Holes



On Board Fiducials



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