

C6472EVM Schematics

SCHEMATIC PAGE DESCRIPTION :

- 01 : COVER SHEET
- 02 : SYSTEM BLOCK DIAGRAM
- 03 : DSP - CLOCK, CONFIGURATION, I2C-UART BRIDGE
- 04 : JTAG EMULATION (ON BOARD / EXTERNAL HEADER)
- 05 : DDR2 INTERFACE
- 06 : GIG ETHERNET INTERFACE_1
- 07 : GIG ETHERNET INTERFACE_2
- 08 : TSIP, SRIO INTERFACE, MMC, AMC CONNECTOR
- 09 : HPI INTERFACE, DSP POWER
- 10 : FPGA - NAND FLASH INTERFACE
- 11 : BOARD POWER SUPPLY & RESET CIRCUITRY
- 12 : REVISION HISTORY & DUMMY PARTS

I2C ADDRESS TABLE :

REF DES	DESCRIPTION	7 BIT ADDRESS
U19	I2C EEPROM	0x50
U20	I2C - UART BRIDGE	0x4D
U9	FPGA	TBD

PCB Mechanical Details :

1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. PCB MATERIAL: FR4
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

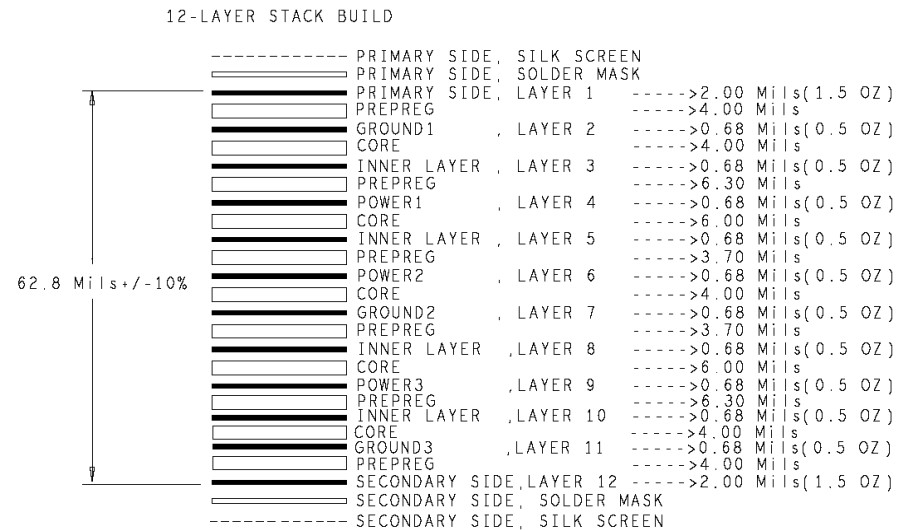
NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.

MAJOR REVISION HISTORY :

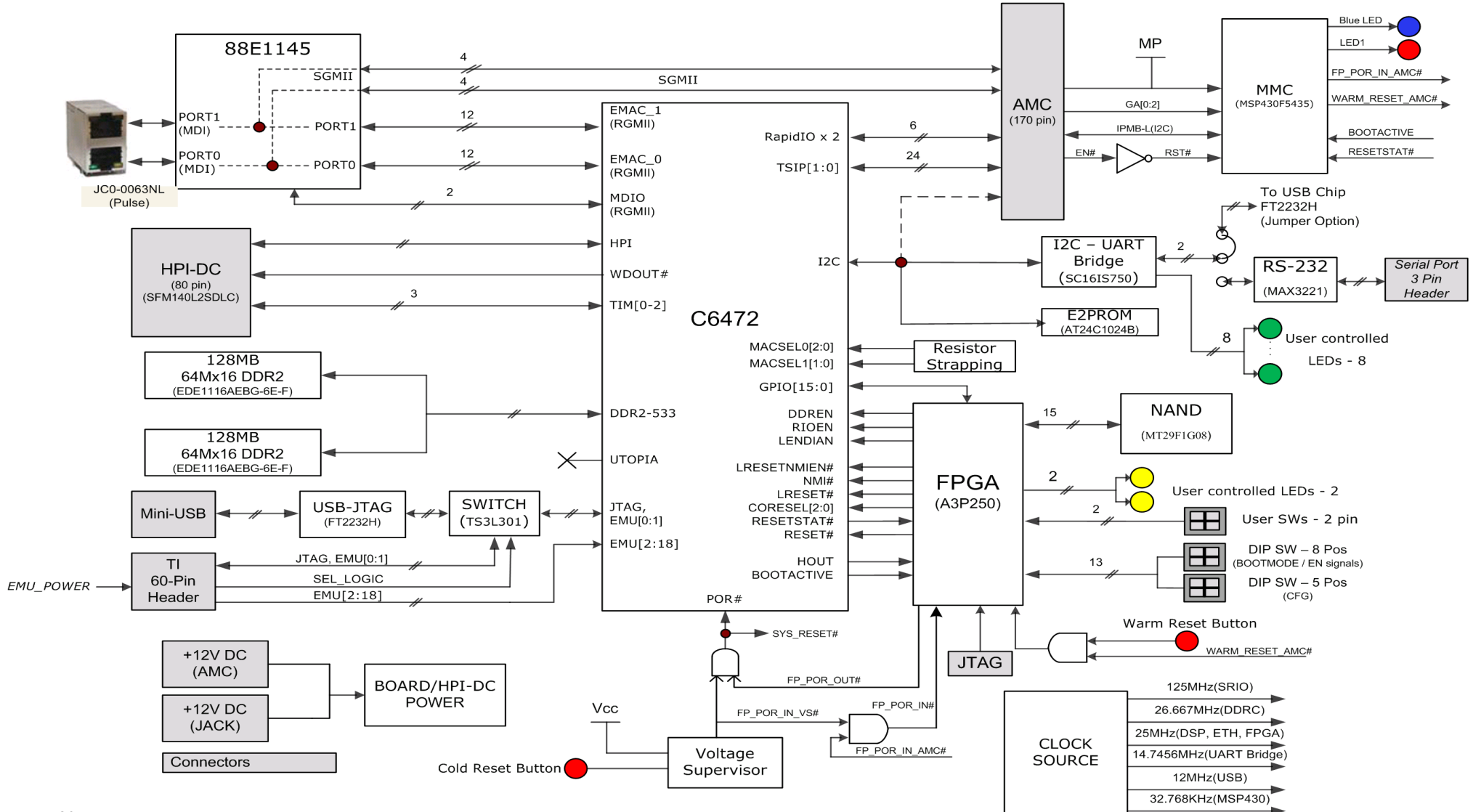
PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	1.0	First Build (Alpha)	06-AUGUST-2009
	1.1	First Build (Beta)	09-SEPTEMBER-2009
2.0	2.1	Second Build (AMC/TSIP/I2C chagnes)	24-SEPTEMBER-2009
3.0	3.2	SGMII feature addition proto Build	27-OCTOBER-2009
4.0	4.2	SGMII Production Build (PHY configuration changes)	22-JANUARY-2010
5.0	5.3	IPMI and XDS560v2 support added	12-JULY-2010
6.0	6.0	TCLKC/D used for Frame Sync	04-SEPTEMBER-2010
	6.1	D18 par# changed	19-NOVEMBER-2010

PCB LAYER STACK-UP DETAILS :



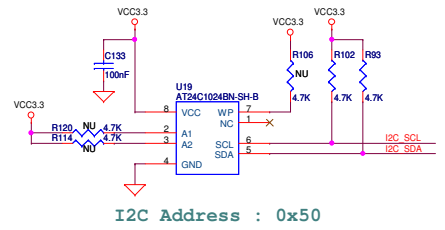
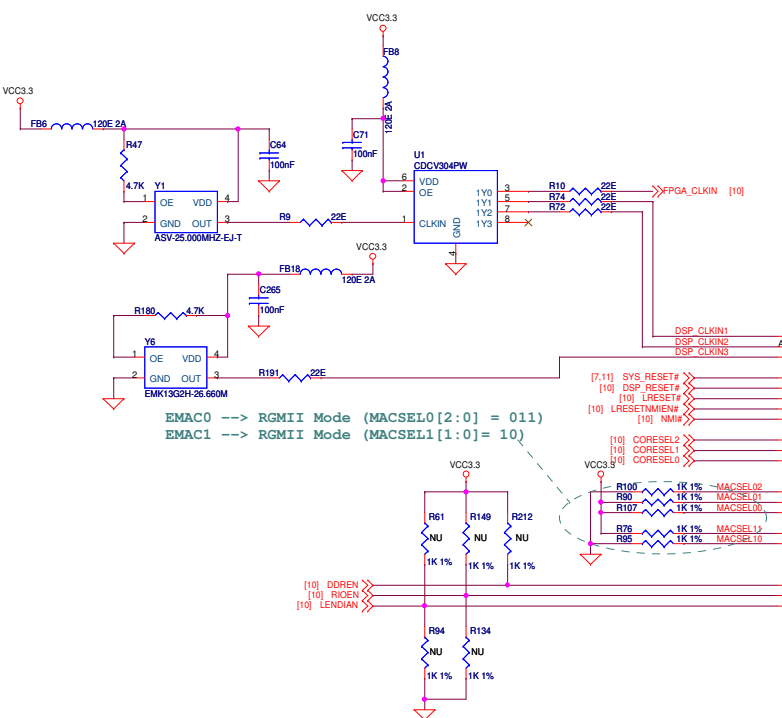
Project TI_C6472EVM		Designed for TI by elfnchips	
Title Cover Sheet			
Size C	Document Number 16-00065-06	Rev 6.1	
Date: Tuesday, May 10, 2011		Sheet 1 of 12	

BLOCK DIAGRAM



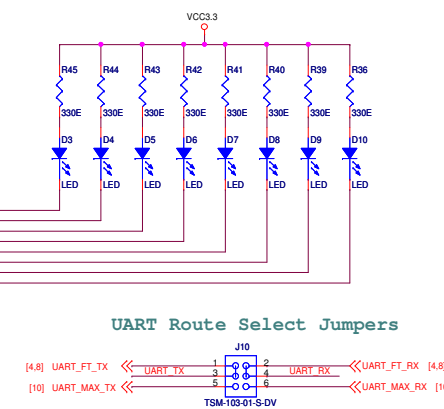
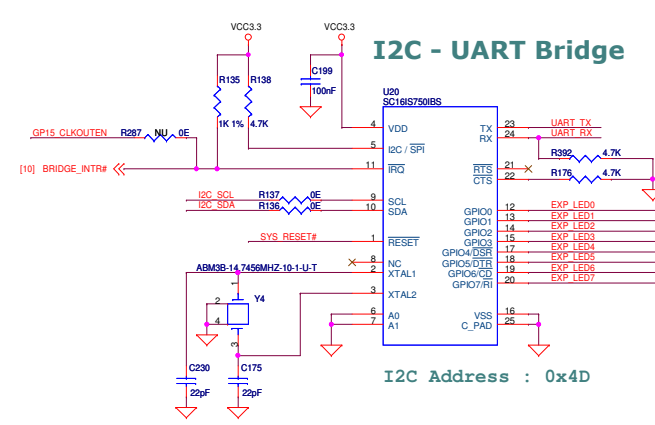
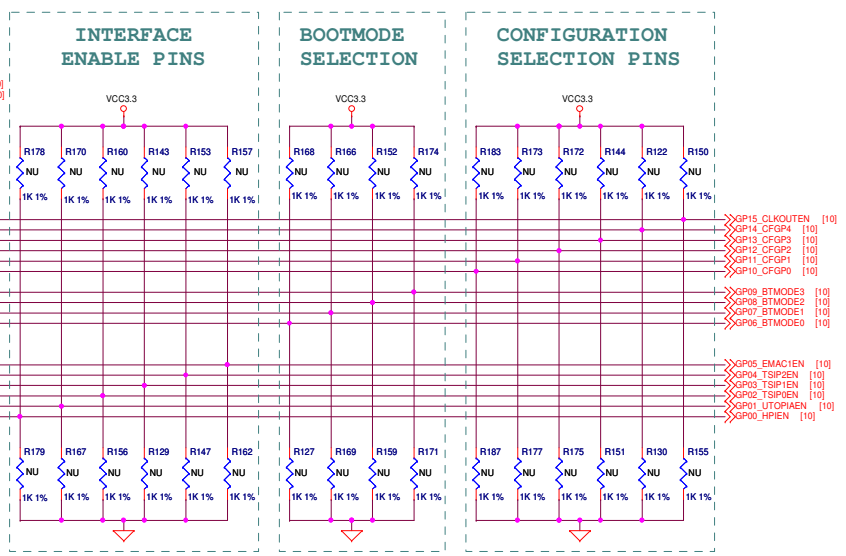
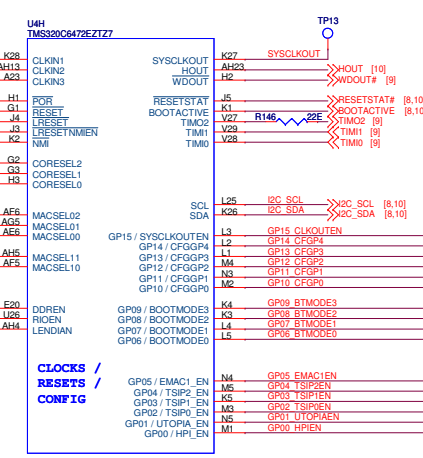
- Notes:
- 1) GPIO[15:0] are multiplexed with configuration pins
 - 2) RAM expandable to 512MB(128Mx16) DDR2-533

Project TI_C6472EVM		Designed for TI by elfnchips	
Title System Block Diagram			
Size C	Document Number 16-00065-06	Rev 6.1	
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FPGA to drive GP[15:00], DDREN, RIOEN & LENDIAN signals at reset

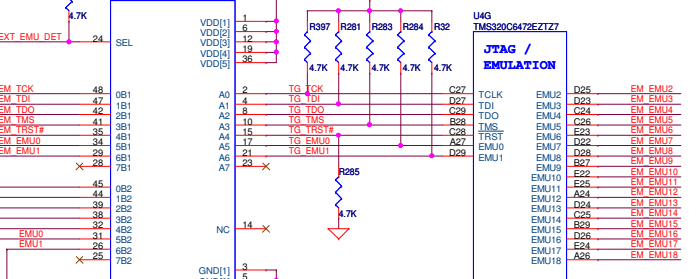
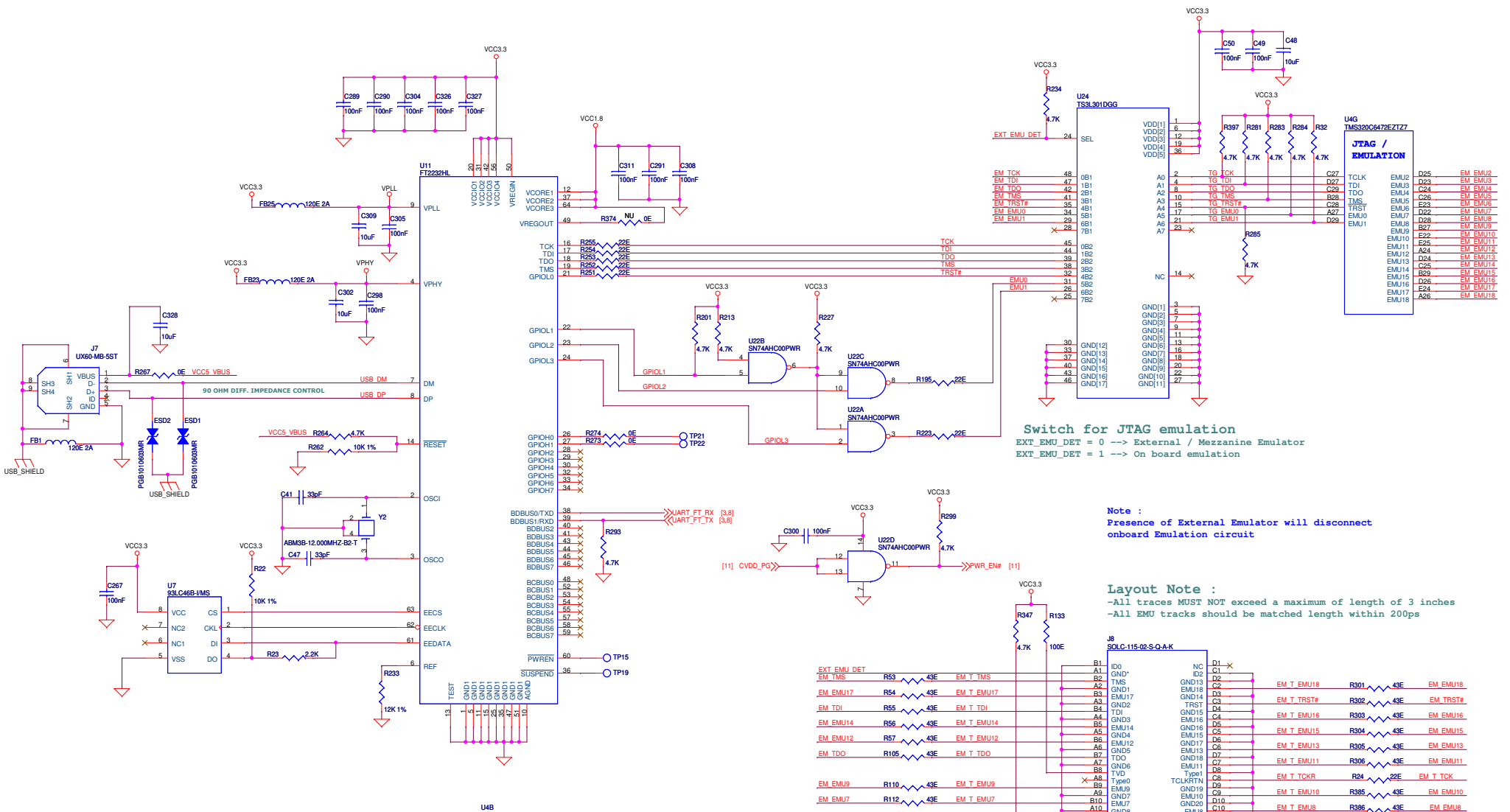
I2C Address : 0x50



J10.3 to J10.1 & J10.4 to J10.2: UART over USB Connector (Default)
 J10.3 to J10.5 & J10.4 to J10.6: UART over 3-Pin Header J4

BOOTMODE [3:0]	DESCRIPTION
0000 (0)	Immediate Boot
0001 (1)	Host (HPI) boot
0010 (2)	Master I2C boot (address : 50H) -- Default
0011 (3)	Master I2C boot (address : 51H)
0100 (4)	Slave I2C boot
0101 (5) - 1000 (8)	UTOPIA boot
1001 (9)	EMAC0 boot
1010 (10)	EMAC1 boot
1011 (11) - 1110 (14)	RIO[1:4]
1111 (15)	Reserved

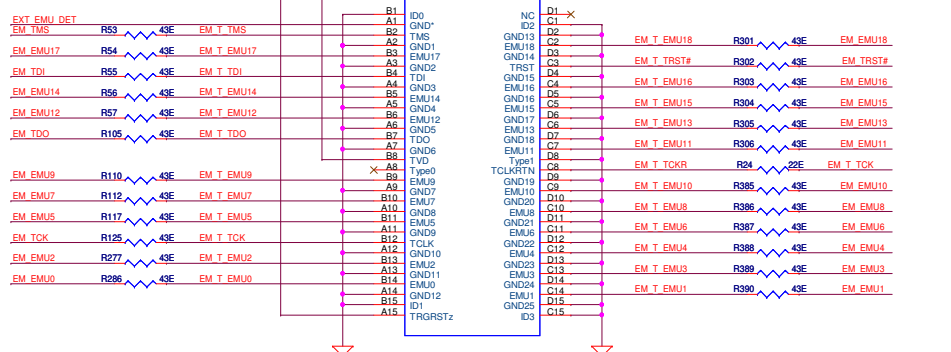
Project TI_C6472EVM		Designed for TI by elfnfochips	
Title DSP Configuration, UART Bridge			
Size C	Document Number 16-00065-06	Rev 6.1	
Date: Tuesday, May 10, 2011		Sheet 3 of 12	



Switch for JTAG emulation
 EXT_EMU_DET = 0 --> External / Mezzanine Emulator
 EXT_EMU_DET = 1 --> On board emulation

Note :
 Presence of External Emulator will disconnect onboard Emulation circuit

Layout Note :
 -All traces MUST NOT exceed a maximum of length of 3 inches
 -All EMU tracks should be matched length within 200ps



TI-60 Pin JTAG Connector for External/Mezzanine Emulator

U4F TMS320C647ZE2T27

(G) MI10 / RMI1[1:0] / SMII[1:0]

AG10	MRCLK0 / SRXCLK1	GMTCLK0 / REFCLK1 (SREFCLK1)	AG6
AE12	MRXEN0 / RMRXEN0 / SRXCLK0	MTXEN0 / RMTXEN0	AE11
AE12	MRXD00 / RMCRSVD1		
AE10	MRCS0 / RMCRSVD0		
AE8	MCCL0		
A13	MRXD07	MTXD07 / STXCLK0	AG11
AG7	MRXD08 / RMRXEN1	MTXD08 / RMTXEN1	AE10
AG7	MRXD05 / RMRXD11	MTXD05 / RMTXD11	AE7
AG8	MRXD04 / RMRXD10	MTXD04 / RMTXD10 / STXCLK1	AE9
A10	MRXD03 / SRXSYNC1	MTXD03 / STXSYNC1	AG8
A11	MRXD02 / SRXD1	MTXD02 / STXD1	AG5
A12	MRXD01 / RMRXD01 / SRXSYNC0	MTXD01 / RMTXD01 / STXSYNC0	AE8
A11	MRXD00 / RMRXD00 / SRXD0	MTXD00 / RMTXD00 / STXD0	AE7

(G) MI1 SMI

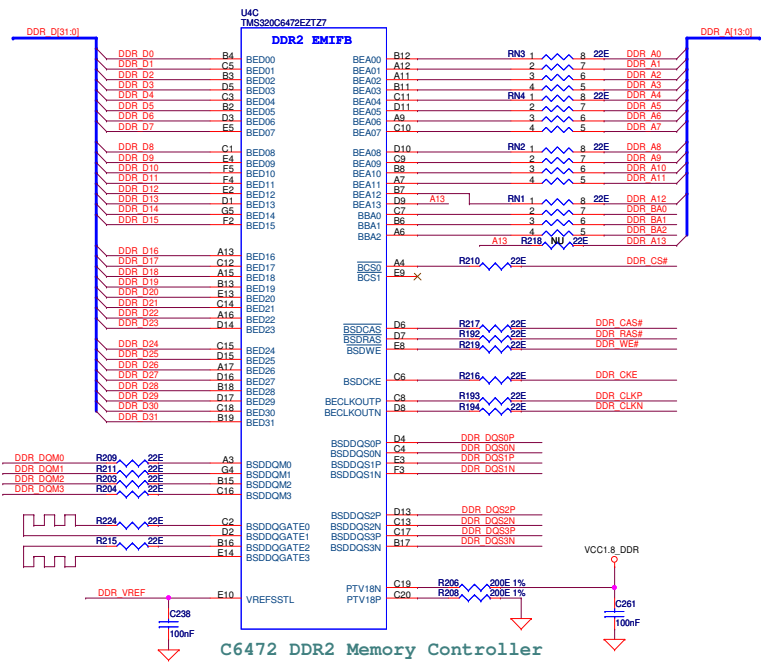
AG8	GMDCLK
AH19	GMDIC

U4B TMS320C647ZE2T27

UTOP1A

AE29	URCLK	UXCLK	J26
AE27	URENB	UXENB	AA25
AA25	URSOC	UXSOC	F29
J28	URCLAV	UXCLAV	JH27
Y25	URADDR4	UXADDR4	W25
Y26	URADDR3	UXADDR3	W26
Y27	URADDR2	UXADDR2	W27
Y28	URADDR1	UXADDR1	W28
Y29	URADDR0	UXADDR0	W29
AD26	URDATA15	UXDATA15	H29
AE29	URDATA14	UXDATA14	J27
AD27	URDATA13	UXDATA13	H28
AD28	URDATA12	UXDATA12	H29
AD29	URDATA11	UXDATA11	F28
AG25	URDATA10	UXDATA10	G27
AG26	URDATA9	UXDATA9	H26
AC27	URDATA8	UXDATA8	J25
AC28	URDATA7	UXDATA7	E29
AC29	URDATA6	UXDATA6	E27
AE25	URDATA5	UXDATA5	G28
AE26	URDATA4	UXDATA4	G26
AE27	URDATA3	UXDATA3	H25
AE28	URDATA2	UXDATA2	E27
AE29	URDATA1	UXDATA1	F26
AA29	URDATA0	UXDATA0	G25

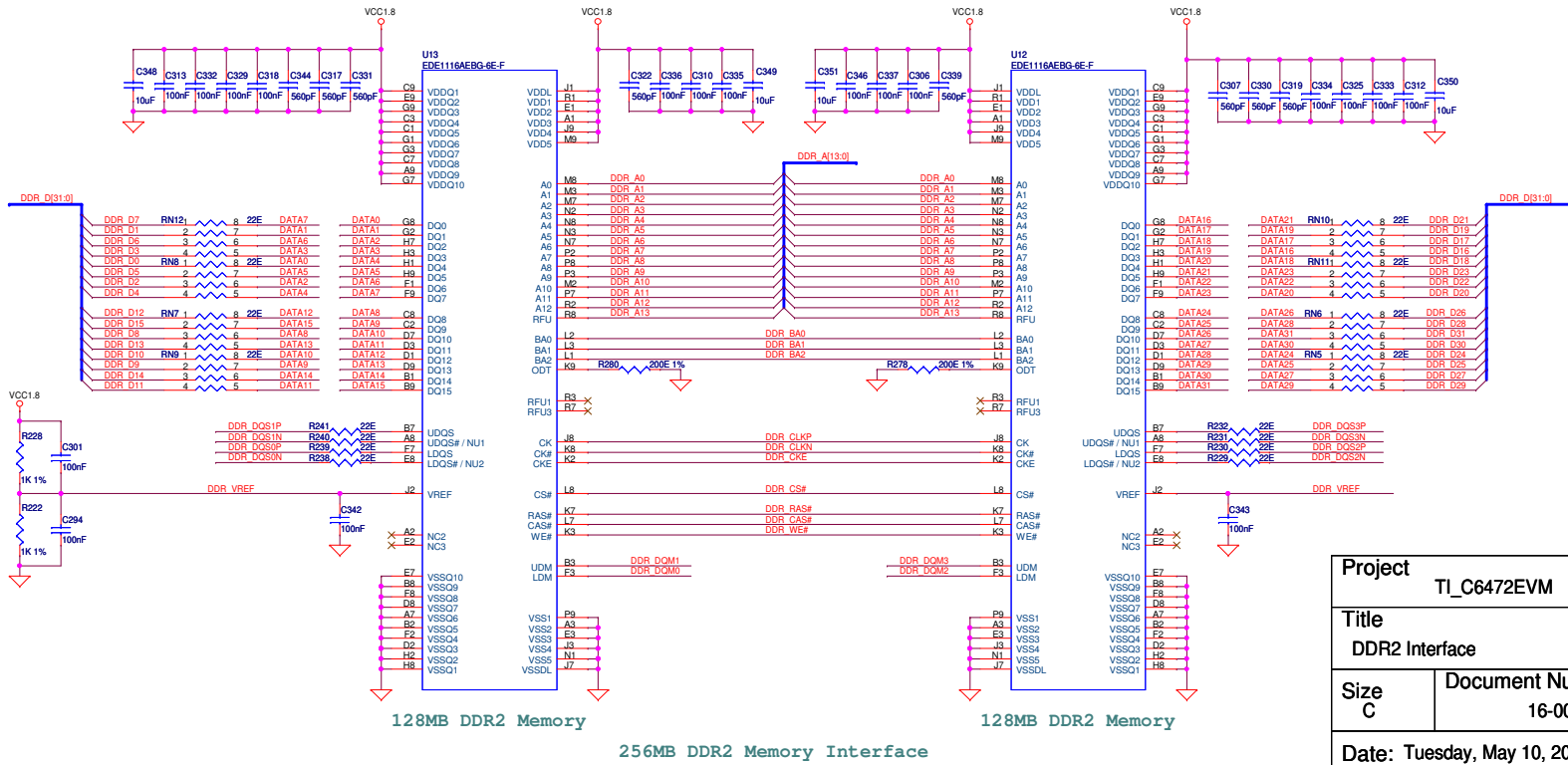
Project	TI_C647EVM		Designed for TI by	Infochips
Title	JTAG Emulation			The Solutions People
Size	C	Document Number	16-00065-06	Rev
				6.1
Date:	Tuesday, May 10, 2011		Sheet	4 of 12



C6472 DDR2 Memory Controller

Supported Memories (84 FBGA) :

	256MB (128MB x 2)	512MB (256MB x 2)
Elpida	EDE1116AEBG-6E-F	
Micron	MT47H64M16HR-3	MT47H128M16HG-3



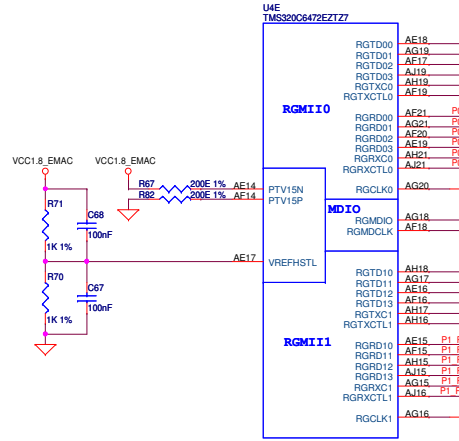
128MB DDR2 Memory

128MB DDR2 Memory

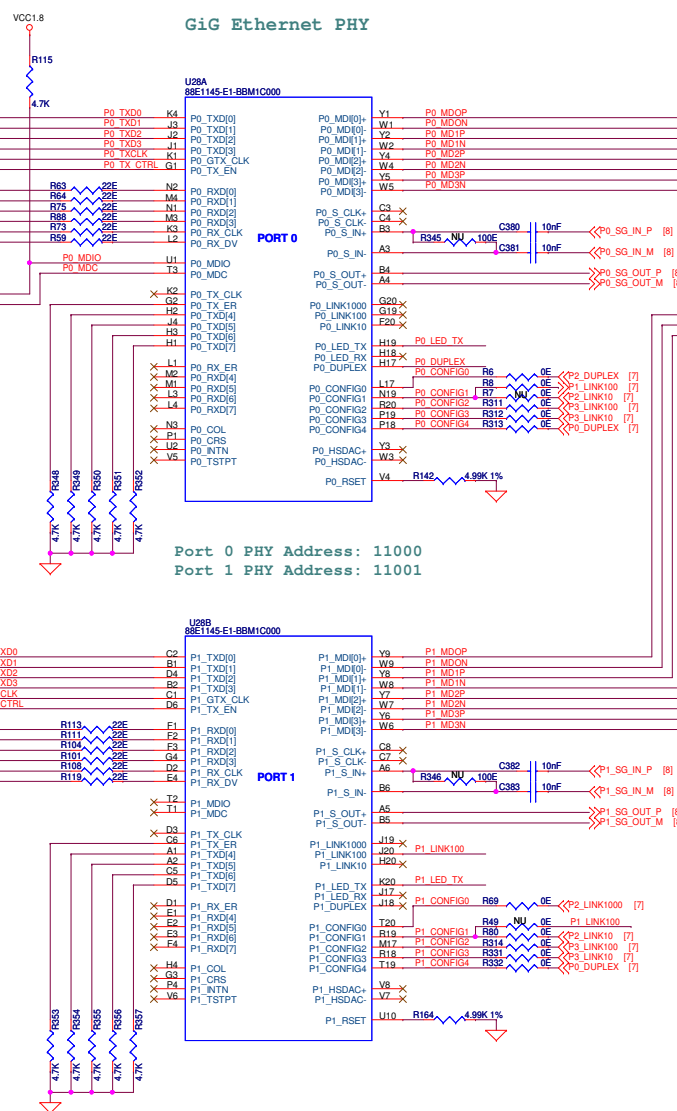
256MB DDR2 Memory Interface

Project TI_C6472EVM		Designed for TI by elfnchips	
Title DDR2 Interface			
Size C	Document Number 16-00065-06	Rev 6.1	
Date: Tuesday, May 10, 2011		Sheet 5 of 12	

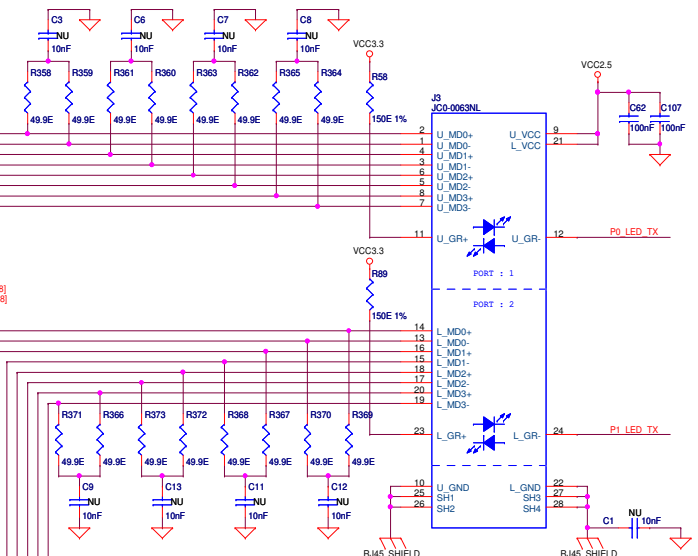
C6472 Ethernet MAC (RGMII)



GiG Ethernet PHY



Port 0 PHY Address: 11000
Port 1 PHY Address: 11001



Dual Port Connector

Port#0 Configuration Pins:

Pin	Bit[3]	Bit[2]	Bit[1]	Bit[0]
P0_CONFIG0	1	0	0	0
P0_CONFIG1	1	0	1	1
P0_CONFIG2	1	1	1	0
P0_CONFIG3	1	1	1	1
P0_CONFIG4	0	0	0	0

Port#1 Configuration Pins:

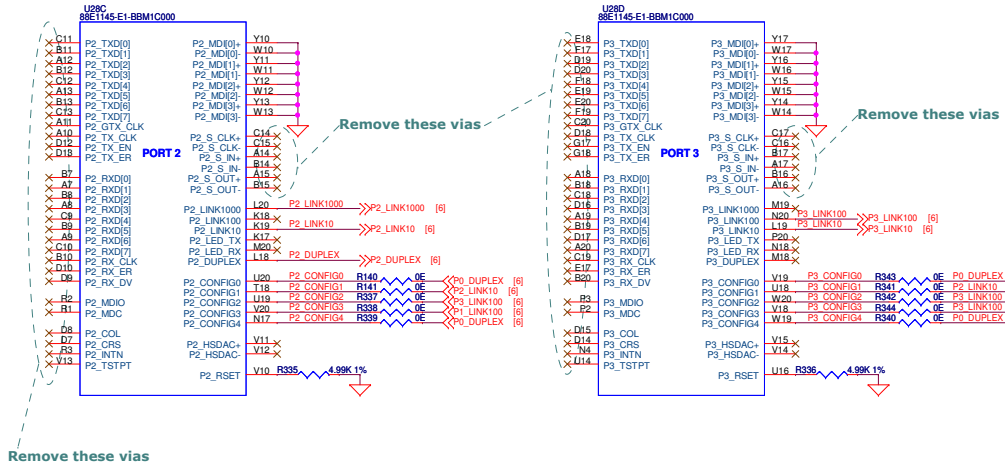
Pin	Bit[3]	Bit[2]	Bit[1]	Bit[0]
P1_CONFIG0	1	0	0	1
P1_CONFIG1	1	0	1	1
P1_CONFIG2	1	1	1	0
P1_CONFIG3	1	1	1	1
P1_CONFIG4	0	0	0	0

Note:

At Power On, Port0 will be "RGMII - SGMII" mode & Port1 will be "RGMII - Copper" mode through hardware configuration.

Project TI_C6472EVM		Designed for TI by elfnchips	
Title GiG Ethernet Interface # 01			
Size C	Document Number 16-00065-06	Rev 6.1	
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These Two ports (Port 2 & Port 3) are disabled

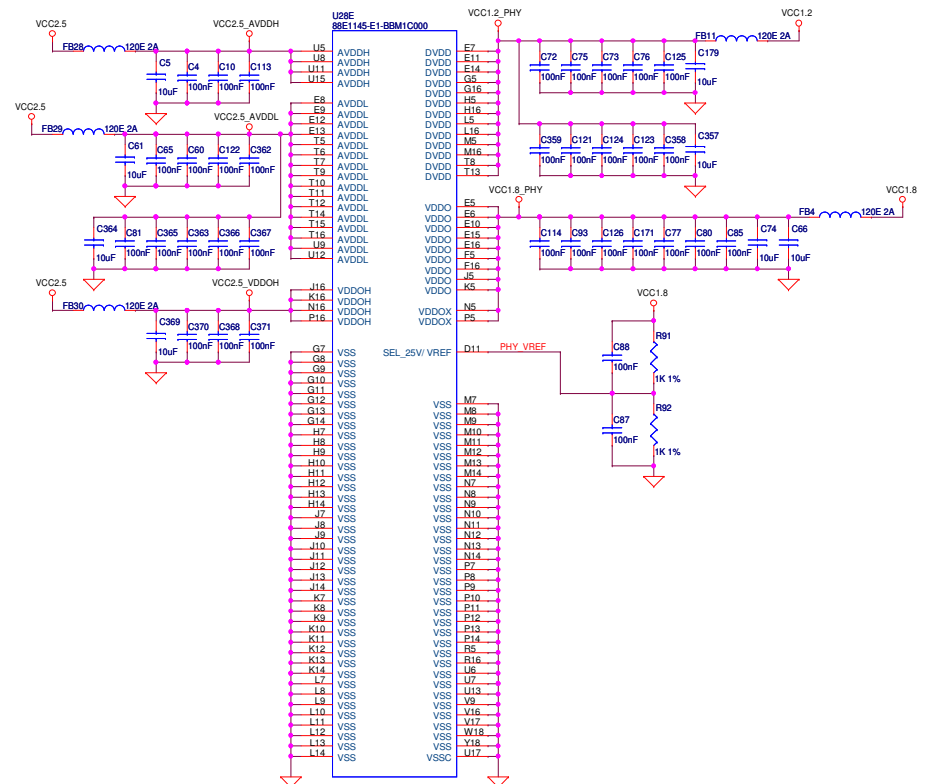


Port#2 Configuration Pins:

Pin	Bit [3]	Bit [2]	Bit [1]	Bit [0]
P2_CONFIG0	0	0	0	0
P2_CONFIG1	1	0	1	1
P2_CONFIG2	1	1	1	0
P2_CONFIG3	0	1	1	0
P2_CONFIG4	0	0	0	0

Port#3 Configuration Pins:

Pin	Bit [3]	Bit [2]	Bit [1]	Bit [0]
P3_CONFIG0	0	0	0	0
P3_CONFIG1	1	0	1	1
P3_CONFIG2	1	1	1	0
P3_CONFIG3	1	1	1	0
P3_CONFIG4	0	0	0	0



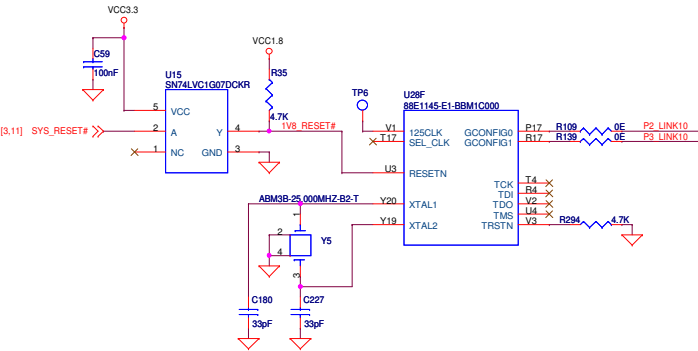
Ethernet PHY Configuration Pins:

Pin	Bit [3]	Bit [2]	Bit [1]	Bit [0]
P [3:0] _CONFIG0	PHYADR3	PHYADR2	PHYADR1	PHYADR0
P [3:0] _CONFIG1	HWCFG_3	HWCFG_2	HWCFG_1	HWCFG_0
P [3:0] _CONFIG2	ANEG3	ANEG2	ANEG1	ANEG0
P [3:0] _CONFIG3	PHYADR4	ENA_XC	DIS_FC	DIS_SLEEP
P [3:0] _CONFIG4	Reserved	Reserved	SEL_TWSI	ENA_PAUSE
GCONFIG0	DIS_DTE	75/50 OHM	1/4 MDIO	DIS_125CLK
GCONFIG1	LED_TXblink	PowerDown	SIG_DET	INT_POL

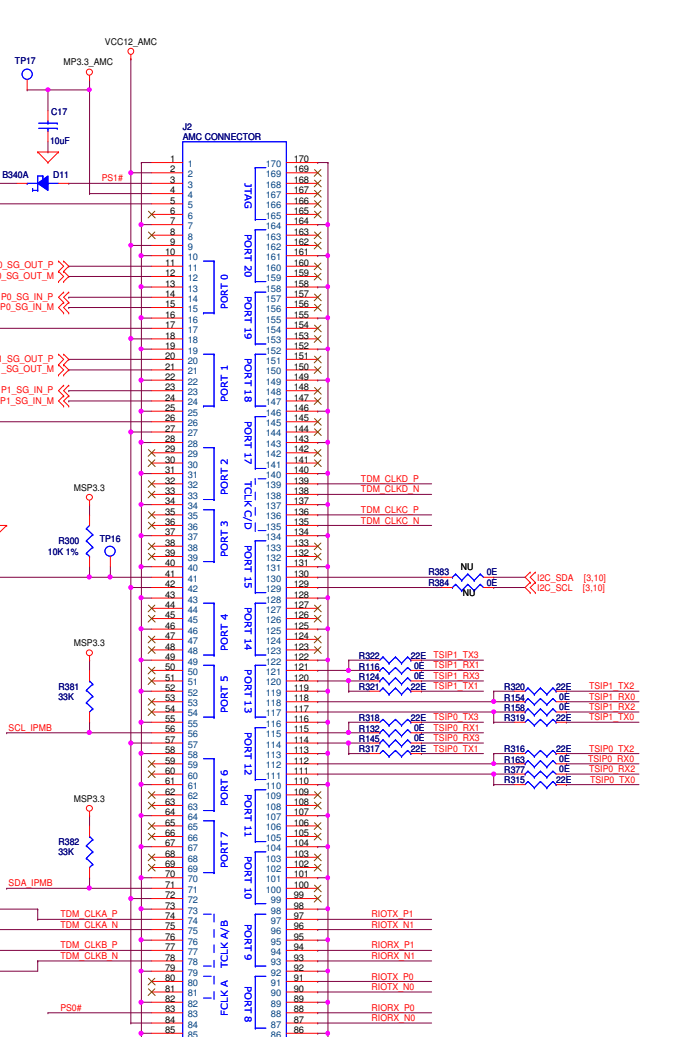
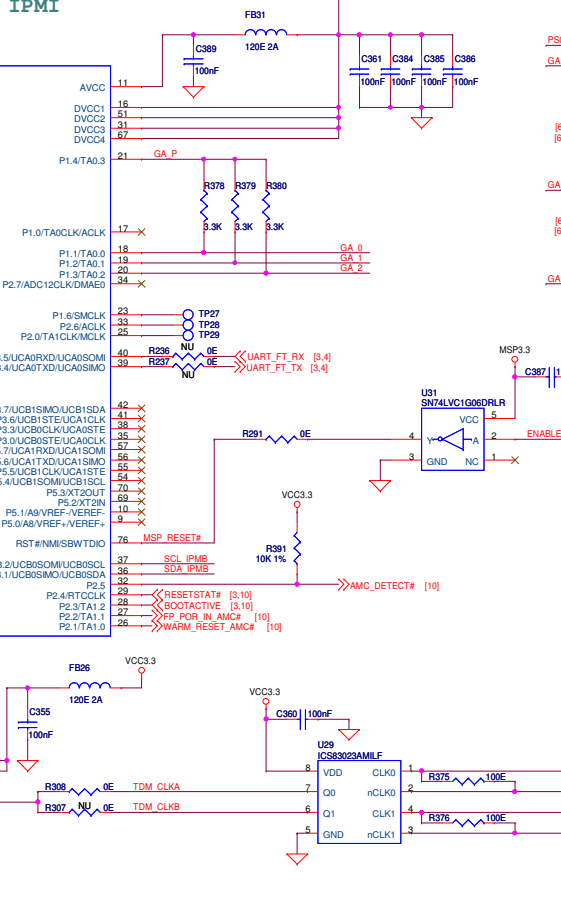
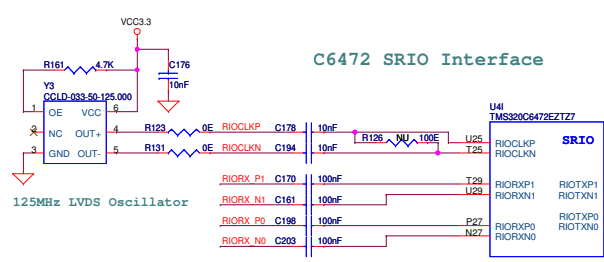
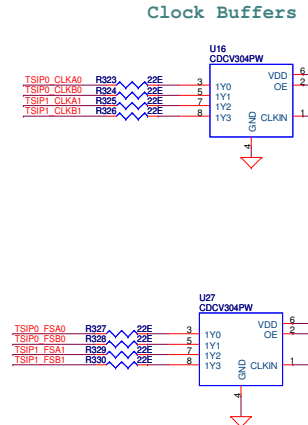
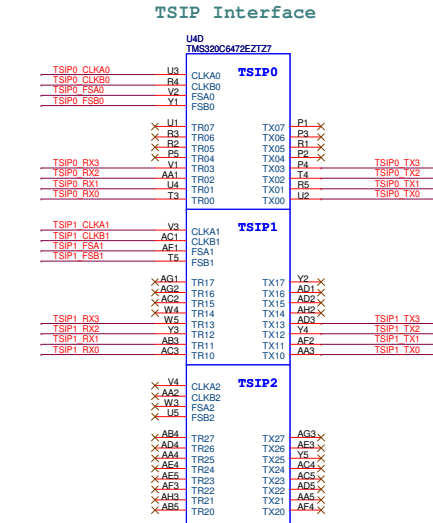
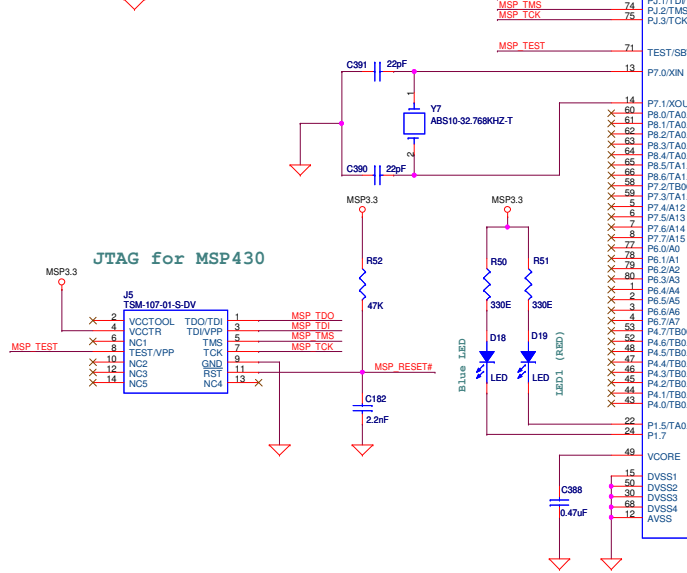
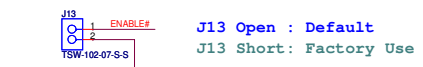
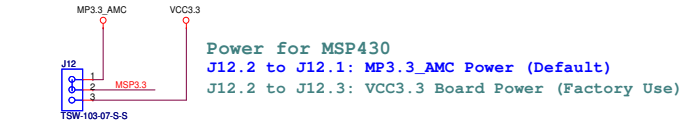
Device Pins	Bit [3:0]
P3_LINK10	1111
P3_LINK100	1110
P3_LINK1000	1101
P3 Duplex	1100
P2_LINK10	1011
P2_LINK100	1010
P2_LINK1000	1001
P2 Duplex	1000
P1_LINK10	0111
P1_LINK100	0110
P1_LINK1000	0101
P1 Duplex	0100
P0_LINK10	0011
P0_LINK100	0010
P0_LINK1000	0001
P0 Duplex	0000
All Other	Reserved

Global Configuration Pins:

Pin	Bit [3]	Bit [2]	Bit [1]	Bit [0]
GCONFIG0	1	0	1	1
GCONFIG1	1	1	1	1

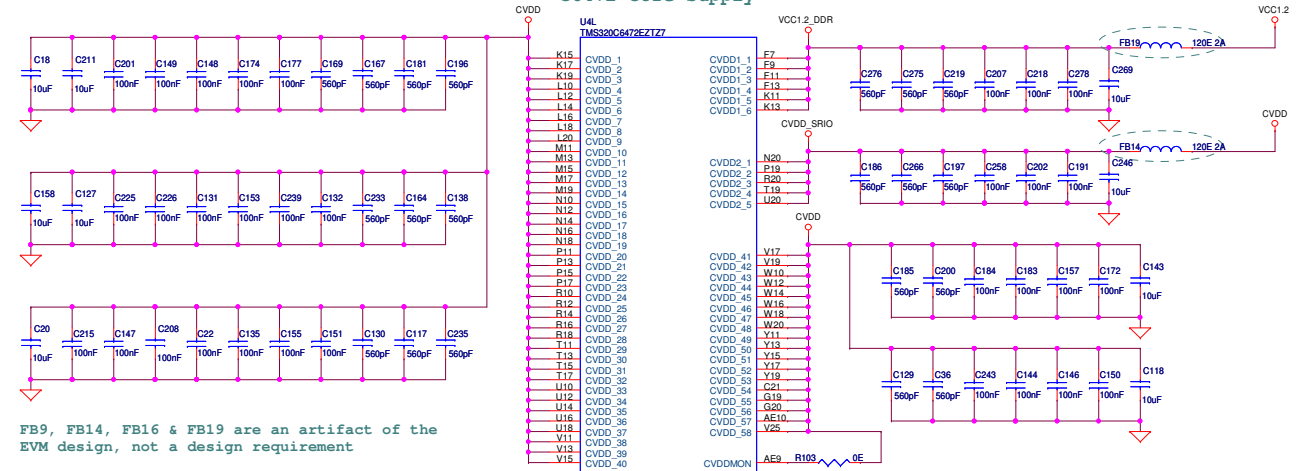


Project TI_C6472EVM		Designed for TI by elfnfochips	
Title GiG Ethernet Interface # 02			
Size C	Document Number 16-00065-06	Rev 6.1	
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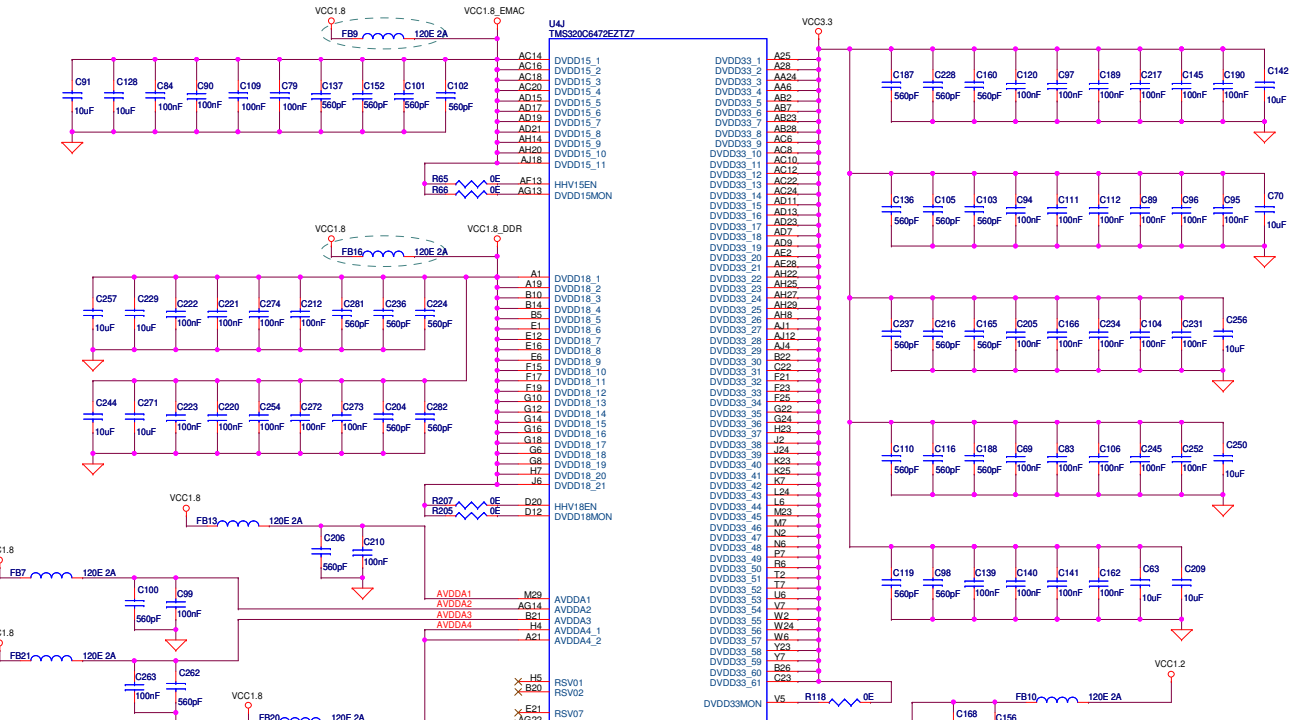
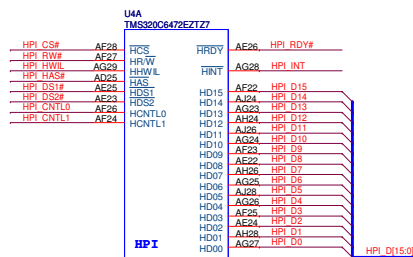
Project		TI_C6472EVM		Designed for TI by elfnfochips	
Title		MMC, AMC Connector Interface			
Size	Document Number	16-00065-06		Rev	6.1
C					
Date: Tuesday, May 10, 2011				Sheet 8 of 12	

C6472 Core Supply

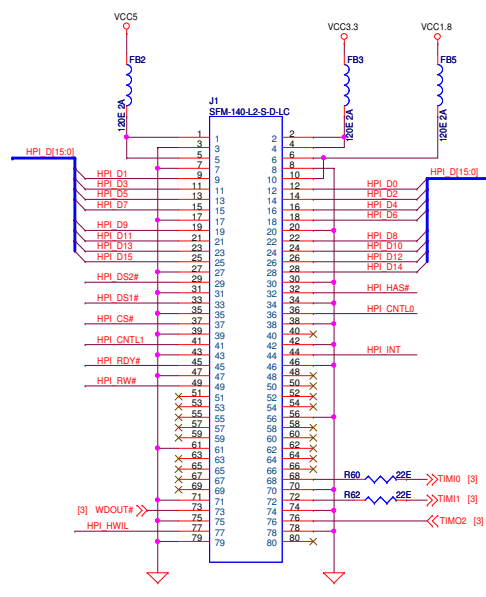


FB9, FB14, FB16 & FB19 are an artifact of the EVM design, not a design requirement


C6472 HPI Interface

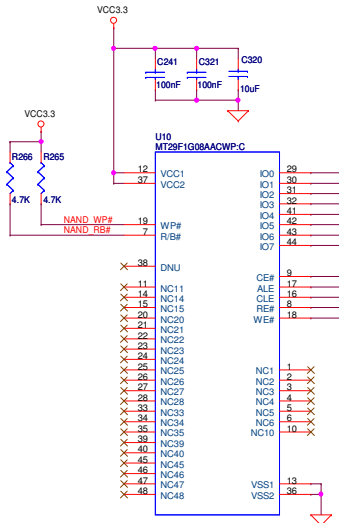


C6472 Ground

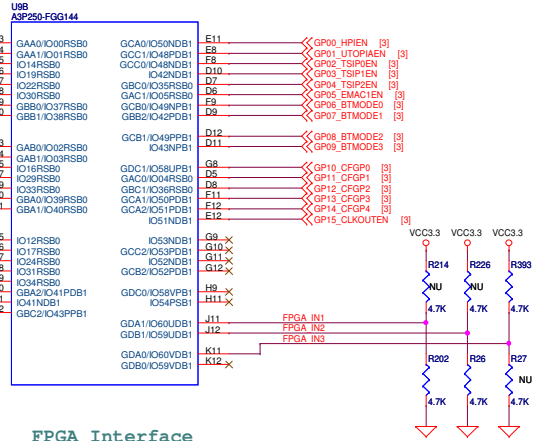


HPI DC Connector

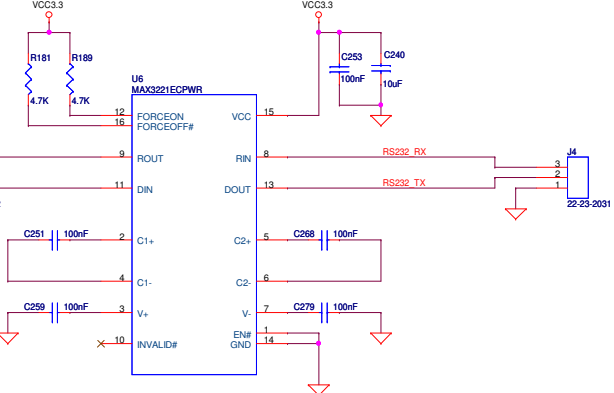
Project	TI_C6472EVM		Designed for TI by	elnfchips
Title	HPI_DSP Power Supply			The Solutions People
Size	Document Number		Rev	6.1
C	16-00065-06			
Date:	Tuesday, May 10, 2011		Sheet	9 of 12



NAND Interface



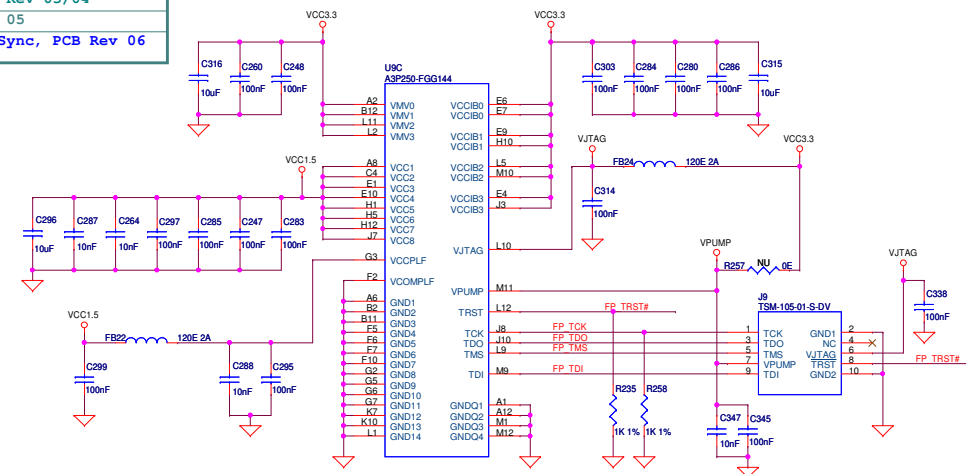
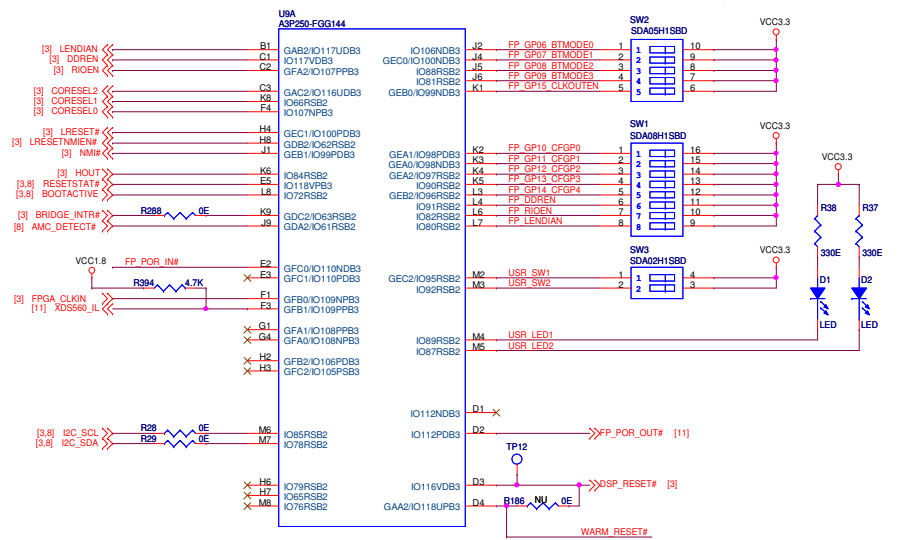
FPGA Interface



Board Build Identification

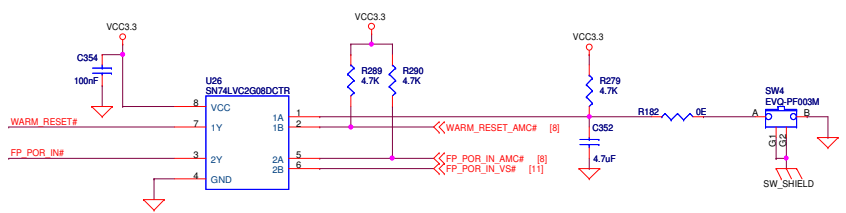
Size	128MB
Device ID	0x2C
Page Size	(2048 + 64) Byte
Block Size	64 Pages

[K11:J12:J11]	Description
000	Proto-type,PCB Rev 01
001	AMC-TSIP/I2C Changes,PCB Rev 02
010	SGMII Support Added, PCB Rev 03/04
011	IPMI MMC Added, PCB Rev 05
100	TCLKC/D used for Frame Sync, PCB Rev 06



FPGA Power

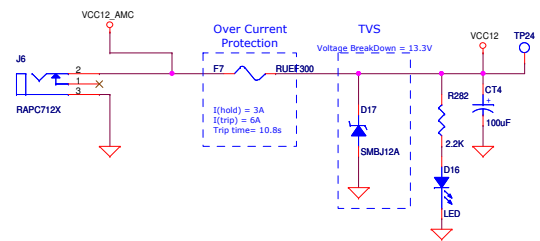
FPGA JTAG Connector



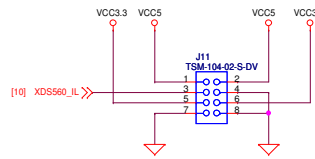
- FP GP06 BTMODE0 R244 4.7k
- FP GP07 BTMODE1 R242 4.7k
- FP GP08 BTMODE2 R255 4.7k
- FP GP09 BTMODE3 R250 4.7k
- FP LENDIAN R247 4.7k
- FP GP10 CFGP0 R246 4.7k
- FP GP11 CFGP1 R245 4.7k
- FP GP12 CFGP2 R256 4.7k
- FP GP13 CFGP3 R31 4.7k
- FP GP14 CFGP4 R30 4.7k
- FP DOREN R272 4.7k
- FP RIQEN R271 4.7k
- FP GP15 CLKOUTEN R245 4.7k
- USR_SW1 R249 4.7k
- USR_SW2 R246 4.7k

Project	TI_C6472EVM	Designed for TI by einfochips
Title	FPGA - NAND Flash Interface	TEXAS INSTRUMENTS einfochips The Solutions People
Size C	Document Number 16-00065-06	Rev 6.1
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12V DC Input Supply

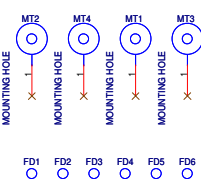
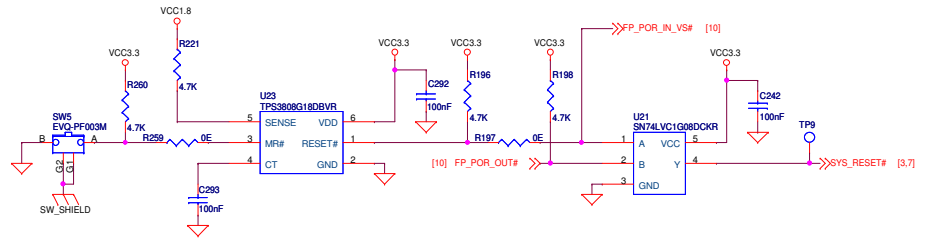
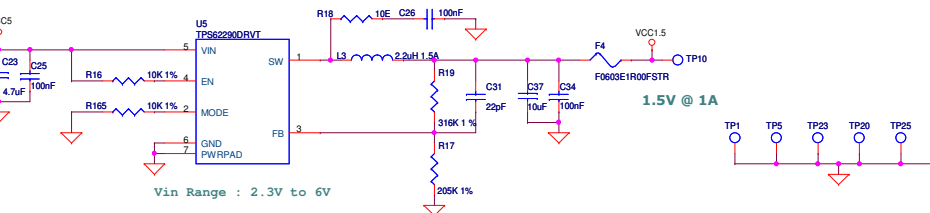
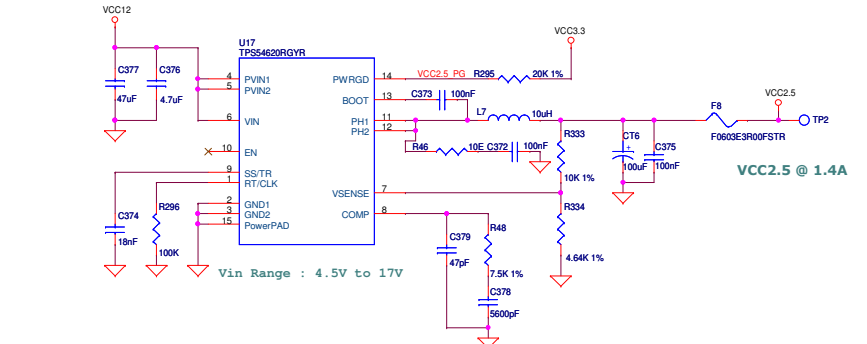
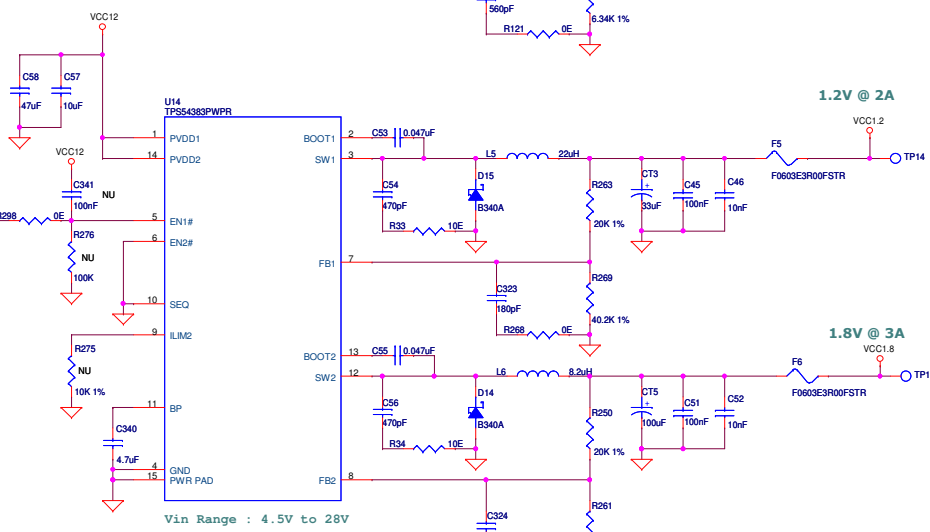
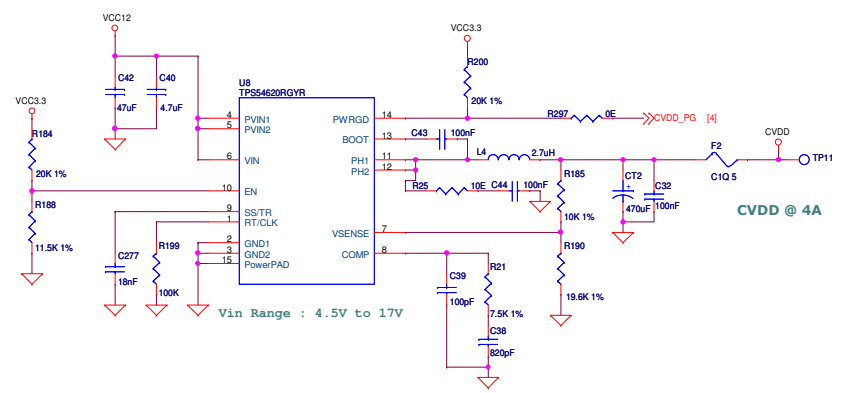
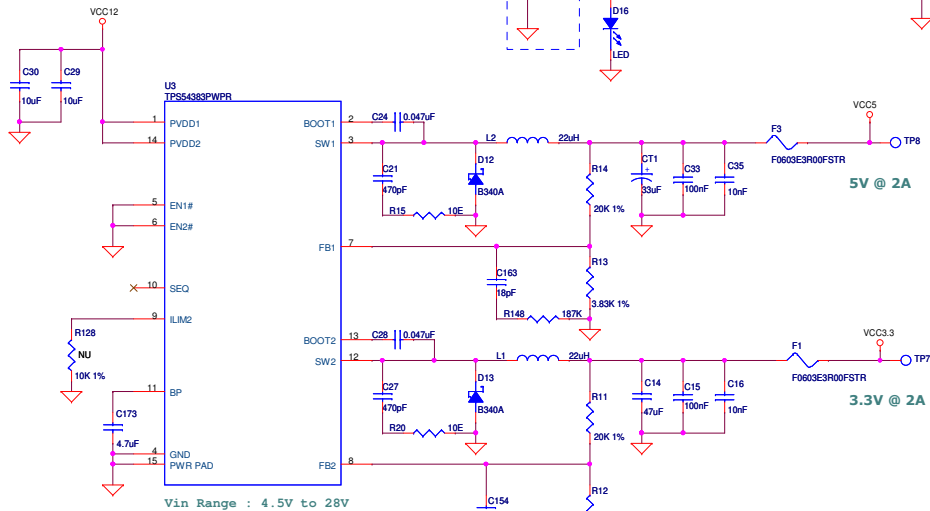


XDS560 v2 Mezzanine Power



IMPORTANT NOTE:

PLEASE REFER ISSUE#5 FROM "TMDSEVM6472-KNOWN ISSUES.PDF" DOCUMENT FOR RECOMMENDED CHANGES IN POWER SUPPLY SCHEMATIC DESIGN.




























Project TI_C6472EVM		Designed for TI by elfnchips	
Title Board Power Supply			
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TI_C6472EVM - REVISION HISTORY

PCB REV.	SCH. REV.	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	Issue 1.0	- Released for Fabrication of PCB ver1.0 (Proto-1)	06AUG2009	eInfochips
	Issue 1.1	- Updated BOM for second batch of 22 boards	09SEP2009	eInfochips
2.0	Issue 2.1	- Released for Fabrication of PCB ver2.0 (Production batch 1)	24SEP2009	eInfochips
3.0	Issue 3.2	- Released for Fabrication of PCB ver3.0 (SGMII Proto)	27OCT2009	eInfochips
4.0	Issue 4.2	- Released for Fabrication of PCB ver4.0 (SGMII Production)	22JAN2010	eInfochips
5.0	Issue 5.2	- Released for Fabrication of PCB ver5.0 (IPMI feature - Proto + Production)	18MAY2010	eInfochips
	Issue 5.3	- R126 changed to NU (Not Used) from Used - Removed U25 from I2C address table at sheet 1 - U11.28 changed to NC (No Connect) - Note on sheet 3 changed from "UART over 3-Pin Header J5" to "UART over 3-Pin Header J4" - Added "Universal Travel Adaptor" as dummy part. -- WEB Release for V05 batch	12JULY2010	eInfochips
6.0	Issue 6.0	- Pull down added on UART inputs lines - Pull up added on "TG_TCK" net - Board build identification changed from 2 bit to 3 bit - U2 (ICS83023AMILF) added	04SEP2010	eInfochips
	Issue 6.1	- D18 Part # changed to LNJ952W8CRA1 (old part is obsolete) - Added note in power supply page	10MAY2011	eInfochips

Dummy Components

 DM1 AS300-120-A0250 Power Adaptor	 DM2 PS737-R-BGA080 DSP Socket	 DM3 22-01-2031 UART - Cable Connector	 DM4 UART Cable	 DM16 STC02SYAN Shoring Link	 DM17 STC02SYAN Shoring Link	 DM5 USB miniB cable	 DM14 LAN cable	 DM15 Heat-Sink	 DM6 Board Screw	 DM7 Board Screw	 DM8 Board Screw	 DM9 Board Screw	 DM19 06-50-0113 Crimp Pin	 DM20 06-50-0113 Crimp Pin	 DM21 06-50-0113 Crimp Pin	 DM10 Board Stud	 DM11 Board Stud	 DM12 Board Stud	 DM13 Board Stud
			 DM23 Universal Travel Adaptor	 DM18 STC02SYAN Shoring Link	 DM22 STC02SYAN Shoring Link														

Project TI_C6472EVM		Designed for TI by eInfochips	
Title Revision History & Dummy Parts		  The Solutions People	
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