Message from the President

Dear Colleague,

Greetings!

The VLSI Society of India continues its efforts to build and sustain an eco-system for research and development in all areas related to VLSI. Several events have already happened this year and more are planned during the year. I strongly recommend you to visit our website on a regular basis to find out about our activities. Members also get notified through e-mail about new activities. You will also find a calendar of planned events in this issue of VSI VISION.

India has established itself as a strong force in VLSI over the past two decades. As will be evident from the research summaries published in VSI VISION, a significant number of papers and patents are originating from India. Many papers are accepted for publication in premier journals and conferences. I am also pleased to see that research originating from India is getting recognition in international forums through awards and appreciation. Much more of this must happen in the future!

While India has a vantage position in niche areas in digital design and verification, we need to go aggressively on full system design, which includes sensors, analog/RF circuits, and MEMS. Much more meaningful collaboration across organizations will be necessary to make this happen. I hope that the forums, which VSI provides, will be used towards this cause. We plan to offer more diversity in our technical programs in the future through focused activities in areas such as embedded systems and their applications in medicine, energy, surveillance, and LED lighting.

As always, we look forward to your suggestions and active participation. We value your feedback!

With best wishes,

Bobby Mitra
July 2008

Editorial

Industry-academia interaction is the most discussed topic in conferences. I have participated in several panel discussions myself and have noticed several recurring themes in this discussion. One of these has to do with placement of students as interns and full-time employees in the industry. With a number of engineering colleges coming up in the recent years and more engineers graduating each year, ironically, the problem of hiring has become more difficult for the industry. In a recently organized panel discussion at Mysore, several panelists from the industry were asked what they look for in a graduating engineer. Most panelists emphasized that they judge a candidate the fundamentals.

The nature of the jobs in the industry today is such that specialization is required. A student may do any of the following within a year of his joining a VLSI company – write or verify hardware descriptions, use formal verification techniques to expose bugs, synthesize hardware descriptions under constraints, design or verify analog circuits, analyze timing of synthesized logic and debug timing problems, use physical design tools to generate layouts that pass a variety of checks, use design-for-testability tools to add test-related circuitry, generate test patterns, write system-software for embedded platforms, develop applications of embedded systems, …

To make this picture even more complex, some jobs demand knowledge in application-areas such as telecommunications, RF, computer networks, digital audio, image processing, video, biomedicine, …

It is unfair to expect the colleges to teach all the special topics in an undergraduate curriculum, which spans a period of four years after twelve years of schooling. The older scheme of five-year undergraduate education provided some flexibility to steer students towards specialization through industrial training. Some specialization can be introduced in the undergraduate program through elective subjects. For example, in most Indian Institutes of Technology, the undergraduate student gets a degree in *Electrical Engineering*. The student may take some elective subjects in broad areas such as electronic communications, power electronics, control theory, computer architecture, biomedical electronics, and so on, depending on the student's interest and the availability of elective subjects.

Many Indian Universities offer specialized undergraduate degrees in Electronics, Electronics and Communication, Telecommunication, Information Technology, Instrumentation, Industrial Electronics, Computer Science, Biomedical Engineering, Biotechnology, and so on. However, often there is not much variation in the curriculum of these degrees. Most colleges do not have specialized faculty in these areas. Industries do not seem to particularly recognize these specializations when they visit a campus for placement. An extreme example is that of "IT companies" that hire from all these branches of engineering – in fact, they even hire students from Civil, Mechanical, and Textile engineering.

Postgraduate study is the natural answer to fulfill the need of specialization that the industries demand, but our M.Tech and MS programs seem to suffer from similar problems. Many companies, therefore, either do not hire postgraduate students, or do not provide sufficient differentiation in benefits when hiring them. The companies argue that they have to invest a similar amount of effort to make a postgraduate student productive. On the brighter side, when a postgraduate program of repute does exist, companies offer significant amount of support to such programs through student fellowships, mentoring, campus placements, and handsome differentiation in benefits.

When VLSI companies have to focus on the much larger population of undergraduate students for hiring, selection is a daunting task. This gets more complicated when companies begin to make offers much earlier, as early as the fifth semester, in the hope of attracting the best. There seems to be general consensus that this is a bad move. Professors complain that students who have job offers in the fifth semester have no serious motivation to take the specialized courses or pursue a specialized project! Industries complain that conducting tests and interviews in the fifth semester can be a challenge.

What, indeed, does someone look for when testing or interviewing a nineteen or twenty year old student for a job that demands much skill and specialization? "Ability to learn" and "strong fundamentals" are the answers that emerge in a number of discussions I have had with industry representatives. Some people also state "soft skills" as an additional criterion. Perhaps we must spend time to discuss and understand these concepts better.

Companies that are looking for special manpower have to do their bit to contribute towards postgraduate programs that have been created to solve the manpower problem. Similarly, the management of colleges must also encourage their faculty and provide the inputs to improve the postgraduate programs.

While curricula exist for postgraduate programs, many colleges do not have faculty to teach the specialized courses. Training the faculty in specialized areas is an area that needs immediate and close attention. I see numerous examples of engineers from industry willing to teach in colleges. This is an incomplete and perhaps an incorrect solution, since it is not sustainable or scalable. A better solution is to train the trainer through mentoring, faculty internship programs and summer training programs for faculty.

A strong research program is necessary to support a strong teaching program. Unless the faculty are engaged in research activities, they will soon fall behind in the fast-changing world of VLSI. Some Universities are making it mandatory for their faculty to obtain higher education (M.Tech, MS, or Ph.D.) It is also important for faculty to continually get updates from fellow researchers on the latest developments in VLSI. This can be done through participation in conferences and workshops and by following published literature. While many colleges are beginning to host their own conferences and workshops, they seem to suffer from lack of serious industry participation.

There is much to be done to solve the problems of undergraduate and postgraduate programs, which I have mentioned above. The VLSI Society of India provides forums where solutions to these problems can be discussed and attempted. The activities of VSI promote much-needed faculty-industry interaction and we appeal to the management of companies, the engineers, the management of educational institutions, and the faculty to support these activities and contribute to them in one way or another. I look forward to hearing from you if you have any ideas in this matter.

If you have additional ideas or counter points on any of the thoughts I have captured in this editorial, please do write. We also look forward to your feedback on this issue of VSI VISION.

C.P. Ravikumar

CONTENTS

AWARDS

Indian Research Scholar wins the IEEE TTTC Doctoral Dissertation Award

VSI congratulates **Devanathan Varadarajan** for winning the first place in the Doctoral Thesis contest organized by the IEEE Test Technology Technical Council. The contest was held at the VLSI Test Symposium during April 2008 in San Diego. Devanathan, an employee of Texas Instruments, India, and a part-time Ph.D. student in the Department of Computer Science and Engineering at IIT Madras, won the award for his thesis entitled "On the power-safe testing of system-on-chips." He submitted the thesis in December 2007 and defended it successfully in May 2008. His supervisors were Dr. C.P. Ravikumar of Texas Instruments and Prof. V. Kamakoti of IIT Madras.

The Doctoral Thesis contest is held annually and is open to all Ph.D. students who have worked on a problem related to VLSI Test and have submitted the thesis in the academic year in which the contest is held. The student must submit a summary of the thesis and must present the highlights of the contributions to an international panel of judges. Congratulations to Devanathan for winning this prestigious award!

Global Indus Technovator Awards

Anantha P. Chandrakasan has received the GITA2007 Award (Global Indus Technovator Awards) under Materials and Energy category. The awards recognize innovators, from either a technical or entrepreneurial perspective, in the fields of biotechnology, healthcare and medicine, information technology, materials and devices, energy, and developmental work.

Anantha P. Chandrakasan received the B.S, M.S. and Ph.D. degrees in Electrical Engineering and Computer Sciences from the University of California, Berkeley, in 1989, 1990, and 1994 respectively. Since September 1994, he has been with the Massachusetts Institute of Technology, Cambridge, where he is currently the Joseph F. and Nancy P. Keithley Professor of Electrical Engineering. More information can be accessed through http://technovators.mit.edu/gita/2007_winners_materials.html#chandrakasan

International Publications and Patents from Indian Authors

POWER-AWARE TEST: CHALLENGES AND SOLUTIONS

Srivaths Ravi (Texas Instruments India)

Name of the International Journal/Conference: ITC 2007 (International Test Conference)

Abstract: Power-aware test is increasingly becoming a major manufacturing test consideration due to the problems of increased power dissipation in various test modes as well as test implications that arise due to the usage of various lowpower design technologies in devices today. Several challenges emerge for test engineers and test tool developers, including (and not restricted to) understanding of various concerns associated with power-aware test, development of power-aware design-fortest (DFT), automatic test pattern generation (ATPG) techniques, and test power analysis flows, evaluation of their efficacy and ensuring easy/rapid deployment. This paper highlights concerns and challenges in power-aware test, surveys various practices drawn from both academia and industry, and points out critical gaps that need to be addressed in the future.

TEST STRATEGIES FOR LOW POWER DEVICES

C. P. Ravikumar, M. Hirech, and X. Wen

Name of the International Journal/ Conference: DATE 2008 (Design Automation and Test in Europe)

Abstract: Ultra low-power devices are being developed for embedded applications in bio-medical electronics, wireless sensor networks, environment monitoring and protection, etc. The testing of these low-cost, low-power devices is a daunting task. Depending on the target application, there are stringent guidelines on the number of defective parts per million shipped devices. At the same time, since such devices are cost-sensitive, test cost is a major consideration. Since system-level power-management techniques are employed in these devices, test generation must be powermanagement- aware to avoid stressing the power distribution infrastructure in the test mode. Structural test techniques such as scan test, with or without compression, can result in excessive heat dissipation during testing and damage the package. False failures may result due to the electrical and thermal stressing of the device in the test mode of operation, leading to yield loss. This paper considers different aspects of testing low-power devices and some new techniques to address these problems.

METHODOLOGY FOR LOW POWER TEST PATTERN GENERATION USING ACTIVITY THRESHOLD CONTROL LOGIC

Srivaths Ravi, Varadarajan Devanathan, and Rubin Parekhji (Texas Instruments India)

Name of the International Journal/ Conference: ICCAD 2007 (International Conference on Computer Aided Design)

Abstract: This paper proposes a new technique of power-aware test pattern generation, wherein the test mode power constraints are specified using pseudo hardware logic functions (referred to as power constraint circuits) that augment the target circuit fed to the ATPG tool. The novelty of this approach is three-fold: (i) The ATPG tool only sees the enhanced circuit This influences the generation of the test cubes themselves, as against post-processing of these cubes for a given pattern, (ii) Pattern generation can be driven to minimize test power according to a programmable switching activity threshold, and hence, is scalable, (iii) The same constraint circuit can also be effectively used for pattern filtering to isolate patterns which cause high switching activity. Additionally, the proposed method does not require any changes to the pattern generation tool or process. This paper describes the methodology, together with techniques for realizing the hardware circuit and specifying thresholds. Experimental results on various benchmark circuits (including an industrial design) are presented to show the effectiveness of this approach.

A STOCHASTIC PATTERN GENERATION AND OPTIMIZATION FRAMEWORK FOR VARIATION-TOLERANT, POWER-SAFE SCAN TEST

V.R. Devanathan, C.P. Ravikumar and V. Kamakoti

Abstract: Process variation is an increasingly dominant phenomenon affecting both power and performance in

sub-100 nm technologies. Cost considerations often do not permit overdesigning the power supply infrastructure for test mode, considering the worst-case scenario. Test application must not overexercise the power supply grids, lest the tests will damage the device or lead to false test failures. The problem of debugging a delay test failure can therefore be highly complex. We argue that false delay test failures can be avoided by generating "safe" patterns that are tolerant to on-chip variations. A statistical framework for power-safe pattern generation is proposed, which uses process variation information, power grid topology and regional constraints on switching activity. Experimental results are provided on benchmark circuits to demonstrate the effectiveness of the framework.

A REGRESSION BASED TECHNIQUE FOR ATE-AWARE TEST DATA VOLUME ESTIMATION OF SYSTEM-ON-CHIPS

Rajesh Tiwari, Abhijeet Shrivastava, Mahit Warhadpande, Srivaths Ravi, and Rubin Parekhji, (Texas Instruments India)

Name of the International Journal/ Conference: VTS 2008 (VLSI Test Symposium)

Abstract: Conventional methods to assess the test data volume (TDV) of logic in system-on-chips (SoCs) use intuitive formulae that are often agnostic of the target automatic test equipment (ATE) hardware or the ATE test program compilation process. In this paper, we first show that such ATE-unaware approaches lead to a significant gap between these estimates and the actual tester memory consumed. We also provide a generic solution to this problem by using statistical regression techniques to build an ATE-aware TDV model that accurately estimates test program memory consumption as a function of the design and test pattern characteristics. We have implemented this methodology using an off-the-shelf regression solver in the context of a production test flow. We show that the estimator can be used to compute TDV with very high accuracy for logic tests of various industrial IPcores and SoCs.

PMSCAN: A POWER-MANAGED SCAN FOR SIMULTANEOUS REDUCTION OF DYNAMIC AND LEAKAGE POWER DURING SCAN TEST

V.R. Devanathan (Texas Instruments), C.P. Ravikumar (Texas Instruments), Rajat Mehrotra (Texas Instruments), V. Kamakoti (IIT Madras)

Abstract: In sub-70nm technologies, leakage power becomes a significant component of the total power. Designers address this concern by extensive use of adaptive voltage scaling techniques to reduce dynamic as well as leakage power. Low-power scan test schemes that have evolved in the past primarily address dynamic power reduction, and are less effective in reducing the total power. We propose a Power-Managed Scan (PMScan) scheme, which exploits the presence of adaptive voltage scaling logic to reduce test power. We also discuss some practical implementation challenges that arise when the proposed scheme is employed on industrial designs. Experimental results on benchmark circuits and industrial designs show a significant reduction in dynamic and leakage power. The proposed method can also be used as a vehicle to trade-off test application time with test power by suitably adjusting the scan shift frequency and scan-mode power supplies.

LOW POWER TEST FOR NANOMETER SYSTEM-ON-CHIPS (SOCS)

Srivaths Ravi, Rubin Parekhji, and Jayashree Saxena (Texas Instruments India)

Name of the International Journal: Journal of Low Power Electronics (JOLPE), April 2008

Abstract: Shrinking power consumption budgets and increasing use of low power design techniques in nanometer designs are forcing test engineers to examine the two problems of (a) reducing power consumption in the test mode of circuit operation, and (b) testing the device in the presence of various power management structures. This paper examines the various concerns associated with this domain (often referred to as low-power or power-aware test), identifies the relevant design and test challenges, surveys salient solutions along with the associated trade-offs, and identifies open topics that require further attention from researchers in both academia and industry.

MEMORY YIELD IMPROVEMENT THROUGH MULTIPLE TEST SEQUENCES AND APPLICATION-AWARE FAULT MODELS

Aman Kokrady* (Texas Instruments), C.P. Ravikumar (Texas Instruments), Nitin Chandrachoodan (IIT Madras)

Abstract: The inability to screen memory defects especially in newer technology with pre-programmed algorithms calls for ability to program newer algorithms on the fly on silicon. Such Built in Self Test strategy is known as Programmable BIST (PBIST). In this paper,

we propose a way to improve the yield and reduce the DPPM of memory products by selecting the appropriate test strategy for a memory using PBIST. Memories are getting more sensitive to variations in layout, voltage scaling and process variations. This causes memory defects to occur not just in bit-array but also in the peripheral logic. We argue that the test strategy must take into consideration the usage model of the memory to test. This reduces DPPM while increasing yield. For example, a number of video and audio buffers are used in sequential access mode, but are overtested using conventional memory test algorithms which model a large number of defects which do not impact the operation of the buffers. We propose a binning strategy where memory test algorithms are applied in different order of strictness such that bins have a specific defect / fault grade. A theoretical model for yield improvement with cost-benefit analysis is presented. Experimental data on production devices will be presented to illustrate the impact of new techniques both on yield and DPPM.

SOPC BASED ASYNCHRONOUS PIPELINED DCT WITH SELF TEST CAPABILITY

T.N.Prabakar (Saranathan College of Engg, Tiruchirappalli), G.Lakshminarayanan, and K.K.Anilkumar (NIT Tiruchirappalli)

International Conference on Microelectronics, 29-31 December 2007 at Cairo, Egypt

Asynchronous pipelined circuits have many potential advantages over their synchronous equivalents including lower power consumption, design reuse without compromise in speed. In this paper, a new technique i.e., “SOPC based Asynchronous Pipelining Technique” (SOPC – System On Programmable Chip) is used for designing and implementing FPGA based Low-Power VLSI Systems. In this approach, the soft core processor available within the FPGA is used to generate various control signals to control the asynchronous data flow in addition to its regular work as processor. Importantly, NIOS processor is also used to validate the results by comparing the results with a known set of test vectors. This type of verification and validation of the digital systems using NIOS provides higher speed and doesn’t require any external hook up wires and I/O cards. To verify the efficacy of the proposed approach, an 8 tap DCT using Winograd algorithm is implemented as External Logic to the NIOS processor. The intermittent data between asynchronous pipelined stages are latched by using multiplexer based latches. The completion of each stage is informed to the NIOS processor using interrupts. In turn, NIOS processor generates various control signals to pass the intermittent data stored in the multiplexer based latches. The designed system has been implemented in a STRATIX EP1S25F780C5 FPGA SOPC kit. The results are validated using the same NIOS processor. In the proposed system, storage of intermittent data is done with multiplexer based latches instead of pipelined registers. Hence this approach results in obtaining the speed of a pipelined DCT with comparably lower power consumption. This approach is also avoiding the need for global clock signals and their consequences like skew problems.

COMPARATIVE STUDY OF EVOLUTIONARY MODEL AND CLUSTERING METHODS IN CIRCUIT PARTITIONING PERTAINING OF VLSI DESIGN

Prof K.A Sumithradevi, Banashree.N.P, Dr. Annamma Abraham, Dr.Vasanta.R (R.V. College of Engineering, Bangalore)

Name of the International Journal: **ENFORMATIKA,** International Journal of Applied Mathematics and Computer Sciences, Quarterly Volume 4 Number 2, ISSN 1305-5313
Month/ Year of Publication: April 2007

Abstract: Partitioning is a critical area of VLSI CAD. In order to build complex digital logic circuits its often essential to sub-divide multi –million transistor design into manageable Pieces. This paper looks at the various partitioning techniques aspects of VLSI CAD, targeted at various applications. We proposed an evolutionary time-series model and a statistical glitch prediction system using a neural network with selection of global feature by making use of clustering method model, for partitioning a circuit. For evolutionary time-series model, we made use of genetic, memetic & neuro-memetic techniques. Our work focused in use of clustering methods - K-means & EM methodology. A comparative study is provided for all techniques to solve the problem of circuit partitioning pertaining to VLSI design. The performance of all approaches is compared using benchmark data provided by MCNC standard cell placement benchmark net lists. Analysis of the investigational results proved that the Neuro-memetic model achieves greater performance then other model in recognizing sub-circuits with minimum amount of interconnections between them.

Keywords: VLSI, Circuit Partitioning, Neuro-Memetic, Memetic algorithm, genetic algorithm.

A NEW CLUSTERING APPROACH FOR VLSI CIRCUIT PARTITIONING

Prof K.A Sumithradevi, Vijayalakshmi.M.N, Dr. Annamma Abraham, Dr.Vasanta.R (R.V. College of Engineering, Bangalore)

Name of International Conference: IV International Conference on Computer, Electrical and Systems, Science and Engineering CESSE 2007

Publishing: Proceedings of World Academy of Science, Engineering and Technology, Volume 25, ISSN 1307-6884

Month/Year of Publishing: November 2007

Abstract: Circuit partitioning is a vital problem in very large scale integration (VLSI) for physical design algorithm. This paper aims at a range of partitioning methodological aspects, which predicts to divide the circuit into subcircuits with minimum interconnections between them. Our paper considers two clustering algorithms Nearest neighbor and PAM clustering algorithm for dividing the circuits into subcircuits. The experimental results show that PAM clustering algorithm yield better subcircuits than Nearest neighbour. The experimental results are compared using benchmark data provided by MCNC standard cell placement bench netlists.

Keywords: Circuit Partitioning, VLSI, nearest neighbor, PAM

EVALUATION OF FUZZY ARTMAP WITH DBSCAN IN VLSI APPLICATION

Prof K.A Sumithradevi, Vijayalakshmi.M.N, Dr. Annamma Abraham, Dr.Vasanta. R (R.V. College of Engineering, Bangalore)

Name of International Conference: IV International Conference on Computer, Electrical and Systems, Science and Engineering CESSE 2007

Publishing: Proceedings of World Academy of Science, Engineering and Technology, Volume 26, ISSN 1307-6884

Month/Year of Publishing: December 2007

Abstract: The various applications of VLSI circuits in high-performance computing, telecommunications, and consumer electronics has been expanding progressively, and at a very hasty pace. This paper describes a new model for partitioning a circuit using DBSCAN and fuzzy ARTMAP neural network. The first step is concerned with feature extraction, where we had make use DBSCAN algorithm. The second step is the classification and is composed of a fuzzy ARTMAP neural network. The performance of both approaches is compared using benchmark data provided by MCNC standard cell placement benchmark netlists. Analysis of the investigational results proved that the fuzzy ARTMAP with DBSCAN model achieves greater performance then only fuzzy ARTMAP in recognizing sub-circuits with lowest amount of interconnections between them the recognition rate using fuzzy ARTMAP with DBSCAN is 97.7% compared to only fuzzy ARTMAP.

Keywords: VLSI, Circuit partitioning, DBSCAN, fuzzy ARTMAP

DIGITAL CIRCUIT DESIGN USING CMOS TRANSISTOR MODEL FOR DEVELOPMENT IN ASIC/SOC TECHNOLOGY

Saroj Kumar Satapathy, Design Engineer: Storage, LSI Research, Bangalore, India

Name of the international journal/conference: ISSCS 2007 (International Symposium on Signals, Circuits and Systems, Lasi, Romania)

Month/Year of publication: July 12-13, 2007

Abstract: With the advent in VLSI technology and design, the challenge to design the complex ICs and maximizing productivity in the methodology has grown. In order to meet market expectation of cost, time, and quality, it is indispensable to reuse pre-defined blocks called Intellectual Property (IP) modules in Application Specific IC (ASIC)/ System-on-Chip (SOC) designs. At the same time, improving the quality and attributes of these basic blocks has also become essential. This paper aims at describing a basic Complementary Metal Oxide Semiconductor (CMOS) transistor model, and its implementation to design and analyze efficient basic digital circuits like logic gates and arithmetic circuits. These concepts have been experimented through some famous EDA tools like PSpice and Tanner tool. The result demonstrates the effectiveness of these circuits as compared to their conventional counterparts, in the development of ASIC/SOC technology and forces the justification to explore its future potentials and prospects.

RIGHT INFERENCE OF HARDWARE IN HIGH-LEVEL SYNTHESIS

M.Joseph, Narasimha B.Bhat and K.Chandra Sekaran (NITK Suratkal, India)

International Conference on Information processing - ICIP – 2007, Bangalore, India, August – 2007

Date of Publication: 10.8.2207 Pages: 389 - 398.

Abstract: This paper suggests a new methodology to make High-Level Synthesis aware of the target technology, using attribute grammars. It makes the right inference of hardware, by attaching target technology specific attributes to the parse tree. This right inference based on the domain knowledge of a target Field Programmable Gate Array, will guide to generate optimized hardware in terms of power, silicon area and speed.

PERFORMANCE ENHANCEMENTS IN SPI 4.2 IP CORE

Kaushal Buch, Tarang Popat and Rahul Jain, ASIC Engineers, eInfochips Ltd., Ahmedabad, India

Design & Reuse IPSOC 2007 held - Grenoble, France, 5- 6 December 2007

Paper - http://www.us.design-reuse.com/articles/18135/system-packet-interface-spi-4-2-ip-core.html

Presentation - http://www.us.design-reuse.com/ipbasedsocdesign/slides_2007-76_01.html

Abstract: System Packet Interface-4 Phase 2 (SPI-4.2) is a protocol used for data transfer between link layer and physical layer. It is an interface for packet and cell transfer between a physical (PHY) layer device and a link layer device, for aggregate bandwidths of OC-192 ATM and Packet over SONET (POS), as well as for 10 Gb/s Ethernet applications. The SPI 4.2 protocol defines a 311 MHz (minimum) dual data rate (DDR) operation for a 16-bit data bus, effectively yielding a 10 Gb/s data rate. In order to achieve optimum performance, the architecture outlined below does not add any padding data/control packets between two consecutive back-to-back transfers. Also, in order to transfer data efficiently, the architecture incorporates an SPI Performance monitor, which reflects the arbitration status and FIFO status measured over a period of time, which can be analyzed by the firmware. This feature helps the firmware to change the calendar sequence or arbitration logic of a specific port, thus achieving a significant improvement in SPI 4.2 channel utilization. Most of the blocks used in the IP are configurable and can also be re-used in protocol implementation of a similar kind.

REVISITING FIDELITY: A CASE OF ELMORE-BASED Y-ROUTING TREES

Tuhina Samanta, Prasun Ghosal, Hafizur Rahaman (Bengal Engg. & Sc. University, Howrah), and Parthasarathi Dasgupta (IIM Calcutta)

Name of the international journal/conference: IEEE/ACM 10th International WOrkshop on System Level

Interconnect Prediction 2008 (SLIP 2008), Newcastle-upon-Tyne, UK (Pages: 27-34)

Month/Year of Publishing: April 4-5, 2008.

Abstract: The dominance of interconnect delay in VLSI circuit design is well known. Construction of routing trees in recent times has to take care of the timing issues for faster design convergence. Thus there is immense scope of research in design and performance of interconnects. Our current work encompasses two aspects of this research. On one hand, we consider the construction of cost-effective global routing trees with the recently introduced Y-interconnects, and on the other hand, we utilize this framework for verifying the supremacy of the Elmore delay estimate for its high fidelity. In order to ensure accurate computation of fidelity, (i) we propose new statistically proven formulae for fidelity, and (ii) compute the fidelity values based on delay estimates for optimal and near-optimal trees. Our experiments on several randomly generated problem instances and benchmarks confirm once again the supremacy of fidelity of Elmore delay over that of linear delay.

THERMAL-AWARE PLACEMENT OF STANDARD CELLS AND GATE ARRAYS: STUDIES AND OBSERVATIONS

Prasun Ghosal, Tuhina Samanta, Hafizur Rahaman (Bengal Engg. & Sc. University, Howrah), and Parthasarathi Dasgupta (IIM Calcutta)

Name of the international journal/conference: IEEE Computer Society International Symposium on VLSI (ISVLI'08), Montpellier, France, 7-9 April 2008

Month/Year of Publishing: April 6-8, 2008 (One of SIX Best paper Nominees)

Abstract: In high-performance VLSI circuits, the on-chip power densities are playing dominant role due to

increased scaling of technology, increasing number of components, frequency and bandwidth. The consumed power is usually converted into dissipated heat, affecting the performance and reliability of a chip. In this paper, we consider the placement of standard cells and gate arrays (modules) under thermal considerations. Our contributions include: (i) an algorithm for optimal placement of the gates or cells to minimize the possible occurrence of hot spots, (ii) results of sensitivity analysis of thermal characteristic of a layout with respect to the power densities of the modules in the layout, and identifying three classes of modules, and (iii) an algorithm for optimal placement of modules, with minimum possible occurrence of hot spots, and reasonable estimated interconnect lengths. Experimental results on randomly generated and standard benchmark instances are quite encouraging.

PERFORMANCE STUDY OF FIXED VALUE INDUCTORS AND THEIR OPTIMIZATION USING ELECTROMAGNETIC SIMULATOR

Genemala Haobijam and Roy Paily (IIT Guwahati, India)

Name of the international journal/conference: Microwave and Optical Technology Letters, Vol 50, Issue 5, pp 1205-1210

Month/Year of Publishing: May 2008

(www.interscience.wiley.com). DOI 10.1002/mop.23310

Abstract: In this article, we present an extensive analysis of the dependence of quality factor, peak frequency, self resonance frequency, and area of a spiral inductor on its layout parameters, while keeping the inductance value constant as opposed to various studies reported. This performance trend study establishes the optimum metal width and number of turns for a specified inductance value and desired operating frequency. We propose here an algorithm for accurate design and optimization of spiral inductors using a 3D electromagnetic simulator with minimum number of inductor structure simulations, and thereby reducing its long computation time.

Patents

The patents are related to implementations of wireless blocks, and have all gone into silicon.

Patent Number: 7,298,799
Title: ALL-TAP FRACTIONALLY SPACED, SERIAL RAKE COMBINER APPARATUS AND METHOD
Issue Date: 20-Nov-07
Inventor(s): N. Venkatesh, S.D.N. Sailaja, and M.Parthasarathy
Abstract: A decision processor for 802.11b codewords for 1 MB and 2 MB data rates includes a sliding correlator for the acquisition of correlation peaks. During a training interval, these correlation peaks are summed into a channel profile memory. The correlation peaks corresponding to a codeword are added into the channel profile memory, and correlation peaks corresponding to the inverse of this codeword are inverted and added into the channel profile memory during the training interval. After the training interval, a decision interval follows whereby correlation peaks are multiplied by the complex conjugate of the contents of the channel profile memory. The multiplication results are accumulated over a codeword window interval to produce a decision output.

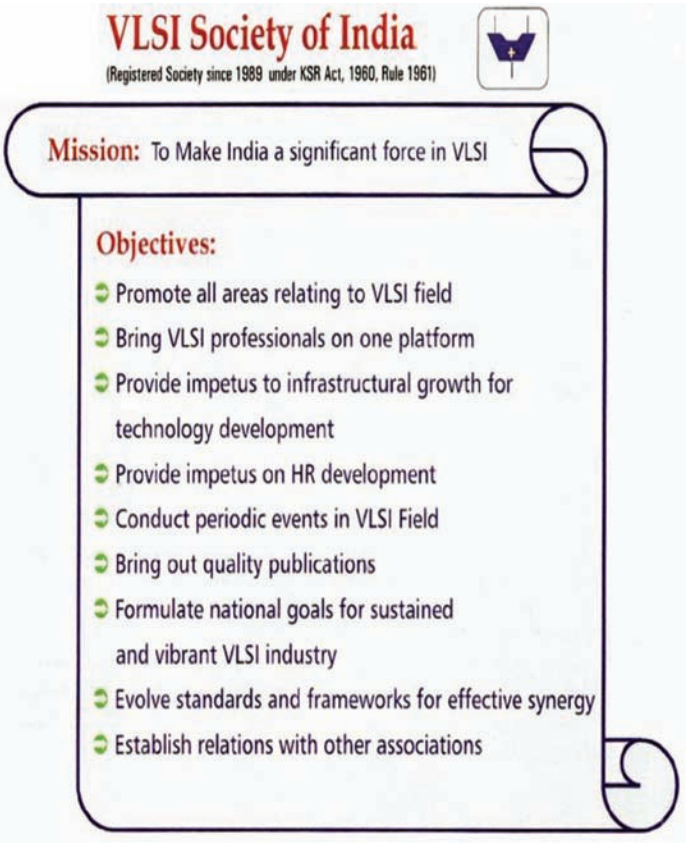
Patent Number: 7,298,772
Title: PACKET DETECTION, SYMBOL TIMING, AND COARSE FREQUENCY ESTIMATION IN AN OFDM COMMUNICATIONS SYSTEM
Issue Date: 20-Nov-07
Inventor(s): N. Ravikumar, N. Venkatesh, and P.V.Chandrasekhar
Abstract: A integrated system for generation of packet detection, symbol timing, and coarse frequency offset for an orthogonal frequency division multiplexed (OFDM) receiver having a stream of input symbols applied comprises a first multiplier performing a multiplication on a delayed and conjugated stream of input symbols multiplied by the input symbol stream. The output of the first multiplier is summed over a symbol length. A second multiplier has an output formed from multiplying the delayed symbol stream by its conjugate, thereby providing a signal strength term Pn. The output of the second multiplier is summed over two symbol periods, and multiplied by a known threshold to form a threshold value. When the magnitude of cn term rises above the known threshold, this generates a packet detect output,

and when the magnitude of Cn terms thereafter falls below the known threshold, this generates a symbol timing output.

Patent Number: 7,296,100
Title: ALL-TAP FRACTIONALLY SPACED, SERIAL RAKE COMBINER APPARATUS AND METHOD
Issue Date: 13-Nov-07
Inventor(s): N. Venkatesh and Satya Rao
Abstract: A memory controller for a wireless communication system comprises a packet buffer write system and a packet buffer read system. The packet buffer write system places packets including packet header and packet data into a packet buffer. The packet buffer read system removes packets including a packet header and packet data from a packet buffer. The packet buffer is arranged into a plurality of packet buffer memory slots, each slot comprising a descriptor status array location including an availability bit set to "used" or "free", and a packet buffer memory location comprising a descriptor memory slot and a data segment memory slot. The descriptor memory slot includes header information for each packet, and the data segment memory slot includes packet data. The memory controller operates on one or more queues of data, and data is placed into a particular queue in packet memory determined by priority information derived from incoming packet header or packet data. Data is removed from packet memory based on which queue the data may be found in. The queues are based on a priority system, where one queue receives priority over another queue for data reception and transmission.

Patent Number: 7,295,144
Title: QUANTIZER RESPONSIVE TO NOISE LEVEL FOR A WIRELESS COMMUNICATIONS SYSTEM
Issue Date: 13-Nov-07
Inventor(s): Karthik Vaidyanathan, Sundaram Vanka, and M.Parthasarathy
Abstract: A quantizer has a plurality of decision blocks, each coupled from input to output, where each decision blocks output generates a binary value that is an unchanged decision block input if the decision block input is below the threshold input level divided by a power of 2, or the decision block subtracts a threshold divided by the power of 2 and passes this result as the decision block output. The quantizer output is formed from the bits of each comparison from each decision block. The threshold is developed from a channel noise variance, which may be multiplied by a scale factor related to coding type and rate. In this manner, a large number of input bits to be quantized may be converted to a smaller number of quantizer output bits, while preserving the dynamic range information required to correctly decode signals passed through a communications channel having multi-path frequency selective fading.

Patent Number: 7,218,896
Title: MULTIPLEXED WIRELESS RECEIVER AND TRANSMITTER
Issue Date: 15-May-07
Inventor(s): N. Venkatesh
Abstract: A baseband receiver having quadrature analog outputs and a plurality of analog control and status signals and a transmit modulator having analog quadrature inputs and a plurality of analog control and status signals are coupled to a transmit processor having a digital output and a plurality of digital control and status signals and to a receive processor having a digital input and a plurality of digital control and status signals by multiplexing analog to digital converters and digital to analog converters such that during a receive time the converters are used for a receive purpose and during a transmit time, the converters are used for a transmit purpose.



The SRC Model for Research Collaboration

C.P. Ravikumar, Texas Instruments

During April 2008, two special visitors were in India - Larry Sumney, President and CEO of Semiconductor Research Corporation (SRC), and Steve Hillenius, Vice President of SRC. Their mission was to spread the awareness about SRC's model of research collaboration. They met several leaders of the semiconductor industry at a meeting held at Texas Instruments India. They visited the Indian Institute of Science, the Indian Institute of Technology Bombay, and the Indian Institute of Technology, Delhi. They also met several senior officials in the Government of India.

The SRC executes a cooperative research effort supported by leading global integrated circuit manufacturers and suppliers. The research is carried out at Universities across the globe. Until recently, the participating Universities were only from North America, but now SRC receives and funds proposals from all parts of the world. Presently, SRC funds four research projects from India – two from the Indian Institute of Science, one from IIT Bombay, and one from IIT Delhi. SRC encourages University Professors from India to submit research proposals. One can begin by visiting their website (www.src.org). Funding opportunities are regularly announced through "Call for Research" on the SRC website. The areas where research proposals are invited are based on the needs of the semiconductor industry. SRC analyzes these needs through active interaction with representatives from the member companies. Initially, a one-page abstract describing the proposed research must be uploaded. A committee creates a shortlist from the submitted abstracts and invites a select group of Professors to submit full proposals. SRC provides funding for supporting the salary of Ph.D. students and travel for attending conferences. Funds towards construction of buildings/ labs and equipment are expected to come from other sources such as the Governmental bodies which provide such funding.

SRC's monumental contribution to the semiconductor industry is the Technology Roadmap for Semiconductors. Initially, this was a National Technology Roadmap for Semiconductors (NTRS) which carved a roadmap for the semiconductor industry in USA. Later, SRC worked on the International Technology Roadmap for Semiconductors, as many countries such as China and India became significant forces in semiconductor research and development. ITRS is the result on

Deepak Bhardwaj (TI), Bobby Mitra (President, VSI), C.P. Ravikumar (Secretary, VSI), Larry Sumney (President and CEO, SRC), Steven Hillenius (Vice President, SRC), and Sham Banerjee (TI)

hundreds of experts and visionaries who laid out the growth plan for the semiconductor industry. Without such a roadmap, it would have been impossible to witness the dramatic developments in the semiconductor industry, that we have seen over the past two decades. In fact, as Larry points out, the availability of the roadmap gave the companies a challenge to not only meet the guidelines set by the roadmap, but to out-do. This is why we often saw some technology nodes appear a little earlier than the predictions.

It is often said, in a humorous note, that the only thing that is difficult to predict is the future. Larry also likes to quote an American baseball player Yogi Berra - "You've got to be very careful if you don't know where you are going because you might not get there." SRC divides semiconductor research into three classes – near-term, medium-term, and long-term. These are handled by GRC (Global Research Consortium, which invites proposals from Universities world-wide), FCRP (Focus Center Research Program), and NERC (Nanoelectronic Research Consortium). Indian Universities can submit proposals to the Call for Research published regularly by GRC.

SRC completed 25 years of service in 2008 and is the proud winner of the National Medal of Technology in USA in 2005. You can learn more about SRC by visiting their website.

2007 Turing Award for Formal Verification

Adapted from an article that appeared in Dr. Dobb's Portal
(http://www.ddj.com/206103622)

The prestigious Turing award for 2007 has been given to Edmund M. Clarke, E. Allen Emerson, and Joseph Sifakis for their work on formal verification. Their work enables an automated method for finding design errors in computer hardware and software. Edmond Clarke is a professor at Carnegie Mellon University, USA. Allen Emerson is a Professor at the University of Texas, Austin, USA, and Joseph Sifakis is a Professor at the University of Grenoble, France. The award is given annually by the Association for Computing Machinery (ACM) to honor researchers who have made path-breaking contributions to Computer Science. The award, popularly known as the "Nobel Prize of Computing," is named after the British mathematician Alan Turing, who is regarded as the father of Computer Science. See http://en.wikipedia.org/wiki/Alan_Turing for a sketch on the life and contributions of Alan Turing.

Today, Model Checking is a widely used technique for detecting and diagnosing errors in complex hardware and software design. The use of this formal technique helps in improving the reliability of complex integrated circuits, systems and networks. Mathematicians like a formal proof for a statement that someone claims to be true; if the statement is false, a counter-example is presented. For example, if we claim that all numbers of the form 2n+1 are prime, a counter-example can be produced for the case n = 4. Formal proof techniques are based on techniques such as mathematical induction, proof by contradiction, and so on. Model Checking analyzes the digital logic underlying a design to prove or disprove that a theorem is correct. Far from hit or miss, Model Checking considers every possible state of a hardware or software design and determines if it is consistent with the designer's specifications.

Clarke and Emerson originated the idea of Model Checking at Harvard in 1980 (E. Allen Emerson, Edmund M. Clarke: "Characterizing Correctness Properties of Parallel Programs Using Fixpoints". ICALP 1980: 169-181.) They developed a theoretical technique for determining whether an abstract model of a hardware or software design satisfies a formal specification, given as a formula in Temporal Logic, a notation for describing possible sequences of events (Edmund M. Clarke, E. Allen Emerson: "Design and Synthesis of Synchronization Skeletons Using Branching-Time Temporal Logic". Logic of Programs 1981: 52-71.) Moreover, when the system fails the specification, it could identify a counter-example to show the source of the problem. Several commercial tools for model checking exist today.

Clarke implemented the first Model Checker in 1982. It could analyze all the possible states of a given circuit, but was limited to relatively small designs — much smaller than the systems being built by computer manufacturers. In 1987, Clarke's graduate student, Kenneth McMillan, implemented Model Checking by a series of operations on a data structure called binary decision diagram (BDDs), which was proposed by Prof. Randal E. Bryant of Carnegie Mellon University. This new system, called "Symbolic Model Checking," was able to analyze billions of billions of states, making it relevant to commercial computer design problems and leading to its widespread adoption by the industry (*Symbolic Model Checking*, Kenneth L. McMillan, Kluwer, ISBN 0-7923-9380-5.). For this invention, Bryant, Clarke, Emerson and McMillan won the 1998 Paris Kanellakis Award for Theory and Practice from the ACM. In 1999, they also received the Allen Newell Award for Research Excellence from CMU.

"As Processing Becomes Digital Intensive, Systems Will Require More Analogue Content"

Interview with Dr. Biswadeep (Bobby) Mitra

Reproduced from *Electronics For You Magazine,* November 2007 edition, Page 157-158

DR BISWADIP (BOBBY) MITRA
MANAGING DIRECTOR, TEXAS INSTRUMENTS (INDIA) PVT LTD

Dr Biswadip (Bobby) Mitra, managing director of Texas Instruments (India), leads all of TI's marketing, sales and R&D activities in India across all product domains. Under his leadership, Texas Instruments won several awards including the 'Most Innovative Company in India' (in terms of US patents filed) and ranked No. 1 in the 'Great Places to Work' survey conducted by Grow Talent and Business World.

Dr Mitra speaks to EFY's Swapnil Bhartiya about the trends in semiconductor industry and

Q: What's the future of the Indian semiconductor industry?

The Indian semiconductor market is growing rapidly at a compounded annual grwoth rate of 36 per cent. A recent report by ISA-Frost & Sullivan says that the total available market (TAM) will grow from $1.74 billion in 2007 to $3.18 billion in 2009. The TAM for analogue ICs will rise sharply to $437.2 million in 2009 from $141.7 million in 2006. The TAM for digital signal processors and microcontrollers is forecast to be $295.5 million and $123.6 million, respectively, in 2009.

Q: What is driving this growth?

Broadly, two factors are driving the growth in the Indian industry. The first relates to the overall improvement in the macroeconomic, investment and regulatory climate. Rising consumer affordability and current low penetration have been key to the growth in the wireless, consumer and automotive industries. Regulatory trends are driving growth in areas like DTH/IPTV transmission and medicine, respectively. Increased investment in areas like power, telecom infrastructure, defence/ aerospace and retail are also fueling growth in these areas.

The second growth driver is technology. Advances in analogue technologies (for example, data converters, power management, amplifiers, interface chips, etc), low-power microcontrollers and digital signal processors (DSPs) are driving growth across every domain-industrial, medical, consumer, wireless, etc. This is helping OEMs innovate by bringing in more differentiated features, flexibility and product efficiency to their markets in a cost-effective manner.

Q: Which verticals in India will help push the growth?

Industrial electronics is a key vertical. According to the ISA-Frost & Sullivan report, this will be a $319.5-million market (in terms of TAM) in 2009. Some of the key products are energy meters (single-phase and three-phase), UPS (offline and online), inverters, stabilisers, lighting, weighing scales and water purifiers. Most of the manufacturing of these products is from India. We are also seeing growing focus in renewable energy (wind, solar and fuel).

The wireless growth is likely to accelerate further. Increased consumer orientation towards a rich personal experience (music, games, images, etc) will drive a higher penetration of feature phones. Likewise, the consumer electronics market (such as satellite and IP set-top boxes and colour TVs, especially with rapid growth in LCD TVs) is growing rapidly-with the 2009 TAM forecast at $240.4 million.

For automobiles, the semiconductor opportunities include capacitor discharge ignition units, flashers, regulators, instrument clusters, engine management systems, engine control unit and body electronics (wipers, power windows, remote keyless entry, anti-lock braking system and immobilisers).

Use of portable medical equipment at home (blood glucose meters, blood-pressure monitors, etc) or at the hospital (portable ultrasound, etc) will be another increasing trend. Advances in low-power semiconductor and imaging technologies will provide an impetus to several medical applications.

Q: Talking about the role of TI India, can you share its key innovations with us?

A large number of products have been designed by the TI India centre in the last 22 years. In fact, today, there is hardly any chip produced by Texas Instruments that is not touched by TI India in some fashion. This includes products for wireless handsets, infrastructure, video and imaging, industrial applications, etc.

In addition to several strong product innovations from our TI India centre, we have been very pleased with the excellent innovations from several of our partners. Over the last couple of decades, TI has worked with over 50 very innovative companies in India as part of our ecosystem. These companies

have influenced nearly 500 customer product designs worldwide across an array of applications such as next-generation video phones, video surveillance cameras, portable media players, portable medical instrumentation and digital motor control.

It is also very exciting to see strong product and system innovations by OEMs in India-both local and multinational. Leveraging the right semiconductor and software solutions, they are developing innovative products for India and export.

Q: What attracts TI more, the development talent or the growing sales potential of India?

TI India will always remain a significant contributor to our products globally. Our R&D teams in TI India employ some of the best engineering talent in the country. We will continue to strive for world-class excellence in R&D with products that are targeted to our customers worldwide. This has been our focus over the last two decades, and will remain fundamental to our future.

Q: In technology, the world is going digital. What is the importance of analogue then?

The digital world offers immense possibilities in terms of speed and processing power. However, the ultimate human interface is always analogue. In other words, as processing becomes more digital-intensive, systems will require more analogue content to pipe in and out the signals, to amplify, to power, to interface, etc.

Examples of analogue solutions are analogue-to-digital converters, digital-to-analogue converters, amplifiers, and power management and interface chips. These complement the DSPs or microcontrollers in the system.

Q: The analogue market opens up big opportunities for TI. How do you see yourself growing in this space?

With a comprehensive portfolio and diversity of analogue products across application areas, we expect to play a very important role in this space. Most importantly, leadership in analogue requires a close working relationship with our customers to understand their requirements and provide application support.

Q: Why power management assumes so much importance?

In an environment that is increasingly conscious of energy issues, power management assumes significance in every area of electronics-whether it is wall-powered or battery-powered. It includes increasing the conversion efficiency (from input to output) and power quality, smart technologies that increase the product differentiation/features while not increasing the power consumption, etc.

Efficient conversion of power means less power consumed from the utilities. If you notice, the size of the battery has not gone up significantly over the last few years, yet today one has FM radios, cameras, e-mails and a plethora of other features available on handheld devices. Advances in power management technology have greatly enabled vendors to incorporate these features with far fewer drawbacks. This also helps the worldwide initiative of 'Green Earth.'

TI's green-mode controller (GMC) when integrated in your cellphone charger will prevent it from drawing power from the wall in idle state. GMC is a power management chip with inbuilt advanced energy-saving and high-level protection features to provide cost-effective solutions for energy-efficient power supplies. It supports AC/DC adaptors, LCD and digital TVs and is programmed to reduce the operational frequency in 'light load' and 'no load' operations. The GMC is used in telecom, medical, industrial and computing applications.

TI's SmartReflex technologies also help in efficient use of power. These include a broad range of adaptive hardware and software techniques that dynamically control voltage, frequency and power based on device activity, modes of operation and temperature.

Q: Your plans for this space?

Power management is a key focus area for TI globally. TI is the top provider of power management integrated circuits in the industry with 15 per cent market share in 2006 as per a report by Databeans. iSuppli also ranked TI No. 1 with 15 per cent market share in voltage regulator/reference products in its 2006 Annual Semiconductor Market Share report.

The total power management market exceeds $6.9 billion globally, and is expected to reach nearly $10.7 billion by 2009. ISA-Frost & Sullivan India forecasts the power semiconductor market in India to grow from $46.2 million in 2005 to approximately $375 million in 2015 its terms of revenue.

Q: Coming to wireless technologies, what are the biggest challenges?

Subscribers are looking for increased capabilities to suit their personal needs. The consumer today is increasingly conscious of features like music, games, Internet access, Bluetooth, etc, while not compromising on the battery life. This provides an opportunity to semiconductor players, OEMs/ODMs, design houses, operators and ISVs alike to develop compelling technologies.

Q: How prepared is TI for next-generation wireless technologies?

TI is focused on technology innovation that enables nextgeneration wireless technologies. Our portfolio of products provides the complete spectrum of solutions. Our OMAPV1035 eCosto single-chip EDGE solution enables affordable multimedia-rich devices with capabilities like up to 3-megapixel camera, high-quality audio and video including streaming, 3D games, Bluetooth and Wi-Fi connectivity, and digital TV reception. On the other hand, the LoCosto line of chips ensures affordable, feature-rich phones with colour display, music, etc. For increased multimedia and productivity, TI's leadership OMAP3 application platform provides unparalleled performance.

Q: The mobile phone market in India is at an inflection point. How do you address the challenges (technological and otherwise) thrown up by this market?

India has a large cellphone subscriber base ranging from entry-level to high-end. TI provides a diverse range of solutions to cater to this market. Our solutions can address both the voice as well as the value-added requirements (with affordable multimedia-enabled phones that provide voice, text, music, video and gaming through LoCosto and OMAP-Vox family of products).

DATE 2008 – A Conference Report

C.P. Ravikumar

I attended the DATE 2008 conference (Design Automation and Test in Europe) held in Munich, Germany, during March 10-14, 2008. Munich was cold, with strong gusts of cold wind, but there was no snow on the streets, a phenomenon that people attribute to global warming. The organizers expressed happiness over the good attendance in the conference – my estimate would be well over a thousand participants — from all parts of the world.

With five parallel tracks, it is not easy to choose what you want to attend in DATE. I attended the keynote talks and several technical sessions. The keynote by Prof. De Micheli (Stanford) was on how the future research in Electronic Design Automation should be directed. He hinted on how problems similar to those in EDA manifest themselves in the society, and researchers are missing out on opportunities at the system-level. He prodded the EDA community to move from the system-on-chip domain to the much larger domain of distributed embedded systems. The areas that Prof. De Micheli mentioned are - breaking language barriers and connecting all the people on this planet, providing safety to everyone, better health care, protection of the environment and elimination of the dependence on non-renewable sources of energy. He stressed the need for powerful data processing algorithms and software that will become necessary when the EDA community takes on these challenges.

Dominuqe Vernay (Thales) presented a keynote talk on the industrial and research challenges of the Embedded Systems. He noted that we build the electronics in cars and aircraft whose life expectancy is 10 to 25 years with components whose life expectancy is 5 to 10 years. This problem can only be solved through redundancy and software that can hide the faults. He also stressed on the importance of middleware in developing distributed embedded systems – middleware is necessary to take away from the programmers the tedium of writing the code for networking and messaging, hence permitting them to focus on the application at hand.

An entire day of technical sessions on Automotive Systems was organized by Prof. Alberto Sangiovanni Vincentelli (Berkeley). The session on Physical Architectures focused on advances in electronic automotive architectures. Forest (General Motors) provided an overview of the FlexRay communication system that supports higher data rates and is fault-tolerant in comparison to the CAN architecture. Alberto Ferrari (Parades) stressed on the importance of reliability, availability, and safety in automotive electronics. He described various ways to achieve these goals, starting from technological solutions to TMR flip-flops to self-checking hardware to CPU and ECU redundancy. Audisio (Pirelli) spoke about new opportunities for sensor networks in the area of making automotive tyres safer. Tyre Pressure Monitoring Systems (TPMS) make use of pressure sensors that are embedded in the tyres. To my query about whether this would increase the cost of the tyres, Prof. Vincentelli quoted the going price of car tyres, which is in excess of $200, which means the addition of sensors may not be such a burden after all!

I attended a panel discussion on how EDA strategies would change in a fab-less or fab-lite era. This was organized by Antun Domic of Synopsys and was moderated by Richard Wallace of EE-Times (Europe). Panelists from Xilinx, ST Microelectronics, NXP, and Synopsys debated on the topic. There seemed to be general concurrence that adopting a fab-less or fab-lite may not take away the differentiation from the chip vendors, since the underlying IP and the architectural and algorithmic innovations have a major contribution to cost, performance, and power. Antun Domic felt that a fab-lite strategy does not always reduce cost. He quoted statistics about a fab-lite company that spends 21% of its profits on 45 nm R&D, as opposed to a fab owner who spends only 15%. He felt that this anomaly can only be fixed when design houses collaborate closely with EDA partners.

Another panel discussion on the Perils of 45 nm generated an equal amount of interest among the participants. Anil Jain (Cavium) outlined the perils of variability and leakage power in 45 nm – e.g. transistor width variation can result in 40% variation in Id,sat, and leakage of transistors that are at 100 degrees Celsius can be 3X compared to those that are at room

temperature. Ted Vucurevich revealed that unlike what can be expected, companies are adopting 45 nm technology faster and some are skipping the 65 nm node. This is because of the increased complexity of integrated circuits e.g. systems-on-chips for set-top boxes. He felt that statistical timing analysis may not be needed at 45 nm to manage variability, and that the real challenge will be in managing the software costs for these complex systems. Rudy Laureins (IMEC) stressed the importance of modeling variability in simulations and system-level techniques for yield prediction.

I attended several technical paper presentations in areas of my own interest, and found most of them to be highly engaging. The technical sessions were packed on all days, and the speakers were well rehearsed. I participated in a "Hot Topic" session on Low Power Testing, which was organized by Patrick Girard (LIRMM, France). My co-presenters were Xiaoqing Wen (Kyushu Institute of Technology, Japan) and Mokhtar Hirech (Synopsy, California). Power dissipation in the test mode can indeed make the chips hot, and the title "hot topics" was justified! What was more, the session was packed and generated heated debate!

The exhibits, which were perhaps over a hundred in number, also attracted significant interest among the participants. Book exhibitions by publishers were drawing a crowd, with several new titles in hot areas such as Design for Manufacturability, RF Design, and System-level Design and Verification.

There were many opportunities for social networking during coffee breaks and lunch. Although the vegetarian lunches were not so memorable, the conversations with colleagues seated at the lunch table were certainly so! For those of you who are thinking of attending DATE next year, it will be held in NICE, France.

News - Indian Government to encourage publicly funded universities to commercialize innovation

Now, professors to turn entrepreneurs

Reproduced from *The Economic Times*: May 19, 2008

New Delhi: In a move that would transform knowledge professionals into entrepreneurs, the government plans to allow professors and research scholars to set up commercial entities while being employed in academic institutes. Academics will also be allowed to invest their knowledge and skills to pick up equity stakes in companies. For instance, a scholar may offer his skills and knowledge to a company to pick up equity in it.

The model is on the lines of the ones followed at renowned institutions such as Massachusetts Institute of Technology, Stanford and University of Cambridge. The scheme would help central universities and premier institutes such as IIT, IISc, NIT and JNU attract talent.

A Cabinet note in this regard is already in circulation. Under the law, academics and institutes, including government-promoted societies, availing income-tax benefits are not permitted to pick up equity stakes in commercial ventures.

Confirming the move, an official in the ministry for science & technology said: "The move follows the prime minister's direction to encourage development and commercialization of innovations." The government may also exempt researchers working in publicly-funded research organizations and universities from central civil services (CCS) conduct rules, enabling them to set up companies while continuing in government service.

"Private institutions such as Amity have started encouraging such moves to attract and retain talent. The proposed scheme would help government-funded institutions encash their knowledge," said an official in the department of Information Technology. Amity group has recently set up the Amity Innovation Incubator (AII) in Noida.

The incubator will forge tie-ups with industry. Even government institutes such as CSIR, IISc and IITs have devised mechanisms to start incubation centres to nurture start-up companies and give the students a first-hand experience in entrepreneurship.

The move is in line with the finance ministry's proposal to allow government-promoted societies to invest in private sector equity. The proposal, mooted in 1997, could not be implemented due to strict income-tax regulations.

Press Coverage for VSI Activity
Researcher's methodology eases VLSI-layout updates

K.C. Krishnadas, EE Times
(12/13/2007 10:53 AM EST)

BENGALURU, India — The time-consuming process of recompiling designs from scratch after every update in traditional CAD design is a function not only of the size of the update, but also of the new layout size. The updates may be local, affecting only small parts of the layout, but the entire layout must be recompiled, and incremental algorithms are needed to cut design cycle time. Now, a researcher here has outlined a method to ease the process, especially when larger VLSI layout sizes do not fit into the main memory.

The algorithms that search for parts of the layout affected by the update and that give the result of the updates are hampered when the layout is so large that it cannot fit into the available main memory. The main performance bottleneck here is the communication between fast internal memory and slow external memory. Hence the need for algorithms and data structures that can tap external memory management to reduce external memory access and, therefore, the I/Os between main and external memory.

To address the problem, Akash Agrawal of the Algorithms and Computation Theory Laboratory at the International Institute of Information Technology, Hyderabad, champions an I/O-efficient and output-sensitive external-memory algorithm for incremental connectivity extraction. The algorithm is based on a recursive tiling approach that Agrawal claims enables an easy-to-implement data structure for the aggregation of parts of the layout for fast search and updates.

"Traditionally, algorithms and data structures are designed assuming that there is a large amount of memory available, which requires constant time per access to any memory location. But this assumption may not be true in practice," Agrawal notes in a paper describing his approach. "While the memory hierarchy of a computer system can be divided into CPU registers, several levels of cache, RAM (main memory) and hard disk (external or secondary memory), there are many applications, including those of VLSI layout editing, that require such a large amount of data to be processed that it cannot fit into main memory.

"For processing data sets that cannot be fit into main memory, the bottleneck is the communication between the internal memory (RAM) and the external memory (disk), instead of the internal computation time, as accessing the data from secondary memory is a million times slower than that from main memory. To process such large amounts of data, we need algorithms and data structures that can reduce the amount of data accesses from the external memory and, hence, are I/O-efficient."

Main-memory size continues to rise, but at a far lower rate than the size and complexity of VLSI devices. Thus VLSI tools must consider external-memory management. "In the incremental setting, we have to search and update the parts of the layout [affected by] the incremental changes; but if the size of layout is so large that it cannot fit entirely into main memory, we have to search the secondary memory for the portions of the layout that have to be modified, and load those portions into main memory from secondary memory. So we need an external memory algorithm for incremental changes for large layouts," Agrawal argues in his paper.

"The problem of incremental connectivity extraction is to report on the changes in connectivity information due to incremental updates in the layout," he adds. "An incremental update can be either an insertion or a deletion of a polygon. The resultant change can be an instance of a short-circuit or an open circuit in the layout. More formally, the online connectivity extraction can be defined as follows: Preprocess the given layout such that on insertion or deletion of a polygon in the layout, the change in connectivity can be reported efficiently. A dynamic or incremental algorithm, which requires updating the connectivity in the presence of insertion and deletion, is very useful for layout editors.

"A net-list is associated with each design, and each net can be thought of as a signal and is associated with a unique net ID. Assuming that each polygon is attached with the net ID of the net to which it belongs, the notion of short-circuits and open circuits in the layout can be defined.

"If two polygons originally on different nets belong to the same connected component, the nets are electrically connected—an instance of a short-circuit—and the two nets are said to be shorted. If two polygons originally on the same net belong to different connected components, it shows a break in electrical connectivity of that net and is an instance of an open circuit."

The electrical connection in the layout is made using the metal and via (or contact) layers. The polygons of the two metal layers are connected through a polygon via layer between the two metal layers. While Agrawal's paper considers only two metal layers and one via layer in between them, the same approach can be extended if there are more metal and via layers.

Agrawal uses a generalization of the recursive tiling method of partitioning that he says is easy to implement and update. It also provides for an efficient mechanism for extending the main-memory application to external memory, as any existing main memory can be used to process the tiles.

The method was implemented and tested against main memory on a line-connectivity-extraction algorithm. The implementation used the STXXL package, which provides an I/O-efficient extension to standard C++STL vectors, along with other data structures.

Binary search was used in the main-memory algorithm to implement incremental changes to find portions of the layout to be updated. The experiments were conducted on a 3-GHz Pentium IV processor with 512 Mbytes of RAM.

VSI Calendar

AUGUST 2008

Seminar on DSP

August 18-20, 2008, VNRVJIET Campus, Hyderabad ... Details to be announced

Short Course on Digital Circuits Test and DFT

Presenters: Dr.Nilanjan Mukherjee, Mentor Graphics Corporation, USA; Prof. Sudhakar M.Reddy, Iowa Univ., USA, Dr. C.P. Ravikumar, Texas Instruments India

August 11-14, 2008; Hyderabad ... Details to be announced

JULY 2008

12th VLSI Design And Test Symposium - VDAT2008

July 23-26, 2008; Wipro Campus, Electronics City, Bangalore

3rd Workshop on Custom LSI Design - CLDW2008

Conducted by: Dr.Mahant S.Shetti, and KarMic Team

July 28 - Aug 8, 2008; Kudalsangam. Bagalkot Dist, Karnataka

One-day workshop on Design for Manufacturability

Conducted by Sandip Kundu, Professor of Electrical and Computer Engineering at University of Massachusetts, Amherst

July 7, 2008, Bangalore

JUNE 2008

Three-day Workshop on Audio Codecs and Data Converters

June 16-18, 2008, Jadavpur University, WB India

Organized by VLSI Society of India, in cooperation with Jadavpur University, and IEEE Calcutta Section

Co-sponsored by Texas Instruments India and Tata Consultancy Services

APRIL 2008

4th Workshop on Design Verification Methodologies - DVM2008

April 25-26, 2008; Bangalore

The calendar is tentative – more events may be announced. If you wish to receive information about these events, please become a member of the mailing list (vdat@yahoogroups.com).

2nd International Workshop on Interconnect Design and Variability

December 13-14, 2007, Bangalore

A report by C.P. Ravikumar

Interconnects continue to remain a challenge for VLSI designers, and especially so in the sub-90 nm era. On-chip variability of process parameters, temperature, and voltage create further difficulties during chip design, validation, and testing. VLSI Society of India organized a two-day workshop on Interconnect Design and Variability during December 13-14, 2007 at Bangalore. The event, organized by VLSI Society of India was supported by IEEE-CAS Bangalore Chapter, and was sponsored by Cadence Design Systems.

The event began with an introductory talk by Nagaraj N.S., TI Inc., and C.P. Ravikumar, TI India on *Interconnect Design and Variability in Nanometer Era*.

In the morning session, on behalf of Juan C. Rey, Mentor Graphics Corporation, Srinivas Mandavilli, Mentor Graphics India, spoke on *Big Challenges for the Semiconductor Industry: Bridging Design and Manufacturing*. Prof. Kazuya Masu, Tokyo Institute of Technology, presented a talk on *On-Chip Global Interconnect Using Transmission Line*. Ersed Ackasu, OEA International Inc., spoke on *Interconnect Parasitic RLC and delay Variability below 90nm, Physical Origins and its Impact on the Future Geometry Scaling*.

The afternoon session had Noel Menezes, Intel Corporation, speaking on *Interconnect variability - A front-end perspective*. Prof. Sachin Sapatnekar, University of Minnesota, spoke on *Thermal Challenges in Integrated Circuit Design*. Tom Williams, Synopsys Inc, talked about *Quality now Requires -small delay fault model*.

The day ended with a panel discussion on *Managing Variability - should it be a Design Issue or a Test Issue?*. It was moderated by C.P. Ravikumar. The participants included Nagaraj N.S., Erced Ackasu, Noel Menezes, Sachin Sapatnekar, and Tom Williams. The topic of the panel was selected to create a lively discussion on who owns the responsibility of solving the problem of variability – is it the technologist/manufacturer, the EDA developer the library/IP designer, the chip designer, or the test engineer. Panelists gave their perspectives on the topic, but agreed that it is a collective responsibility of everyone to address the challenges posed by variability.

The second day began with a presentation on *Process-aware Timing and Power Analysis and Optimization* by Steffen Rochel of Blaze DFM Inc.. Nishath Verghese and Atul Sharan, Cadence Design Systems; spoke on *Addressing pattern-dependent variability in design using model-based DFM tools*. Nagaraj, N.S., Texas Instruments Inc., Dallas, Palkesh Jain and Gautam Kapila, Texas Instruments India covered *Design-In-Reliability for Interconnect*.

In the second session, Madhav P. Desai, IIT Bombay,

Vish Sundararaman, TI Inc., and Vish Visvanathan, TI India

Panel discussion

and Vani Prasad, Freescale Semiconductor covered *On the use of standardized interconnect in VLSI Systems*; Vidyasagar Ganesan, AMD, spoke on *Clocking in GHz designs*, with Vish Sundararaman, Texas Instruments Inc., Dallas focusing on *Interconnect Design – Packaging Perspectives and Considerations*.

The day ended with a panel discussion on *VLSI Design in the Nanometer Regime – Is Prevention better than a Fix?*.The panelists included Nishath Verghese, Palkesh Jain, Vidyasagar Ganesan, N.S. Nagaraj, Venugopal (Qualcomm), and Vish Sundararaman. The panel was moderated by Vish Visvanathan of Texas Instruments, Bangalore. A detailed report on this panel discussion appears in this issue of VSI VISION.

VSI likes to thank Cadence Design Systems for sponsoring the event. The workshop proceedings that include the previous workshop IDV2006 additionally is available in CD form. Write to **vsisecy@vlsi-india.org** to purchase a copy.

VLSI Design in the Nanometer Regime – Is Prevention better than a Fix?

A VSI Panel Discussion

Report by C.P. Ravikumar

At the second International Workshop on Interconnect Design and Variability (IDV 2007) held in Bangalore (Dec 13-14, 2007), a panel of experts debated the question of whether prevention is better than a post-silicon fix for the nanometer chips. The panelists were Nishath Verghese (Cadence), Steffen Rochel (Extreme DA), Palkesh Jain (TI), Vidyasagar Ganesan (AMD), and Erced Ackasu. The panel was moderated by Vish Visvanathan of TI. "Prevention" refers to careful design which includes closure against various checks – signal timing, clock timing, signal integrity, power, reliability, testability, and manufacturability, to name a few. Point solutions for applying the checks and making design fixes are becoming available, but to attain a flow that achieves a "Nash equilibrium" remains elusive. If a brave designer risks ignoring some of the design rules, what silicon issues is he really likely to see? Is there evidence today to justify such a defensive design methodology which may leave some optimization on the table? Is it better to take the risk and do post-silicon fix to correct timing and power problems? For example, solutions are emerging to integrate on-chip sensors for making measurements and tune the clock-tree. There are also companies, which invest heavily in silicon validation, where test chips are made and post-silicon learning is integrated in the design.

Nishath Verghese of Cadence felt that both approaches are required to succeed in the nanometer era – use a conservative design style in the early stages of ramp-up, and relax the constraints to gain optimization in high-volume production. The "correct by construction" approach is difficult, if not impossible. Vidyasagar agreed with Nishath by adding that it is difficult to fathom all the sources of variability up-front. Palkesh felt that the right solution would depend on the cost and schedule. High-volume yield would also be an important consideration in selecting the right approach.

Venu Puvvada (Qualcom) felt that designers often rush to embrace the latest without understanding the practical implications. For example, in the aluminum era, having peak current density constraints for preventing electromigration in signal lines was an overkill. Vish wondered if we are overreacting on reliability by considering 20-odd failure mechanisms, some of which may not be serious threats. Palkesh felt that learning from silicon is not an option when cost and schedule are tightly constrained.

Erced pointed out that design discipline and a deep understanding of physics is perhaps more important than all the CAD tools. He quoted the example of a PLL design which failed because the power line resistance was 50 ohm. Steffen agreed and related his experience with designers who did not practice basic discipline in data management which are bare essentials in a design environment! Ravikumar (TI) asked the panelists what today's VSLI/CAD courses must include in the curriculum – can all the bewildering array of deep-submicron design issues be taught in the classroom? Nagaraj (TI) felt that it is the fundamentals that need to be emphasized in the schools. Vidyasagar felt that schools should regularly have speakers from the industry to expose the students to reality. Availability of industrial case studies to colleges and sharing of success stories will also help the situation.

4th Workshop on Design Verification Methodologies

April 25-26, 2008, Bangalore

A report by P. Sakthivel,
Anna University, Chennai – 600 025

VLSI Society of India organized the fourth Workshop on Design Verification Methodologies during April 25-26, 2008 at Bangalore. The venue was The Capitol Hotel, Bangalore. This two-day workshop was a forum to discuss the new methodologies and current practices in VLSI Design Verification. About 50 participants from industry and academic institutions attended the Workshop.

The workshop began with inaugural and welcome addresses by Dr. C. P. Ravikumar, secretary of VSI, who highlighted the success of the series of *Workshops on Design Verification Methodologies* organized by the VLSI Society of India during the past three years. He also mentioned the importance and motivations of this fourth workshop. The complete technical program of the workshop can be viewed at the VSI website (http://vlsi-india.org/vsi/activities/) under the "Events" tab. The presentations made at the workshop are also available on a CD published by the VLSI Society of India.

The first day started with a keynote talk by Professor Pallab Dasgupta of Indian Institute of Technology, Kharagpur on *Model-Driven Integration - Putting together the bits and pieces of verification*. He talked about the dominance of verification in design and highlighted the importance of divide-and-conquer technique at different levels of abstraction in the verification process. The keynote talk included aspects of inter-domain verification issues, integrated early analysis, Model driven integration, challenges and different domains of verification, verification methodologies, generic challenges in web service verification, and the verification group profile.

The second session was on *Low Power Verification* by Abhijit Ray of Cadence Design Systems. He discussed the need for low power, significance of low power techniques, design, verification and implementation of low power techniques.

Holistic Verification: Myth or The Magic Bullet was title of the third session by Dr. Pradip Thaker of Analog Devices India. He discussed the key components, mission and metric of design verification. He illustrated the design methodology to aid verification and introduced the concept of design for verification. He talked about

Ansuman Banerjee, Interra Systems

Raj Mitra, TI India

the evolution of verification methodology, simulation based verification methodology, reference model based verification methodology, assertion based verification methodology and power-domain simulation for verification.

Dr. Srinivasan Venkataramanan of Synopsis India spoke about the *Need for a methodology in Functional Verification* in the fourth technical session. In this talk, he discussed the recent developments and exponentially growing challenges of verification, typical verification flow, tools used in the verification flow, complete design verification with System Verilog, design verification components and methodology applied to the verification.

Session five was on *Realizing Design for debug infrastructure in complex SoC* by Dr. Haridas Vilakathra of NXP Semiconductors. He started by discussing the evolution for design for debug and major requirements of DfD. He also discussed about Hyper JTAG, Silicon debug trends, OCP-IP standardization, debug security option and Infineon Multi-core debug solution.

The sixth and final session on the first day was on *Verification Re-Use in RTL and SystemC IP* by Dr. Aniruddha Baljekar of NXP Semiconductors. He gave an overview of the verification environment and methodology to enable re-use across different levels of abstractions.

The programmes on the second day of the workshop started with the keynote talk on *Verification of Clock Domain Crossing in Today's complex SOCs* by Dr. Kaushik De of Synopsis India. In his talk, he introduced the Clock Domain Crossing, The Metastability Problem, Various design styles for clock domain crossing and listed the detailed CDC Verification steps.

The second session was on *Coverage Driven Verification* by Gurudutt Bansal of Cadence Design Systems. He highlighted the different aspects of verification planning, coverage metrics, coverage flow and high-level architecture of a Coverage driven Verification solution.

Verification methodologies for Analog Design Modules/Blocks was the topic of the third session by Prabhat Agarwal of Sankalp Semiconductor. He outlined the different devices in the era of communication and the IC design flow. Technology in the communication era, Mixed signal VLSI Design flow and challenges, Analog/ Mixed Signal Verification were discussed during this talk.

Dr. Ansuman Banerjee of Interra Systems India talked in the fourth session on *Increasing dynamic assertion-based verification productivity with formal techniques for compositional coverage analysis*. He discussed the reality in system design, reality of system verification, Taxonomy of verification, Historical perspective of verification solutions, simulation based verification, formal verification, advantages and limitations of formal verification and Dynamic property verification.

The fifth session was on *Systematic Approach for Verification of Complex SoC* by Badri Seshadri of NXP Semiconductors. The talk provided an verview of Multimedia Domain and the associated verification challenges, verification methodologies and verification environment.

The two-day workshop came to a conclusion with an interesting and interactive panel discussion on *Verifying Monster SOC – Whose job is it anyway?* The moderator for this panel discussion was Dr. Raj Mitra, Texas Instruments, Bangalore. The issues addressed in the panel discussion were *How and where should the verification job be partitioned*? The panel focused on 1) IP vs SoC teams, 2) Design Vs Verification teams, 3) Hardware vs Software teams, 4) Inhouse vs Outsourcing options. The panel members were Ish Dham, Texas Instruments, Dr. Pradip Thaker, Analog Devices, Gurudutt Bansal, Cadence Design Systems, Srinivasan Venkataramanan, Synopsis India, Giri Raju, Wipro Technologies, and Sundaresan Kumbakonam, Broadcom India.

ANSWER TO CROSSWORD PUZZLE – 6

■	1B	U	2C	K	3C	O	4N	V	5E	R	T	6E	R	■
■	O	■	L	■	H	■	P	■	R	■	■	L	■	■
7M	O	T	O	R	C	8O	N	T	R	O	L	L	E	9R
■	S	■	C	■	■	C	■	■	O	■	■	I	■	C
■	T	■	K	■	■	T	■	■	R	■	■	P	■	V
■	10C	C	D	I	M	A	G	E	S	E	N	S	O	R
■	O	■	R	■	■	V	■	■	I	■	■	E	■	■
11U	N	S	I	G	N	E	12D	■	G	■	■	■	■	■
■	V	■	V	■	■	■	13D	Y	N	A	M	O	■	■
14R	E	C	E	I	15V	E	R	■	A	■	■	■	16L	■
■	R	■	R	■	O	■	P	■	L	■	17R	F	I	D
■	T	■	■	■	Y	■	L	■	■	■	■	■	N	■
18N	E	W	S	■	A	■	19L	20E	A	K	A	G	E	■
■	R	■	■	■	G	■	■	V	■	■	■	■	A	■
■	■	21C	O	D	E	C	■	22M	I	R	R	O	R	S

Clues Across

1 What the American traveler, Ms. Ana Log, used to change her currency? **(4, 9)**
7 What Herbie and Taarzan may have used to be in command of the position, velocity, and torque of a mechanical drive **(5,10)**
10 The TC237B product from TI can capture a picture of Mr and Mrs Coulomb **(6, 8)**
11 The MSP430 microcontroller from TI comes with two built-in DACs - what kind of integer values do these DACs convert? **(8)**
13 This mechanical energy to electrical energy converter can charge your mobile if you crank it up? **(6)**
14 Where will you find the low noise amplifier, the RF front-end, the automatic gain control…? (TI makes chips for all of these!) **(8)**
17 With TI technology, you can flash your badge in the air to open doors **(4)**
18 What TI made in all four directions with the announcement of the Da Vinci technology **(4)**
19 Smart Reflect technology from TI arrests this to elongate battery life in mobile systems **(7)**
21 This twisted C source is an integral part of the software for MPEG and Audio compression/decompression **(5)**
22 How do they do this magic? The DLP girl and the elephant in the ad finally understood the secret - they do it with… **(7)**

Clues Down

1 I have heard of energy transformation, but this circuit changed the "secret of my energy" into a higher DC voltage! **(5,9)**
2 What the timing signal became, after passing the test from the Department of Motor Vehicles? **(5, 6)**
3 NBTI is a reliability degradation mechanism discovered first at TI. This cousin of NBTI is another bed of hot coals for analog designers! **(3)**
4 This BJT is used in the TI TV/VCR tuner IC **(3)**
5 What you might call the difference between where you want to be and where you are in a control system? **(5, 6)**
6 Using a TI calculator and a motion detector, you can plot the velocity versus position of a swinging pendulum (x,y). The equation

$$y = \pm b\sqrt{1-\frac{x^2}{a^2}}$$

will lead to a plot of this figure! **(7)**
8 What an analog designer may refer to doubling or halving the frequency as? **(6)**
9 When the tube radio became solid state and shrunk in size, they decided to call it by this short form? **(4)**
12 This circuit generates the 2X clock for the memory controller? **(3, 3)**
15 The TI calculator (TI-89) can take you on an expedition to the world of math! **(6)**
16 Related to the long line of Analog ICs made by TI? **(6)**
20 This module is for evaluation **(3)**

Feedback

Dear Ravi,

Thanks for mailing a copy of the January issue of VSI VISION.

Since last July, CMP introduced a 45 nm CMOS process, as well as a 65 nm SOI and a .12 µ SOI process.

Best regards,
Bernard Courtois

Dear Sir,

Thanks for sending a copy of VSI VISION Jan'08 Vol. 4 Issue 1.

Its really nice to see that there are some people in our country who are taking care of the research work being carried out in the field of VLSI in our country by publishing and promoting it in this reputed magazine.

Once again thanks and regards,

R.V. Kshirsagar

Dear Prof. Ravi Kumar

I would like to thank VSI for organizing an excellent workshop on Audio Codecs and Data Converters at Kolkata (June 16-18, 2008). I liked the rich technical content of the workshop. I strongly feel that VSI should continue to take an active role to promote VLSI education and research in India and we would request you to organize such events more regularly in coming days.

Ashis Kumar Mal
Asst Prof, NIT Durgapur

Hello Ravikumar

I enjoyed attending the Design Verification Methodologies (DVM) workshop this year, which was well organized with good response. Because of the structure of the workshop with focused attendees (~50), it provided an excellent forum for interactive sessions on the existing technologies and methodologies, and possible future directions in the critical and complex domain of Verification. The workshop had a good mix of participants from academia and industry, which included representatives from both the design companies and verification solution providers. Overall, a very successful workshop!

Gurudutt Bansal
Cadence Design Systems

Dear Ravi

Thanks for giving me an opportunity to be a speaker at DVM 2008. With ever growing complexity of analog designs, I feel that Innovative Methodologies for Analog Verification have not received as much attention as Digital Verification. This area needs some collective thrust from core semiconductor companies, EDA providers and academia in order to make a significant impact in terms of cycle time reduction, reducing risk of failures, etc.

Prabhat Agarwal
Sankalp Semiconductor

Dear Sir

Based on your message in the month of February through VDAT group, I submitted a paper entitled **"A 52.6mW 10-bit 100MS/s pipelined CMOS ADC"** for the **ASP Journal of Low Power Electronics (JOLPE)**, and it has been accepted for publication.

I thank you very much for your kindness in sending such valuable information to the VLSI related community.

Meganathan
Lecturer, MIT, Anna University, Chennai

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The initial submissions must be made in WORD or PDF format. Papers must adhere to the following guidelines:

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- Sections – 10 point Times-Roman font. Number the sections 1, 2, etc. Number the subsections 1.1, 2.2,1, etc.
- Figures and Tables - All drawings must be original. If the authors wish to reuse any drawings, charts, or tables, they must have prior permissions from the original authors. Figures and Tables must be numbered and must have captions.
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