eInfochips | The Solutions People

Effective PHY Verification of High Bandwidth Memory (HBM) Sub-system

Block & Full Chip Verification

50+ Bugs found in Preverified

Controllers and Memory Models

3+ Design Releases, On time

5+ End Customers Supported

Case Study

Executive Summary

Memory systems have improved a lot in the past few years owing to increasing data digitization and advancements in fabrication technology. High Bandwidth Memory (HBM) is an example of a new kind of memory chip designed to support low power consumption, ultra-wide communication lanes and the latest advances in stacked configurations. HBM's vertical stacking and fast information transfer rates can lead to some truly astounding performance rates across different, innovative form factors. It is ideally suited for high performance graphics and computing applications, high-end networking/communication devices and memory-hungry processors.

The eInfochips client, being an early adopter of HBM, wanted to introduce the technology to its newly launched storage solution, with in-built support for multiple memory controllers (full speed, half speed), HBM PHY and HBM DRAM. The client, however, was facing struggles in the verification of the HBM PHY layer due to the lack of an effective verification strategy and stringent delivery deadlines for multiple end customers. eInfochips introduced a verification strategy for the client to support the entire block and full-chip verification on HBM physical layer, meeting timelines while supporting 3 design releases and more than 5 end customers.

Client Profile

The client is a leading player in the analog and digital semiconductor market. Its fabless semiconductor applications serve multiple verticals including telecommunications, enterprise storage, wireless connectivity, broadband and more.

Business Challenge

For one of its enterprise storage solutions, the client wanted to introduce the latest designs in High Bandwidth Memory (HBM) technologies. However, effective verification remained a challenge as there were serious gaps in technical knowledge as well as timeline pressures due to the schedule committed to end customers. The support from third-party memory vendors was limited in scope.

Solution

The eInfochips team, owing to years of experience in the design of memory solutions, was able to quickly execute a verification strategy for complete block and chip-level verification on the HBM physical layer. The verification was executed in three phases to ensure timely delivery to end customers with following features and add-on modules:

- Block & full chip verification
- **Encrypted** third-party design and support for memory models of Samsung, Hynix and Cadence Systems
- Sensor integration for future functionalities
- 4 test benches developed
    - Block level test bench with third party memory controller
    - Replacing NWL Controller with DFI Driver test bench
    - Full-chip test bench with memory controller as design
- IEEE 1500 Testing for PHY & HBM Design
    - 100+ test cases for each test bench
    - System Verilog UVM 1.2 simulation
    - 10+ bugs found in preverified memory controller and memory models

Client Benefits

eInfochips was able to successfully plan and execute the verification strategy for the client with 3 design releases while supporting 5 different end customers.

"eInfochips' verification strategy helped us achieve on-time delivery of the product for our end customers."

About eInfochips

eInfochips is a global technology firm specializing in Product Engineering and Software R&D services. The company is recognized for technology leadership by Gartner, Frost & Sullivan, NASSCOM and Zinnov. eInfochips has contributed to 500+ products for top global companies, with more than 10 million deployments across the world.

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