eInfochips | The Solutions People

Improved ATPG Effectiveness through Intelligent Verification in ASIC

Targeted for Leading Automated Test Equipment (ATE) Client

40nm Pattern/Timing Generator Mixed ASIC

2.4 Gbps Max Throughput; 400 Mhz Operating frequency

2.2 GHz Data Bandwidth

Over 100 million gates in Digital Mode

Case Study

Executive Summary

The client is a global supplier of Automated Testing Equipment (ATE) for some of the world's most prestigious semiconductor companies. To meet its goal of developing faster, next-gen ATE instruments, it was working on a series of internal IPs, out of which a mixed signal ASIC chip with 40 nm pattern/timing generator and industry-wide high speed interfaces, emerged as a turnkey innovation. At once, time-to-market assumed key significance, and the client started looking for a partner to speedily ramp up its existing verification environment.

eInfochips enabled a highly configurable, scalable and intelligent verification environment in ASIC for the client, leading to enhanced verification coverage in a much shorter time. This also fulfilled Automatic Test Pattern Generation (ATPG) effectiveness criteria because thorough verification was achieved at block level (more than 20 internal blocks), cluster level, SoC-digital level, SoC-Chip level (Digital + Analog) and System Sim level. A critical architectural bug was found in the designs related to bandwidth verification.

Client Profile

With annual revenue in billion USD and 3500+ employees worldwide, the US-based client is a leading provider of Automated Testing Equipment (ATE) for the global semiconductor industry.

Business Challenge

For its next-generation ATE, the client developed an IP built on mixed signal ASIC with potential to be a game-changer. There was a need to shorten verification time as long as there was no compromise on schedule and ASIC features. This necessitated engaging with the right partner with strong expertise and having right skills. Also, it was expected that the solution would be reusable and sustainable in future ASIC work.

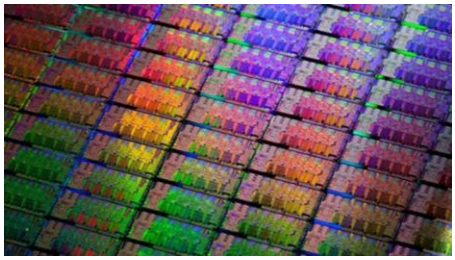
Solution

eInfochips created a highly reusable test bench fulfilling ATPG criteria which achieved thorough verification all the way from functional blocks to Silicon level. Key solution highlights included:

- Verification architecture development for block, cluster and chip level from scratch
- **Test bench** environment (SV/UVM)
- Digital Gate level verification
- UVC's interface creation for reusability
- Chip (digital + analog) level Gate verification
- 500 + (RTL + ref Model) bugs filed
- Found a critical architectural bug in the design of bandwidth verification
- Key voter for tape-out sign-off

Tools and Technologies

ATE, ASIC, SV/UVM, DDR4, PCIe (Gen.2), AXI Interconnect.



Client Benefits

Client completed the planned next-generation ASIC verification for ATE with the desired quality in the planned time. UVCs like AXI primary/replica were developed from scratch and customized with all customer requirements. And the client used them in existing and later ASIC projects as well.

"Intelligent Verification helped to Reduce time-to-market with critical architecture bug found + Reusability enabled for future ASIC roadmap."

About eInfochips

eInfochips is a global technology firm specializing in Product Engineering and Software R&D services. The company is recognized for technology leadership by Gartner, Frost & Sullivan, NASSCOM and Zinnov. eInfochips has contributed to 500+ products for top global companies, with more than 10 million deployments across the world.

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