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eInfochips Announces DDR2 SDRAM Verification IP and Reed Solomon Encoder Design IP

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eInfochips announced the availability of JEDEC (JESD79-2D) compliant DDR2 SDRAM (Double-Data-Rate-Two Synchronous Dynamic Random Access Memory) verification IP and European DVB, IEEE 802.16, IntelSat Earth Station (IESS), ETS 300 421 and ETS 300 429 standards compliant Reed Solomon encoder design IP.

eInfochips' DDR2 SDRAM verification IP (VIP) can be used to verify JEDEC standard (JESD79-2D) based DDR2 SDRAM memory model(s). The Reed Solomon design IP is designed for efficient implementation on FPGA and ASIC and can be used for communication systems like satellite communication, telecommunication, video and audio broadcast or data storage systems (ex: CD-ROM, Hard Disks etc.).

The DDR2 SDRAM verification IP supports normal mode command operations, multiple bank operations, data transfer with sequential/interleaved burst, extended mode registers, variable additive latency (0 Â 5 clocks), differential signaling for DQS (or LDQS and UDQS) and RDQS signals and auto configuration of timing parameters.

The command operations supported by DDR2 SDRAM VIP are truncated read/write, data masking, read/write with auto-precharge, posted column address strobe (CAS) read/write and seamless read/write command operations for bandwidth conservation. User configurable features of DDR2 SDRAM VIP are clock frequency model (400, 533, 667, 800), data port interface (x4, x8, x16), memory size (256 Mb, 512 Mb, 1 Gb, 2 Gb, 4 Gb), speed bins (3-3-3, 4-4-4, 5-5-5, 6-6-6).

The verification features available are functional coverage for coverage driven verification, protocol checks (assertions), active/passive VIP configuration operation and error injection mechanism.

Reed Solomon Design IP

The Reed Solomon Encoder (RS Encoder) accepts k blocks of symbols and generates n blocks of code words. n-k symbols are the parity. The number of errors that can be corrected for the parity generated by the RS encoder with defined n and k is given by t, where 2t = n - k. The core has been verified through extensive simulations, direct testing and code coverage measurements.

The RS Encoder accepts data serially and in bursts. It supports any primitive polynomial; user defined generated polynomial, shortened RS codes and has low latency output

The symbol width range of the core is 3-31 bits while the code symbol range is 4-231 symbols with parity up to 999 symbols. Its simple interface allows easy integration into larger systems.

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