

STORY

Published in **September / August 2008** issue of Chip Design Magazine

[DFM-DFY] Quantification-Based Verification Checks Embedded-Systems Video Quality

Video quality is crucial to any embedded video system. Using a comprehensive automated verification system is good insurance.

By Bhaskar Trivedi

Digital video consists of a sequence of images that are represented as two-dimensional arrays of pixels. Each pixel has associated luminosity and color information. There can be hundreds of thousands of pixels in a typical image. One second of digital video can contain up to 60 image frames. Thus, digital video comprises large amounts of information (see Table 1). Devices for video applications may contain an embedded system that performs video processing. Such video embedded systems perform capturing, storage, transmission, encoding, decoding, rendering, and other types of video processing in the analog or digital domain. When evaluating these systems, an automated video-quality verification system is highly desirable. One such verification system, for instance, operates on large data-sets, performs pixel-by-pixel verification, and takes into account a wide range of parameters that affect the video signal.

| Resolution (pixels) | Frame rate (frames/second) | Duration (minutes) | Uncompressed (RGB24) video size (GB) |
|---------------------|----------------------------|--------------------|--------------------------------------|
| 480p (720x480) | 60 | 5 | 17.38 (480x720x3x60x60x5) |
| 720p (1280x720) | 60 | 5 | 46.34 (720x1280x3x60x60x5) |
| 1080p (1920x1080) | 60 | 5 | 104.28 (1080x1920x3x60x60x5) |

Table 1: This table shows uncompressed video sizes

Among the examples of video embedded systems are the following: IP video cameras, surveillance systems, DVD players, video distribution systems, video gaming devices, digital televisions, video transcoders, digital cameras, digital camcorders, recognition systems, and video-based assembly-line inspection systems. Because video data is large, video embedded systems process a large amount of data. These systems also might have to perform complex mathematical operations on image frames. Hence, the systems typically contain a high-performance digital-signal-processor (DSP) core, which is capable of performing a large amount of parallel processing of data. It also can efficiently perform complex mathematical computations. Sometimes, a video embedded system also contains a video co-processor or processor core with specialized video-processing capabilities. These capabilities serve to increase the performance of the video embedded system.

During the manufacture of video embedded systems, they are tested and verified. In verification, the output video quality is often verified manually. The drawbacks of such manual verification include the following:

1. Visual/audio errors are easily missed with human play-out.
2. Subjectivity: different skill/level/experience/training
3. Consistency: It's impossible for a person to repeat exactly the same test day after day and week after week.
4. Simple errors: A human may not get constraints correct.
5. A person cannot look inside the file at the details (i.e., compression standard and bit rates of video, audio, and overall).

For some systems, partial quality verification is performed automatically with small data-sets. The drawback of such verification is incomplete and coarse verification. Manual verification is subjective. Thus, automatic objective verification is needed that is capable of operating on large data-sets.

The verification system used as an example in this article was developed for NetStreams, which is a leader in digital entertainment networks based on Internet-Protocol (IP) technology. NetStreams has a product line (video embedded systems) that delivers uncompressed content—including high-definition audio and video—to an unlimited number of rooms. That video system was verified by eInfochips.

To perform such verification, several challenges had to be overcome. Among the various video-processing components are video capture or playback, analog-to-digital or digital-to-analog conversion, format conversion, interlacing or de-interlacing, downsampling or upsampling, encoding or decoding, and packetization or de-packetization. Some of these components introduce losses including data and signal losses. Due to the characteristics of hardware components, signal levels can deviate from ideal or expected signal levels. Such problems pose major challenges in the realization of an automated video-quality verification system.

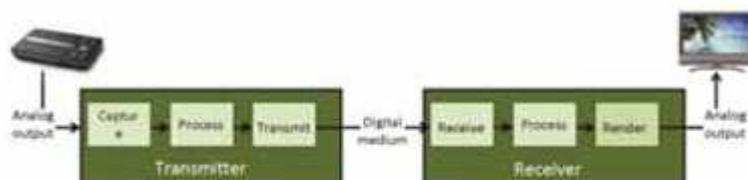


Figure 1: A block diagram of the video embedded system is shown here.

For video embedded systems, functional verification, data-integrity verification, and video-quality verification are of critical importance. The system used as an example here consists of a transmitter and receiver (see Figure 1). The transmitter captures video data from a video source like a DVD player. It then processes captured data and transmits video data over a digital packet network. The receiver receives transmitted video data, processes it, and renders video on a video-rendering device like a television.

During manufacture, each video embedded system undergoes an automatic manufacturing test to verify various on-board device functions. Yet this test doesn't verify whether the receiver renders correctly and the transmitter captures correctly. The automatic verification system that has been developed verifies both the video quality and data integrity of the display and capture path. As shown in Figure 1, the receiver generates analog output while the transmitter captures analog input. This way, the transmitter's analog input and the receiver's analog output can be verified—as long as the receiver's analog output is given as analog input to the transmitter. This setup is used in the automatic verification system (see Figure 2).

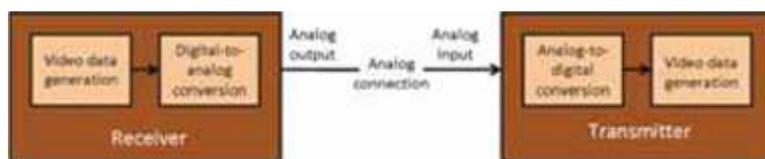


Figure 2: This block diagram details the automated video-quality verification system.

A bar-pattern video is used as sample video. The pixel values of the bar pattern are predefined. Sample video is generated in the receiver at 60 frames/s for progressive video and 30 frames/s for interlaced video. The generated sample video is given to the digital-to-analog converter for analog conversion. The analog video output is obtained at the receiver's output pins, which are connected to the transmitter's input pins by analog signal cables. In the transmitter, the analog signal is converted to digital video data by an analog-to-digital converter. The digital video data is analyzed with a verification algorithm. The automated analysis of video frames is done on a pixel-by-pixel basis. Various criteria have been defined for minimum acceptable video quality, such as maximum pixel-value deviation.

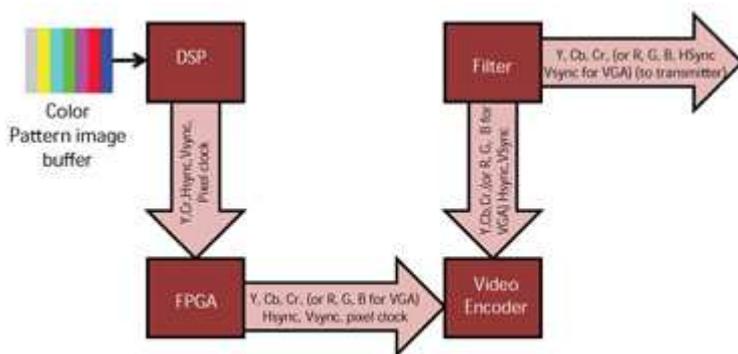


Figure 3: Here is an internal block diagram of the receiver.

An internal block diagram of the video embedded system’s receiver is shown in Figure 3. The DSP generates sample video from a bar-pattern image. The sample video—along with sync signals and a pixel clock—is given to the field-programmable gate array (FPGA). That FPGA performs any necessary format conversions and generates a video signal that’s suitable for the video encoder. It also gives the video signal to the video encoder. The video encoder, in turn, converts the digital video to analog video, which is given to the filter. The filter removes any undesirable frequencies from the video analog signal. The filtered-video analog signal is available at the receiver’s output pins.

The internal block diagram of the video embedded system’s transmitter is shown in Figure 4. The analog-video signal input is given to the video decoder. That decoder converts the analog video to digital video. It also gives the video data—along with sync signals and pixel clock—to the DSP. In addition, the video decoder gives H-sync and V-sync signals to the FPGA. For its part, the FPGA identifies the video resolution from H-sync and V-sync signals and gives the detected resolution to the DSP. The DSP performs verification of the video data that it receives.

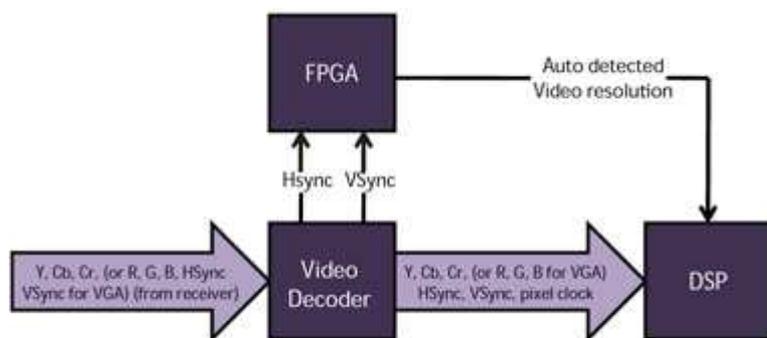


Figure 4: This internal block diagram depicts the transmitter.

For the verification of a large number of systems, “golden units” are made of the transmitter and receiver of the video embedded system. The golden unit is fine-tuned and adjusted to achieve nearly ideal results. The device to be verified is called the device under test (DUT). In the verification setup from the transmitter and receiver, one is a DUT while the other is a golden unit. Because the golden unit gives nearly ideal results, deviation in the DUT can be measured and verified.

Certain parameters of the video embedded system control image characteristics, such as brightness. They also control the analog output of the receiver. Due to incorrect settings of the parameters, a pixel’s value at the transmitter is much different from its value at the receiver. Similarly, the hardware-component characteristics of the video embedded system result in an analog video signal level that deviates from its ideal value. Hence, the parameters have to be adjusted so that a pixel’s value at the transmitter and the receiver only differ by a small amount.

Parameter settings that give desired results on one DUT don’t necessarily give desired results on another DUT. Thus, each DUT has certain optimal parameter settings that give desired results. In verification method 1, an optimal set of parameters is found for the DUT. The DUT is therefore configured with these parameters. verification is then performed on the DUT. A higher tolerance on

maximum pixel-value deviation (≤ 3 LSBs) is required for this verification method. The referenced graphs and measured pixel values (after parameter adjustments) are shown in Figure 5.

In the verification of the video embedded system, a reference image.

Graphs

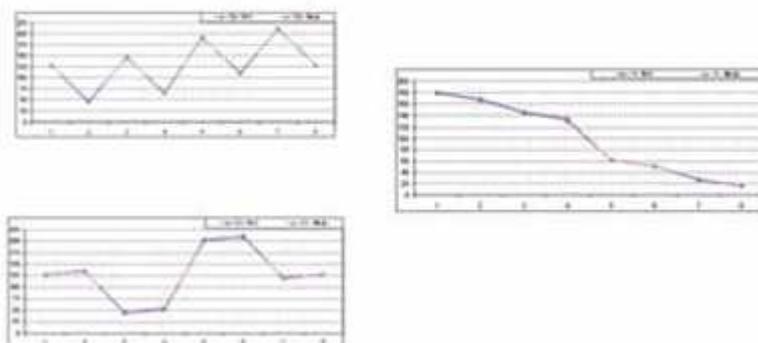


Figure 5: The reference and measured Y, Cb, and Cr values of a pixel for various colors ranging from 1 to 8 are shown after parameter adjustment.

is required at the transmitter. In verification method 2, the reference image is generated at the transmitter itself using a proprietary algorithm. This verification method is more or less immune to the parameter settings at both the transmitter and receiver. A lower tolerance of maximum pixel-value deviation (≤ 2 LSBs) is acceptable in this verification method. In addition, this method doesn't require parameter adjustments on each DUT. Some verification results for both verification methods 1 and 2 are shown in Table 2.

| Verification test | Maximum deviation in pixel value | Quality |
|---|----------------------------------|--------------|
| Before parameter adjustments | > 3 LSBs | Unacceptable |
| Verification method 1 (Parameter adjustment) | ≤ 3 LSBs | Acceptable |
| Verification method 2 (Verification on receiver only) | ≤ 2 LSBs | Acceptable |

Table 2: Here are the results of video-quality verification tests on a typical good unit.

In the verification of the video embedded system, analog signal cables are connected between the receiver and transmitter. The cables can introduce noise in the analog signal. Superior-quality cables add lesser noise. For quality verification, superior-quality cables are therefore used. Video resolutions of 480i, 480p, 720p, 1080i, and XGA are utilized in verification.

For systems involving lossy video compression—for which the video-quality degradation is hard to measure manually—the automated verification system can offer substantial advantages. It can run along with the unit testing of the device. As a result, separate video-quality verification isn't required after functional verification.

The automated verification system can be extended in the following ways:

1. Analog signal levels deviate from ideal values. Automatic feedback and correction can be implemented inside a chip to correct such deviation.
2. A quality-verification algorithm can be embedded inside a chip.
3. Parameters have to be adjusted to correct the deviation in pixel values. Automatic parameter adjustment can be implemented inside a chip.
4. Instructions for quality verification can be included in a chip's instruction set.
5. A pattern-bar image is used for verification. Other images can be used as well.
6. An automatic parameter adjustment can be implemented in the verification

- algorithm.
7. The verification algorithm can be optimized to reduce verification time and/or increase the frame rate of video analysis.
 8. Support for more video resolutions can be added.
 9. The verification algorithm provides pass or fail status in device test. The algorithm can be designed to give quantifiable information about video quality.
 10. Special quality-verification systems can be designed for video-compression-based systems, which take into account compression-related losses.
 11. A quality-verification algorithm can be ported to other embedded systems.

Video quality is of paramount importance in any video embedded system. Clearly, having a comprehensive automated verification system promises better quality. thankfully, much work has been done in this arena and automated verification systems have been successfully developed.

Special thanks to Rushabh Soni and Nirav Shah for their contributions.

References: 1. Jack, Keith, "Video Demystified - A Handbook for the Digital Engineer, Third Edition", LLH Technology Publishing.



Bhaskar Trivedi is a coach/program manager in the embedded division of eInfochips Ltd. (www.einfochips.com). He has more than 24 years of experience in the electronics and IT industry. Trivedi has held various roles in the areas of technology consulting, marketing and marketing support, customer-relationship management, project management, and support.