FOCUSREPORT

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Latest Challenges & Trends in Chip Verification

The sophistication of verification tools and techniques has increased with design complexity.

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There was a time when test issues were easily left as an afterthought to design. But increasing complexity in the design and manufacturability of both chips and embedded devices has brought testing issues to the forefront of the development process. Most designers in the EDA and semiconductor world automatically substitute the word "verification" for testing. But what activities are included in verification?

Logical and functional flaws continue to be the leading cause of costly design respins, notes Tom Fitzpatrick, Verification Technologist, Mentor Design Verification & Test Division (www.mentor.com). They suggest that a successful verification methodology encompasses testbench automation, assertion-based verification, coverage-driven verification, and transaction-level modeling. Critical applications include simulation, formal checkers, emulation and functional prototypes, and the ability to integrate these technologies into a comprehensive verification environment.

The increasing size and complexity of chips are driving verification engineers to adopt highly sophisticated approaches, observes Tom Anderson, Director of Technical Marketing for Synopsys. He explains that three techniques are dominating these approaches: assertions, stimulus generation, and code coverage. Assertions increase visibility into the design and accelerate bug finding. Constrained-random stimulus generation largely replaces hand-written tests while reducing the time for verification closure. Coverage-driven verification uses code and functional and assertion coverage metrics to assess progress and determine what to do next. When they're combined, Anderson says that these three methods help verification teams find more bugs more quickly.

According to the design professionals at eInfochips Inc., the widespread use of assertions for verification is becoming mainstream. System-Verilog-based verification will pick up fast, as it has Hardware Verification Language (HVL) features and assertions built into the language. System Verilog users can employ functional abstraction, coverage, and automation through randomization and reuse techniques. The language is gaining ground as a high-quality language for architecture exploration, verification, and transaction-layer modeling.

One strong trend that has emerged in choosing silicon architectures is an increase in verification and test-friendly techniques, observes Synplicity. At 90 nm, there are many risk and cost factors that require moving to new forms of verification. Examples include power-grid verification, design for yield, and design for manufacturability. But this fundamental skill set needed to handle these newer verification approaches is not readily available. As a result, Synplicity is seeing a strong uptake of 0.13-um, 0.11-um and 90-nm structured/platform ASICs as well as high-end FPGAs as an alternative to cell-based ASIC.

At both the chip and board level, more and more designs are incorporating multi-processing devices. Examples include today's single-chip multiple processors and the combination of FPGA and DSP devices. Successfully architecting these complex designs means stimulating the interaction of all of these differing components. This is best done at a high level before hardware-software implementations have been decided. Ken Karnofsky, Director of Marketing for DSP and Communications at The Mathworks, notes that model-based approaches save time and reduce risks. They use the verification and validation of the system model to find and fix any errors prior to the implementation level.

Testing chips like FPGAs can easily lead to verification issues at the board level--especially as embedded multi-processor architectures grow in popularity. For example, high-end smartphones already contain many microprocessors (MPUs) and DSPs to provide advanced 3G, Wi-Fi, and GPS functionality. These heterogeneous architectures make it more difficult to debug the hardware as well as the embedded

software, notes Filip Thoen, CTO of Virtio. One solution is to create virtual prototypes that allow greater flexibility for simulation.

Another area of verification concern is semiconductor intellectual property (IP). More and more libraries are beginning to fail at smaller process geometries. The effects of nanometer designs often resemble current-related problems because they are transient in nature, explain the experts at Nascentric Inc. Addressing these analog-like problems requires high-capacity, fast simulators that will make SPICE-accurate, transistor-level, full-chip simulation of the IP.

Verification and even the repair of IP has become a key driver in many recent innovations. Virage Logic, for example, recently introduced a Self-Test and Repair (STAR) Memory System. This system enables on-chip self-test and even repair at 130 nm and below. The capability to repair IP leads to reduced test costs, improved yield, and shorter time-to-volume.

Imported IP has placed additional strains on chip designers and tests. One way to verify imported IP is to move to new technologies that help identify bugs faster. These approaches also help to ensure the quality of blocks before system-level simulation, observes Craig Cochran, VP of Marketing for Jasper Design Automation. New assertion languages, such as PSL and SVA, are enabling designers and verification engineers to turn to formal verification to exhaustively prove the correctness of their assertions. They can identify bugs earlier and verify their designs more completely.