Embedded test tackles verification times

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Embedded chips and embedded systems need to be as defect-free as possible. This report addresses the testing criteria for embedded systems as well as system-on-chip (SoC) devices.

Verification consumes 70 percent of the resources in a typical chip design cycle. The ASIC design flow requires verification at each level of abstraction, from architecture to silicon prototype.

The challenge for engineers is to verify spec adherence for multiple abstractions. In its article below, eInfochips details how the hybrid verification model used in most verification processes can be enhanced to meet that challenge.

Carbon Design Systems Inc. argues that an SoC design isn't adequately tested until the system software is executed on the real hardware or on a cycle- and register-accurate model of the hardware.

The functionality of embedded systems is becoming increasingly sophisticated, and their real-time operation makes the debugging and verification of such systems extremely difficult to do in a reasonable time. LogicVision Inc. explains how a system verification team benefits when it designs test circuitry so that manufacturing test can be reused in a fully or partially configured system.

Online, Virage Logic Inc. shows how infrastructure intellectual property embedded in an IC can provide access to various IP for test/debug, analysis and yield improvement for volume manufacturing.

Full system simulation today can virtualize a system being tested along with the other systems with which it interacts. Virtutech Inc. believes that virtualization is beginning to create a sea change in the way that systems are tested and explains why in its contributed article.

A single stuck-at fault scheme is limiting. LSI Logic Corp. and Mentor Graphics Corp. in their co-authored article describe a multiple-detect scheme that caught an additional 70 defective units that had not been detected by the single-detect test on a 180-nanometer design.

Additional articles from EVE, Intel, Novas and Radisys address complementary testing issues online. Among these is the need for an emulation platform with a transaction-level interface that allows the design to be tested in the context of its real-world environment.