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Digital 'verification IP' is becoming more design-like

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San Mateo, Calif. — Once upon a time, digital verification meant test vectors and a good simulator. Everything else — understanding the operation of the design, intuiting the corner cases and finding a set of test vectors small enough to meet the schedule but large enough to find real problems — was up to the verification engineer's skill. It was occasionally pointed out, in quiet corners of the lunchroom, that technically, verification was harder than design, even though it had less status.

Then, as designs became larger and more functionally complex, human skill began to fall short. The test-vector set necessary to drive a system-on-chip to all of its valid states became enormous. It became nearly impossible to intuit the location of corner cases. In response, verification tools blossomed. New tools and whole new languages made it possible to do for verification what RTL had made possible for design — to generate test cases and checking routines from a high-level language. Formal tools made it possible — in some cases, and often after a great deal of manual munching — to formally prove assertions about specific blocks. But verification stayed hard.

But just as chip density eventually overwhelmed the productivity gains from synthesis, that same complexity is now overwhelming the gains from verification tools. And just as designers have turned to the shaky notion of reusable intellectual property (IP) to save them, the term "verification IP" is starting to float about.

"The key to ASIC verification today is IP leverage," said Tepan Joshi, vice president of marketing at design services firm eInfochips Inc. "But verification IP is today where design IP was a decade ago: It's hard to find, often unreliable and difficult to reuse without re-engineering."

ASIC verification at eInfochips is similar to that at a number of other design services organizations and large captive design shops. Its foundation is a collection of signal generators and checkers that connect to the design under test and to a supervisory program to automatically exercise not just the interfaces, but also the internal states of the design. But to gain sufficient productivity to make verification tractable, the methodology seeks opportunities to generalize a generator or checker, making it bulletproof, configurable and reusable.

An obvious opportunity for reuse comes in standard interfaces. A PCI bus, an SPI-4 interface or a DDR DRAM port all offer ideal chances to create reusable transaction generators and checkers, just as they are opportunities for reusable design IP to implement the interfaces themselves.

But just as making a block of PCI controller IP reusable takes a good deal of additional work, making the testbench for the interface takes just as much work.

One of the first lessons of verification IP design for reuse, said Niraj Patel, director of ASIC

engineering at eInfochips, is modularity. And again, the reasons are similar to those that make design IP modular. "In some cases, customers will use a standard block, like a PCI interface," Patel said. "But they will leave out the pieces they don't need. You need the verification IP to be modular as well, so that you can both disable the portions of the verification IP that won't be used, and set filters to look for states that shouldn't occur." Just as many of today's reusable virtual components are configurable by directing the synthesis tool to include or remove modules, the verification methodology must allow configuration of reusable verification IP.