**K2L SCHEMATICS**

**MAJOR REVISION HISTORY:**

<table>
<thead>
<tr>
<th>PCB REV.</th>
<th>SCH. REV.</th>
<th>DESCRIPTION</th>
<th>DATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>1.0</td>
<td>Pre-Proto Build</td>
<td>24-Dec-2013</td>
</tr>
<tr>
<td>2.0</td>
<td>2.06</td>
<td>Proto Build</td>
<td>02-Sep-2014</td>
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</table>

**I2C ADDRESS TABLE:**

<table>
<thead>
<tr>
<th>REF DES</th>
<th>DESCRIPTION</th>
<th>7 BIT ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPROM1</td>
<td>IC EEPROM 1MBIT 1MHZ 8SO</td>
<td>0x50</td>
</tr>
<tr>
<td>U40</td>
<td>IC SPD EEPROM 2KBIT 400KHZ 8TSSOP</td>
<td>0x53</td>
</tr>
</tbody>
</table>

**PCB MECHANICAL DETAILS:**

1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. PCB MATERIAL: TBD
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

**NOTES, UNLESS OTHERWISE SPECIFIED:**

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.
### POWER CONSUMPTION

**Approximate Power Consumption for TI_EVM - Lanam**

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Quantity Per Board</th>
<th>Current Consumed by corresponding device on power supply (mA)</th>
<th>Total Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.75</td>
<td>0.85</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Analog</td>
<td>USB</td>
</tr>
<tr>
<td>Marconis Connector</td>
<td>2 nos of Marconis EVM</td>
<td>2</td>
<td>760</td>
<td>810</td>
</tr>
<tr>
<td>Lanam (K2L) Port</td>
<td>TMS320C6713 DSP with ARM Core</td>
<td>1</td>
<td>1080</td>
<td></td>
</tr>
<tr>
<td>MT41K256M416HA125.E</td>
<td>C- CDRX 6GB (25MB/10)</td>
<td>5</td>
<td>1080</td>
<td></td>
</tr>
<tr>
<td>LM2940T3</td>
<td>Voltage regulator</td>
<td>1</td>
<td>136</td>
<td></td>
</tr>
<tr>
<td>B3E1512</td>
<td>Digital I/O phy</td>
<td>2</td>
<td>428</td>
<td></td>
</tr>
<tr>
<td>MT29F16G164DCECA</td>
<td>64MB Flash</td>
<td>1</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>ND2Q2BA1E1FSH4P</td>
<td>SPI NOR</td>
<td>1</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>LCB</td>
<td>USB display</td>
<td>1</td>
<td>136</td>
<td></td>
</tr>
<tr>
<td>CDMC269</td>
<td>Reference Clock generator</td>
<td>1</td>
<td>636</td>
<td></td>
</tr>
<tr>
<td>MCP25151T-E/S</td>
<td>IC IO Expander SPI BUS 2800</td>
<td>5</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>J23260</td>
<td>UART from EVM to DSP board</td>
<td>1</td>
<td>136</td>
<td></td>
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<tr>
<td>TDA1504A55</td>
<td>GMS Receiver</td>
<td>1</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>CP2165</td>
<td>IC USB to DUAL UART</td>
<td>1</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>KCS54040-4C/4G/901C</td>
<td>IC UART 1 J11 FPGA</td>
<td>1</td>
<td>90</td>
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<tr>
<td>TC993G</td>
<td>GMS Receiver</td>
<td>1</td>
<td>275</td>
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<tr>
<td>USB3.0 connector</td>
<td>USB 3.0</td>
<td>1</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>DSI00575050444/00PB</td>
<td>JESD and PCIe switch</td>
<td>4</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>FAN</td>
<td></td>
<td>1</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>UC53601</td>
<td></td>
<td>1</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Others</td>
<td></td>
<td>300</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Total Current on individual power supply (mA)</td>
<td></td>
<td>1000</td>
<td>760</td>
</tr>
<tr>
<td></td>
<td>6.5% margin added over design (mA)</td>
<td></td>
<td>1065</td>
<td>745.5</td>
</tr>
</tbody>
</table>

**Power Consumption in (mW):**

- **Total Current:** 85.199 mW
- **Total Current @ 12V:** 1.986 mW
- **Total Current @ 25V:** 1.986 mW
- **Total Current @ 3.3V:** 3195.68 mW
- **Total Current @ 3.3V:** 5512.07 mW

**Note:**
1. Above power consumption considers major block of design and provides indicative figure only.
2. Power rail assignment to different regulator is tentative based on power consumption, this can be changed based on sequence requirement.
3. Total power consumption is system is higher than ARC power(800mW), we assume that marconis EVM will be connected only when board is running on external power supply.
TABLE FOR SERDES CONNECTIONS

<table>
<thead>
<tr>
<th>Lamarr Ballname</th>
<th>Lamarr Ballname</th>
<th>Lamarr SOC Net name to switch</th>
<th>Switch Inputs</th>
<th>Switch Outputs</th>
<th>FMC1 Name</th>
<th>FMC1 Pin</th>
<th>FMC2 Name</th>
<th>FMC2 Pin</th>
<th>Marconi Name</th>
<th>AMC Name</th>
<th>AMC Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSISC2_0_RXN0</td>
<td>Diff In</td>
<td>A19</td>
<td>Shm1_RXN0</td>
<td>Shm1_RXP1</td>
<td>JESD0_RXN_FMC1</td>
<td>C7</td>
<td>TXN_S1</td>
<td>AIF0_RXN_AMC</td>
<td>141</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSISC2_0_RXP1</td>
<td>Diff In</td>
<td>A18</td>
<td>Shm1_RXP1</td>
<td>Shm1_RXN0</td>
<td>JESD0_RXP_FMC1</td>
<td>C6</td>
<td>TKP_S1</td>
<td>AIF0_RXP_AMC</td>
<td>142</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSISC2_0_RXM0</td>
<td>Diff In</td>
<td>A20</td>
<td>Shm1_RXM0</td>
<td>Shm1_RXM1</td>
<td>JESD0_RXM_FMC1</td>
<td>A2</td>
<td>TXN_S2</td>
<td>AIF1_RXM_AMC</td>
<td>147</td>
<td></td>
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</tr>
<tr>
<td>CSISC2_0_RXM1</td>
<td>Diff In</td>
<td>A19</td>
<td>Shm1_RXM1</td>
<td>Shm1_RXM0</td>
<td>JESD1_RXM_FMC1</td>
<td>A2</td>
<td>TKP_S2</td>
<td>AIF2_RXM_AMC</td>
<td>148</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSISC2_0_TXN0</td>
<td>Diff Out</td>
<td>A17</td>
<td>Shm2_TXN0</td>
<td>Shm2_TXP1</td>
<td>JESD0_TXN_FMC1</td>
<td>C3</td>
<td>RXN_S1</td>
<td>AIF0_TXN_AMC</td>
<td>144</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSISC2_0_TXP0</td>
<td>Diff Out</td>
<td>A18</td>
<td>Shm2_TXP0</td>
<td>Shm2_TXN1</td>
<td>JESD0_TXP_FMC1</td>
<td>C2</td>
<td>RXP_S1</td>
<td>AIF0_TXP_AMC</td>
<td>145</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSISC2_0_TXM0</td>
<td>Diff Out</td>
<td>A19</td>
<td>Shm2_TXM0</td>
<td>Shm2_TXM1</td>
<td>JESD1_TXM_FMC1</td>
<td>A27</td>
<td>RXM_S2</td>
<td>AIF1_TXM_AMC</td>
<td>150</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSISC2_0_TXM1</td>
<td>Diff Out</td>
<td>A18</td>
<td>Shm2_TXM1</td>
<td>Shm2_TXM0</td>
<td>JESD1_TXM_FMC1</td>
<td>A26</td>
<td>RXP_S2</td>
<td>AIF1_TXP_AMC</td>
<td>151</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: Place the capacitors close to VDD pins of the IC.

Note: Output is fully compatible with AC coupled CML inputs. FMC/AMC end should support CML input.
Note: Place the capacitors close to VDD pins of the IC.

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### TABLE FOR SERDES CONNECTIONS

<table>
<thead>
<tr>
<th>Lamarr Ballname</th>
<th>Lamarr Ball</th>
<th>Lamarr SOC Net name to switch</th>
<th>Sw/SOC</th>
<th>Switch Inputs</th>
<th>Switch Outputs</th>
<th>FMC1 Name</th>
<th>FMC1 Name</th>
<th>FMC2 Name</th>
<th>Marconi Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>JESD2_RXP_SOC</td>
<td>A116</td>
<td>JESD2_RXP_SOC</td>
<td>Sw Out</td>
<td>3323_RXP_SOC</td>
<td>3323_RXP_SOC</td>
<td>A3</td>
<td>A3</td>
<td>A3</td>
<td>TXP_S3</td>
</tr>
<tr>
<td>JESD2_RXP_SOC</td>
<td>A115</td>
<td>JESD2_RXP_SOC</td>
<td>Sw Out</td>
<td>3323_RXP_SOC</td>
<td>3323_RXP_SOC</td>
<td>A6</td>
<td>A6</td>
<td>A6</td>
<td>TXP_S3</td>
</tr>
<tr>
<td>JESD2_RXP_SOC</td>
<td>A117</td>
<td>JESD2_RXP_SOC</td>
<td>Sw Out</td>
<td>3323_RXP_SOC</td>
<td>3323_RXP_SOC</td>
<td>A11</td>
<td>A11</td>
<td>A11</td>
<td>TXN_S4</td>
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<tr>
<td>JESD2_RXP_SOC</td>
<td>A116</td>
<td>JESD2_RXP_SOC</td>
<td>Sw Out</td>
<td>3323_RXP_SOC</td>
<td>3323_RXP_SOC</td>
<td>A10</td>
<td>A10</td>
<td>A10</td>
<td>TXP_S4</td>
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<tr>
<td>JESD2_TXN_SOC</td>
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<td>JESD2_TXN_SOC</td>
<td>Sw In</td>
<td>3323_TXN_SOC</td>
<td>3323_TXN_SOC</td>
<td>A22</td>
<td>A22</td>
<td>A22</td>
<td>BTN_S3</td>
</tr>
<tr>
<td>JESD2_TXN_SOC</td>
<td>A115</td>
<td>JESD2_TXN_SOC</td>
<td>Sw In</td>
<td>3323_TXN_SOC</td>
<td>3323_TXN_SOC</td>
<td>A22</td>
<td>A22</td>
<td>A22</td>
<td>BTN_S3</td>
</tr>
<tr>
<td>JESD2_TXN_SOC</td>
<td>A115</td>
<td>JESD2_TXN_SOC</td>
<td>Sw In</td>
<td>3323_TXN_SOC</td>
<td>3323_TXN_SOC</td>
<td>A31</td>
<td>A31</td>
<td>A31</td>
<td>BTN_S4</td>
</tr>
<tr>
<td>JESD3_TXP_SOC</td>
<td>A116</td>
<td>JESD3_TXP_SOC</td>
<td>Sw In</td>
<td>3323_TXP_SOC</td>
<td>3323_TXP_SOC</td>
<td>A20</td>
<td>A20</td>
<td>A20</td>
<td>RXP_S4</td>
</tr>
</tbody>
</table>
SGMII/PCIe Serdes switch

Note: Place the capacitors close to VDD pins of the IC.

Note: Output is fully compatible with AC coupled CML inputs. FMC / AMC end should support CML input.

TABLE FOR SERDES CONNECTIONS

<table>
<thead>
<tr>
<th>Project</th>
<th>K2L EVM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Title</td>
<td>SGMII/PCIe Serdes switch</td>
</tr>
<tr>
<td>Size</td>
<td>C</td>
</tr>
<tr>
<td>Document Number</td>
<td>16_00176_02</td>
</tr>
<tr>
<td>Rev</td>
<td>2.06</td>
</tr>
<tr>
<td>Date</td>
<td>Thursday, September 11, 2014</td>
</tr>
<tr>
<td>Sheet</td>
<td>14 of 47</td>
</tr>
</tbody>
</table>
VDD = 3.3V

VREF = VDD \times \left( \frac{R2}{R1+R2} \right)

D = 3.3V \times \left( \frac{1K}{5.6K+1K} \right) = 3.3V \times \left( \frac{1K}{6.6K} \right)

Note: Differential signals Routing

10MHz clock input circuit added for positive clamp
Place these resistors at the end of the trace.
* DDR3 pin M7 is used for A15 as per JEDC standard

* Data bits can be swapped within the byte lane to ease routing.

* Address/Command/Control/Clock routing must be FLY-BY in byte order 0, 1, 2, 3 ECC, 4, 5, 6, 7.

* DDR3 pin M7 is used for A15 as per JEDC standard

* DDR3 pin M7 is used for A15 as per JEDC standard

* DDR3 pin M7 is used for A15 as per JEDC standard

* DDR3 pin M7 is used for A15 as per JEDC standard
K2L GND AND POWER

These caps are added for provision only. Values can be changed based on PI analysis result.

0201
Place near to SOC pins

0402

These caps are added to support per pin decap. Based on PI analysis result, it will be changed (# of capacitors, values, etc).

0402

Newly added decaps for PI (12nos added)
K2L USB3, TPS USB 5v isolation, USB Type A connector, magnetics, filter, SOC UART 1.8/3.3v, USB to dual UART

K2L USB3

TPS USB 5v isolation

SOC UART 1.8/3.3v

USB to dual UART

Project: K2L EVM

Designed for TI by eInfochips

K2L USB3, TPS USB 5v isolation, USB Type A connector, magnetics, filter, SOC UART 1.8/3.3v, USB to dual UART

Note: For USB Power Isolation
USIM, SOC UART 1.8v switching, 1.8v/3.3v GPIO INT, SOC UART, GPS

SOC UART 1.8v switching

Note: GPIO8
0, SOC_UART0_Rxd -> UART1_Rxd
1, GPS_UART0_Rxd -> UART1_Rxd

Note: GPIO11
0, SOC_UART1_Rxd -> EXP_UARTTX0
1, SOC_UART1_Rxd -> GPS_UARTTX0

SPI level shift 3.3V ↔ 1.8V

FOR ANTENNA CIRCUIT
Expansion Connector, I2C SOC to Expander 1.8v/3.3vAux

Expansion Connector

I2C SOC to Expander 1.8v/3.3vAux

Expansion Connector, I2C SOC to Expander 1.8v/3.3vAux

Note: Timer Pins showing which pins go to Timer Inputs on the SOC, since all 4 signals here are labeled as outputs

Designed for TI by eInfochips
Note: VCCMON group and EMIF group are different as per IO sheet 0.7

Note: NAND FLASH Device size is 2GB.
EMIF Addr/Cntl Buffer, Ext EMIF_OE, EMIF Data Transceiver
BMC Processor (LM3S2D93), switches, DIPsw, UART Rx Mux, LEDs

Project: K2L EVM
Title: Designed for TI by eInfochips

Size: C
Document Number: 16_00176_02
Rev: 2.06
Date: Thursday, September 11, 2014
Sheet: 29 of 47
LCD, LCD Power, BMC USB for UART, 4pin UART for BMC, BMC JTAG, BMC to PMBus isolator, PCIe clock

**LCD Power**

```
V_O = 1.24*(1+R1/R2)+0.15uA*R1
V_O = 1.24 (1+10k/6.98k)+0.15u*10k
```

**MCU UART**

**USB to BMC UART**

**MCU JTAG**

**PCle CLOCK MUX**

**Project**

K2L EVM

**Designed for TI by eInfochips**

**Date**

Thursday, September 11, 2014

**Sheet**

30 of 47
Ethernet PHY, Magnetics for 2 channel/ Tx/Rx, MDC/MDIO for AMC, K2L SGMII/ PCIe

88E1514

K2L SGMII/ PCIe

MDC/MDIO for AMC

<table>
<thead>
<tr>
<th>Pin</th>
<th>CONFIG</th>
<th>CONFIG PLL</th>
<th>Value Assignment</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>soc_int0=3.3V</td>
<td>VCC</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>PHY0/4/8/12</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>PHY0/4/8/12</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>soc_int0=3.3V</td>
<td>VCC</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>PHY0/4/8/12</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>PHY0/4/8/12</td>
<td></td>
</tr>
</tbody>
</table>

Designed for TI by eInfochips
CDCM62008 Clk1, 122.88/19.2, Power Filter for Clock, VCTXCO, SPI 1.8/3.3v for 1588 DAC, VRef, 1588DAC

Serial Interface Mode or Pin Mode Selection

<table>
<thead>
<tr>
<th>MCU_S_MODE[1:0]</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>SPI MODE (Default)</td>
</tr>
<tr>
<td>01</td>
<td>I2C MODE</td>
</tr>
<tr>
<td>10</td>
<td>PIN MODE (NO SERIAL PROGRAMMING)</td>
</tr>
<tr>
<td>11</td>
<td>RESERVED</td>
</tr>
</tbody>
</table>

[Note] layout would place B440 and C334 close to U47.
STATUS outputs the PLL_LOCK signal
STATUS1 the LOSS OF REFERENCE.

[Note] layout would place R757 and C327 close to U43.

Serial Interface Mode or Pin Mode Selection

<table>
<thead>
<tr>
<th>MCU_SI_MODE(1:0)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>SPI MODE (Default)</td>
</tr>
<tr>
<td>01</td>
<td>1C MODE</td>
</tr>
<tr>
<td>10</td>
<td>PIN MODE (NO SERIAL PROGRAMMING)</td>
</tr>
<tr>
<td>11</td>
<td>RESERVED</td>
</tr>
</tbody>
</table>
XDS200 / AM1802, flash, USB connector for Emulator
XDS200 / AM1802, boot mode, reset, XDS200 power
12v input (fused), 12v to 3p3v MP, K2L VID, 1p8 to VPP1p8 switch, 3v3Aux to 3v3, FMC1 Power (fuse), FMC2 Power (fuse), fan connector

12V to VCC3V3_MP_ALT Generation

FMC1 POWER

Over Current Protection

TVS Voltage BreakDown = 13.3V

I(hold) = 1.5A
I(trip) = 3A
Trip Time= 8s

TVS

Voltage BreakDown = 13.3V

FMC2 POWER

Over Current Protection

TVS Voltage BreakDown = 13.3V

I(hold) = 1.5A
I(trip) = 3A
Trip Time= 8s

TVS

3V3_AUX to VDD33 Generation

VCC1V8 to VPP1V8

DC FAN Connector for SOC
Top Avatar, 12v to CVVD, 12v to 1.5v, 3.3v aux -> 1.2v, 3.3v aux -> 1.8v

12V to CVDD Generation

LAYOUT NOTE:
- Place R586 and R585 very close to the SoC CVDD power pins

PMBUS_DAT 32,44

R839 4.7K_5%
R541 0E
R17 0E
R529 0E

CVDD_EN 32,43

VCC12

LAYOUT NOTE:
- Make the CVDD and GND test points with big test pad for load test purpose.
- Place TP123 and TP124 near resistor group on top side

R586 10E_1%

VSSCMON 27

TPS544C25

CT3
C45
C430
C431

CT2

CT4

R39 1E_0.25W_5%_1206

12V to CVDD Generation

R8 2

R134

R111

182K_0.1W_1%_0402

LM10011_VID1S 32,42
LM10011_VID1C 32,42
LM10011_VID1B 42
LM10011_VID1A 42

MODE

EN

SET

DAP

LM10011SD/NOPB

R840

1.5V @ 4.5A

Vout=0.8 V*(R1/R2+1)
=48000x700^(-0.997)-2
=67.93 (k ohms)

Project
K2L EVM

Designed for TI by eInfochips

Title
Top Avatar, 12v to CVVD, 12v to 1.5v, 3.3v aux -> 1.2v, 3.3v aux -> 1.8v

Size C
Document Number
Rev 2.06

Date: Thursday, September 11, 2014
Sheet 43 of 47

12V to 1.5V Generation

1.5V @ 4.5A

Vout=0.8 V*(R1/R2+1)
=48000x700^(-0.997)-2
=67.93 (k ohms)

Reference Inductor 1.2uH

3.3V_AUX to 1.2V Generation

Vin = 10.8V to 13.2V

Rr=48000xVin(Vout)^(-0.997)-2
=48000x700^(-0.997)-2
=67.93 (k ohms)

(Volt(Vin)^-0.997)-2
=67.93 (k ohms)

(Over all tolerance is 5%, DC tolerance is 2.5%)
LM26430, 12v -> CVVD1, 1v8, v85, 5v

LM26430

LAYOUT NOTE: Follow Layout Instructions guide line

Title  Size  Project  Rev  Date:  Document Number of Sheet
Designed for TI by eInfochips

LM26430, 12v -> CVVD1, 1v8, v85, 5v

C

44 47 Thursday, September 11, 2014

K2L EVM

16_00176_02 2.06
K2L VDDALV, v85 filter, bypass caps, 12v -> 3.3vaux

VCC3V3_AUX

Assume 90% Po

\[ Io = \left( \frac{3.3V}{3.5A} \right) / 90\% / 12V = 1.1A \]

12V@1.1A

\[ R_{t} = 48000 \times Fsw(\text{kHz}) \times (0.997)^{-2} \]

\[ = \frac{48000 \times 840}{(0.997)^{-2}} \]

\[ = 56.2 \times 3 \text{ ohms} \]

(Vout = 0.8 V*(R1/R2+1)
\[ R_{t} = 48000 \times 840^{-0.997} - 2 \]

\[ \approx 56.2 \times 3 \text{ ohms} \]

(Over all tolerance is 5% , DC tolerance is 2.5%)

Reference Inductor = 3.3uH

Reference Capacitor = 100uF
# KEYSSTONE2 LAMARR EVM - REVISION HISTORY

<table>
<thead>
<tr>
<th>PCB. REV.</th>
<th>SCH. REV.</th>
<th>CHANGE DESCRIPTION</th>
<th>DATE</th>
<th>AUTHOR</th>
</tr>
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<tbody>
<tr>
<td>1.0</td>
<td>1.0</td>
<td>Release to Fabrication</td>
<td>24-DEC-2013</td>
<td>eInfochips</td>
</tr>
<tr>
<td>1.01</td>
<td>1.01</td>
<td>1. SDRAM circuitry added in XDS section</td>
<td>23-JAN-2014</td>
<td>eInfochips</td>
</tr>
<tr>
<td>1.02</td>
<td>1.02</td>
<td>1. Serdes switch settings changed to I2C mode from pin mode; [Pages - 12, 13, 14]</td>
<td>12-MAR-2014</td>
<td>eInfochips</td>
</tr>
<tr>
<td>1.03</td>
<td>1.03</td>
<td>1. Layout instruction is given for shorting AGND and PGND at a single point for Top Avatar section. [Page-43]</td>
<td>18-MAR-2014</td>
<td>eInfochips</td>
</tr>
<tr>
<td>2.0</td>
<td>2.01</td>
<td>1. 10MHz clock circuit for clamping input signal to +1V. [Page18]</td>
<td>1-MAY-2014</td>
<td>eInfochips</td>
</tr>
<tr>
<td>2.02</td>
<td>2.02</td>
<td>1. CN21(2-3) changed to CN6(2-3); CN8(2-3) changed to CN10(2-3); CN2(1-2) changed to CN11(1-2)</td>
<td>10-JUL-2014</td>
<td>eInfochips</td>
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<tr>
<td>2.03</td>
<td>2.03</td>
<td>DM21 to DM28 added</td>
<td>21-JUL-2014</td>
<td>eInfochips</td>
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<tr>
<td>2.04</td>
<td>2.04</td>
<td>CN9(1-2) is replaced with CN13(1-2); R417 made NU</td>
<td>4-AUG-2014</td>
<td>eInfochips</td>
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<tr>
<td>2.05</td>
<td>2.05</td>
<td>FXP103 power changed to Vbus mode from Self Power mode</td>
<td>18-AUG-2014</td>
<td>eInfochips</td>
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<tr>
<td>2.06</td>
<td>2.06</td>
<td>DDR3 SDRAM -ECC chip U31 made populated</td>
<td>2-SEP-2014</td>
<td>eInfochips</td>
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## Dummy Components

- Board Stud 3x12mm
- Board Screw 3x6mm
- Nylon Washer 3mm

## On Board Fiducials

- Board Stud 3x12mm
- Board Screw 3x6mm
- Nylon Washer 3mm

## Mounting Holes

- Board Stud 3x12mm
- Board Screw 3x6mm
- Nylon Washer 3mm

---

**Front panel and ESD Strip**

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Project: K2L EVM  
Title: KEYSSTONE2 LAMARR EVM  
Designed for TI by eInfochips  

**REV**ision HISTORY

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<thead>
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