

K2L SCHEMATICS

MAJOR REVISION HISTORY :

PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	1.0	Pre-Proto Build	24-Dec-2013
2.0	2.0	Proto Build	8-AUG-2014

I2C ADDRESS TABLE :

REF DES	DESCRIPTION	7 BIT ADDRESS
EEPROM1	IC EEPROM 1MBIT 1MHZ 8SO	0x50
U40	IC SPD EEPROM 2KBIT 400KHZ 8TSSOP	0x53

PCB MECHANICAL DETAILS :

1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. PCB MATERIAL: TBD
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.

PCB LAYER STACK-UP DETAILS :

LAYER STACK-UP

	----- PRIMARY SIDE, SILK SCREEN	
	PRIMARY SIDE, SOLDER MASK	- 2 MILS
	PRIMARY SIDE, LAYER 1	- 1.794 MILS
	DIELECTRIC	- 3.596 MILS
	GROUND LAYER, LAYER 2	- 1.26 MILS
	DIELECTRIC	- 4 MILS
	INNER LAYER, LAYER 3	- 1.26 MILS
	DIELECTRIC	- 5.014 MILS
	POWER LAYER, LAYER 4	- 1.26 MILS
	DIELECTRIC	- 5 MILS
	INNER LAYER, LAYER 5	- 1.26 MILS
	DIELECTRIC	- 3.814 MILS
	GROUND LAYER, LAYER 6	- 1.26 MILS
	DIELECTRIC	- 4 MILS
67.036 MILS +/-10%	GROUND LAYER, LAYER 7	- 1.26 MILS
	DIELECTRIC	- 3.814 MILS
	INNER LAYER, LAYER 8	- 1.26 MILS
	DIELECTRIC	- 5 MILS
	POWER LAYER, LAYER 9	- 1.26 MILS
	DIELECTRIC	- 5.014 MILS
	INNER LAYER, LAYER 10	- 1.26 MILS
	DIELECTRIC	- 4 MILS
	GROUND LAYER, LAYER 11	- 1.26 MILS
	DIELECTRIC	- 3.596 MILS
	SECONDARY SIDE, LAYER 12	- 1.794 MILS
	SECONDARY SIDE, SOLDER MASK	- 2 MILS
	----- SECONDARY SIDE, SILK SCREEN	

DISCLAIMER: THIS CIRCUIT DESIGN IS PROVIDED AS REFERENCE ONLY, WITHOUT WARRANTY EXPRESSED OR IMPLIED. THE USER IS ENCOURAGED TO PERFORM ALL DUE DILIGENCE WITH RESPECT TO DESIGN AND ANALYSIS. FOR COMMITTED PERFORMANCE AND FUNCTIONALITY OF THE DEVICE, PLEASE REFER TO THE DEVICE DATA MANUAL.

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Project K2L EVM		Designed for TI by einfochips	
Title COVER PAGE			
Size C	Document Number 16_00176_02		Rev 2.04
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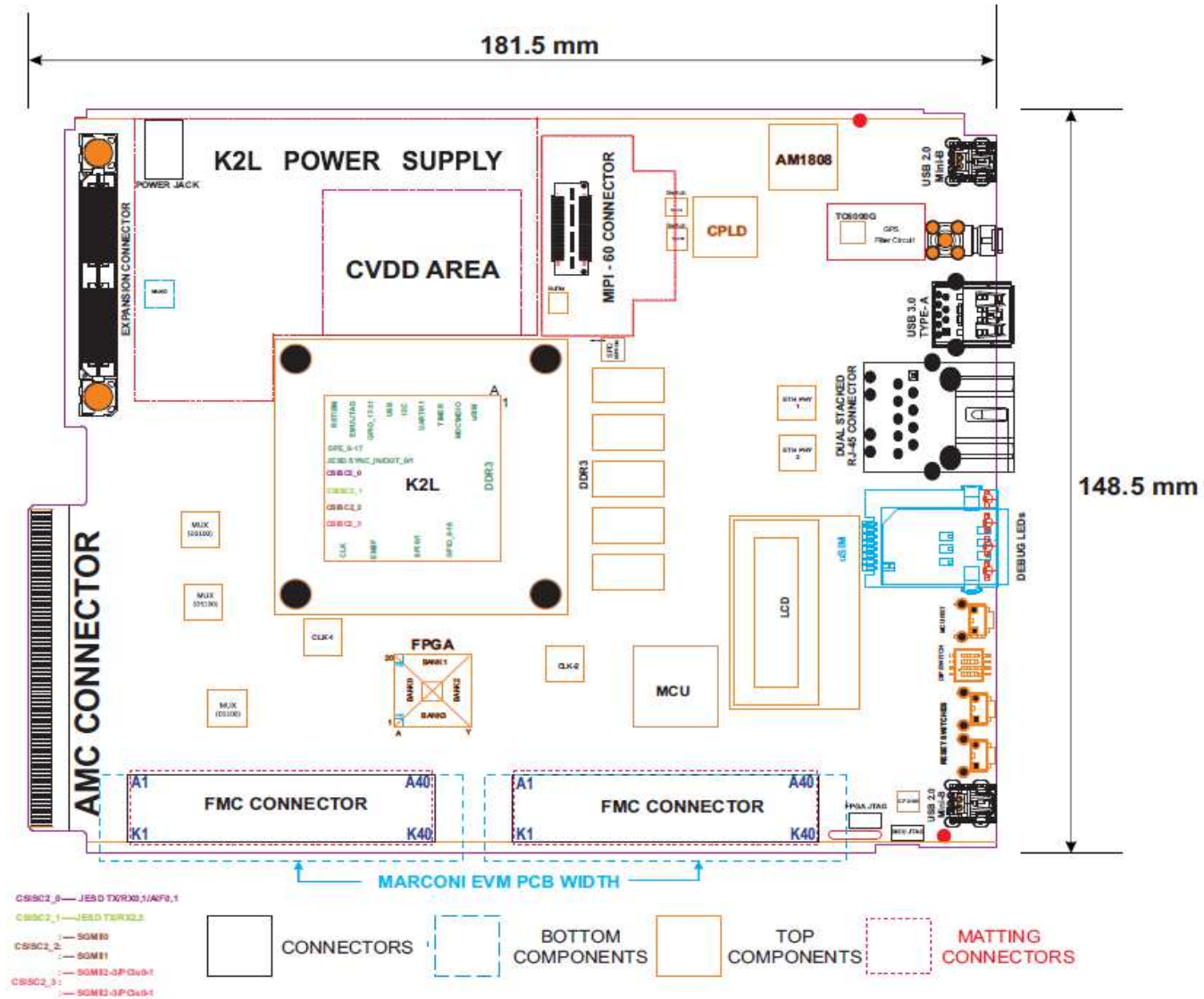
SCHEMATIC PAGE CONTENT

1	: COVER PAGE
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15	: FPGA, SYSREF Buffering, LEDs
16	: FPGA, FPGA 2pin conn, SPI Flash, LEDs
17	: FPGA, K2L SPI/TIM/UART, FPGA test conn
18	: K2L LVDS SigMux, Clock Mux, K2L Reset, K2L CML Serdes JESD/AIL,
19	: K2L DDR3
20	: DDR3(3)
21	: DDR3(2), 3.3vaux -> .75v DDR3 Vt, DDR3 SPD EEPROM
22	: K2L GND AND POWER
23	: K2L USB3, TPS USB 5v isolation, USB Type A connector, magnetics, filter, SOC UART 1.8/3.3v, USB to dual UART
24	: K2L EMU, K2L JTAG, EMU MIPI 60, EMU Detect, AMC/XDS200
25	: USIM, SOC UART 1.8v switching, 1.8v/3.3v GPIO INT, SOC UART, GPS
26	: Expansion Connector, I2C SOC to Expander 1.8v/3.3vAux
27	: K2L EMIF, VDD and VSSMON, EMIFWAIT1 bfr, NAND Flash, I2C EEPROM
28	: EMIF Addr/Cntl Buffer, Ext EMIF_OE, EMIF Data Transceiver
29	: BMC Processor (LM3S2D93), switches, DIPsw, UART Rx Mux, LEDs
30	: LCD, LCD Power, BMC USB for UART, 4pin UART for BMC, BMC
31	: AMC connector
32	: SOC Temp, UCD9090, PMBus Pgm conn, VID Isolator for PMBus
33	: Ethernet PHY, Magnetics for 2 channel/ Tx/Rx,
34	: Ethernet PHY, Magnetics for 2 channel/ Tx/Rx
35	: CDCM62008 Clk1, 122.88/19.2, Power Filter for Clock,
36	: CDCM62008 Clk2, 100 / 156.25, Power Filter for Clock
37	: XDS200 / AM1802, flash, USB connector for Emulator
38	: XDS200 / AM1802, boot mode, reset, XDS200 power
39	: XDS200 / debug hdr, oscillators
40	: XDS200 Power
41	: XDS200 Emulation CPLD
42	: 12v input (fused), 12v to 3p3v MP, K2L VID, 1p8 to VPP1p8 switch, 3v3Aux to 3v3, FMC1 Power (fuse),
43	: Top Avatar, 12v to CVVD , 12v to 1.5v, 3.3v aux -> 1.2v, 3.3v aux -> 1.8v
44	: LM26430, 12v -> CVVD1, 1v8, v85, 5v
45	: K2L CVVD, CVVD1, bypass caps, K2L 1v8, K2L 1v0 PLL, caps, filters
46	: K2L VDDALV, v85 filter, bypass caps, 12v -> 3.3vaux
47	: REVISION HISTORY

Project K2L EVM		Designed for TI by elnfochips	
Title TABLE OF CONTENTS		 TEXAS INSTRUMENTS  The Solutions People	
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Project K2L EVM		Designed for TI by einfochips	
Title BLOCK DIAGRAM		  The Solutions People	
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PLACEMENT



Project K2L EVM		Designed for TI by elfnochips	
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POWER CONSUMPTION

Approx Power Consumption for TI_EVM -Lamar

Components Part No.	Description	Quantity Per Board	Current Consumed by corresponding device on power supply (mA)													Total Power (mW)
			0.75	0.85	0.85	0.95	1	1.2	1.5	1.8	1.8	3	3.3	5	12	
				Analog	USB	Fixed DSP+ARM	AVS(DSP+ARM)			Digital	Analog					
Marconi Connector	2 Nos of Marconi EVM	2													1500	18000
Lamar (K2L) Part	TI- Multicore DSP with ARM Core	1		700	800	2900	18800		800	400	600		25			25912.5
MT41K256M16HA125-E	IC, DDR3, 4Gb (256Mx16)	5	1000						3000							5250
LM3S2093	Microcontroller	1											135			445.5
88E1512	Gigabit ethernet phy	2											426			1405.8
MT29F16G16ADBCA	Nand Flash	1								40						72
N25Q128A11ESF40F	SPI NOR	1								20						36
LCD	LCD display	1										45				135
CDCM6208	Reference Clock generator	2											636			2098.8
MCP23S17T-E/SS	IC I/O EXPANDER SPI 16B 28SSOP	5								16			4			42
XDS200 circuitry (referred from K@E)	XDS200 circuitry	1												136		680
TXS4555RGTR	SIM translaor	1								5			50			174
CP2105	IC USB to DUAL UART	1											45			148.5
XC3S400AN-4FGG400C	IC SPARTAN 3AN FGG400 FPGA	1						90		275			409			1952.7
TC6000G	GPS Receiver	1								83						149.4
USB3.0 connector	USB 3.0	1												900		4500
DS100MB203SQE/NOPB	JESD and PCIe switch	4											828			2732.4
FAN		1													100	1200
UCD9090		1											60			198
Others	Other Ics	1								600			300			2070
Total Current on individual power supply (mA)			1000	700	800	2900	18800	90	3800	1439	600	45	2918	1036	1600	
6.5% margin added over design (mA)			1065	745.5	852	3088.5	20022	95.85	4047	1532.535	639	47.925	3107.67	1103.34	1704	
Power Consumption in (mW)			798.75	633.675	724.2	2934.075	20022	115.02	6070.5	2758.563	1150.2	143.775	10255.311	5516.7	20448	

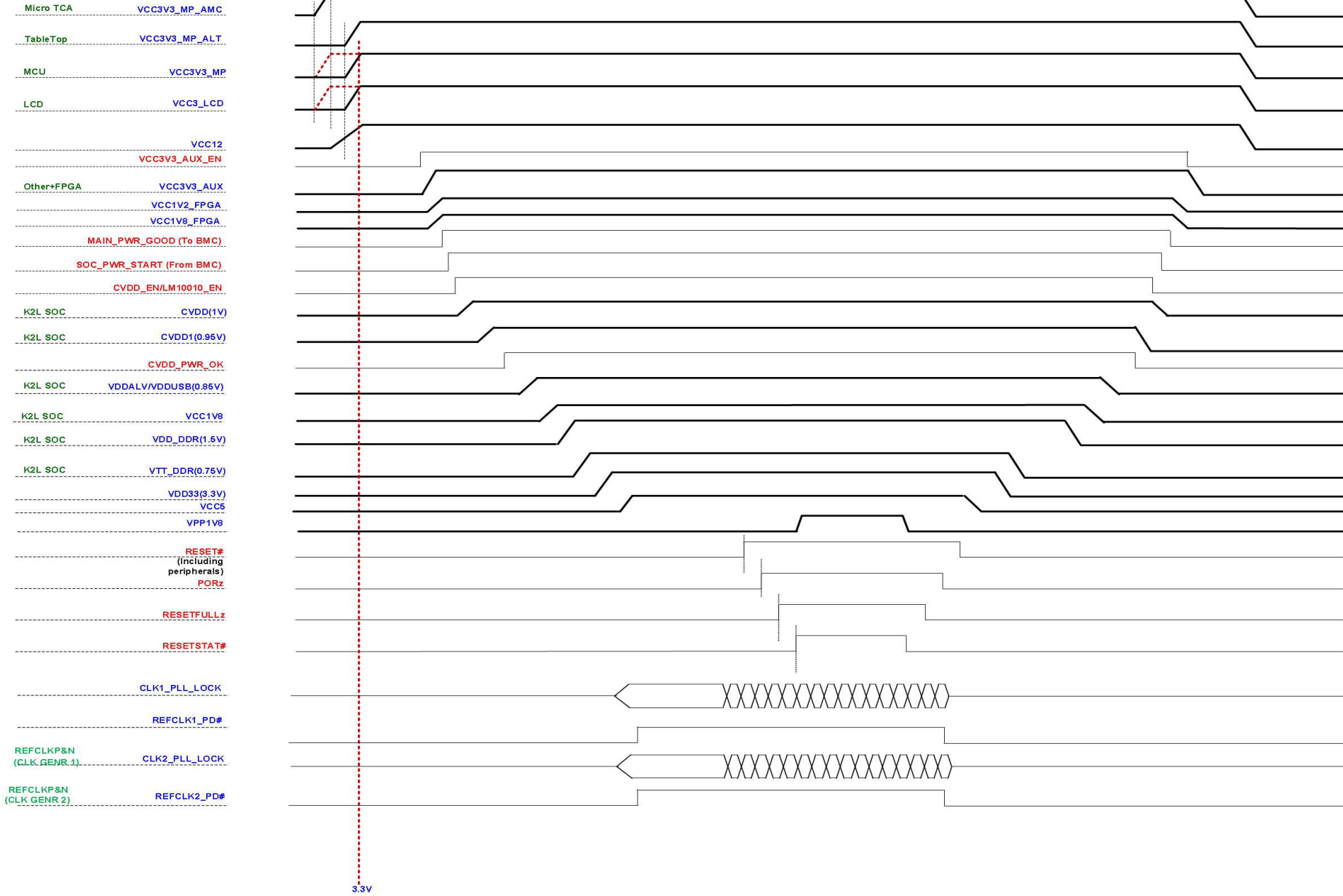
TPS544C24 -- 12V to 1V regulation	1962.94
LM26430-1(SW1) -- 12V to 0.95V regulation	287.65
TLV1117-33CDCY -- 12V to 3.3V BMC (LDO) regulation	148.50
TPS54620 -- 12V to 1.5V regulation	751.76
LM26430-1(SW3) -- 12V to 0.85V Analog SoC regulation	62.13
TPS54620-- 12V to 1.8V Analog regulation	112.76
TPS51200 -- 1.5 to 0.75V DDR regulation	1065.00
LM26430-1(SW4) -- 12V to 0.85V USB SoC regulation	71.00
LM26430-1(SW2) -- 12V to 1.8V Digital regulation	240.79
TPS54620 -- 12V to 3.3V Others regulation	1101.76
TPS54620 -- 12V to 5V regulation	540.85
APL431LBAI-TRG -- 3.3V to 3V regulation	47.93
LDO -- 3.3V OTH to 1.2V FPGA (LDO) - regulation	95.85
LDO -- 3.3V OTH to 1.8V FPGA (LDO) - regulation	302.50
Total Current @ 12V	6.98A
Total Power :	83.81W
Total Current @5V	1103.34
Total Current @3.3V	3155.60
Total Current @1.5V	5112.00

Note :

- 1) Above power consumption considers major block of design and provides indicative figure only.
- 2) Power rail assignment to different regulator is tentative based on power consumption, this can be changed based on sequence requirement.
- 3) Total power consumption is system is higher than AMC power(80W), we assume that marconi EVM will be connected only when board is running on external power supply.

Project K2L EVM		Designed for TI by elnfochips	
Title POWER CONSUMPTION		  The Solutions People	
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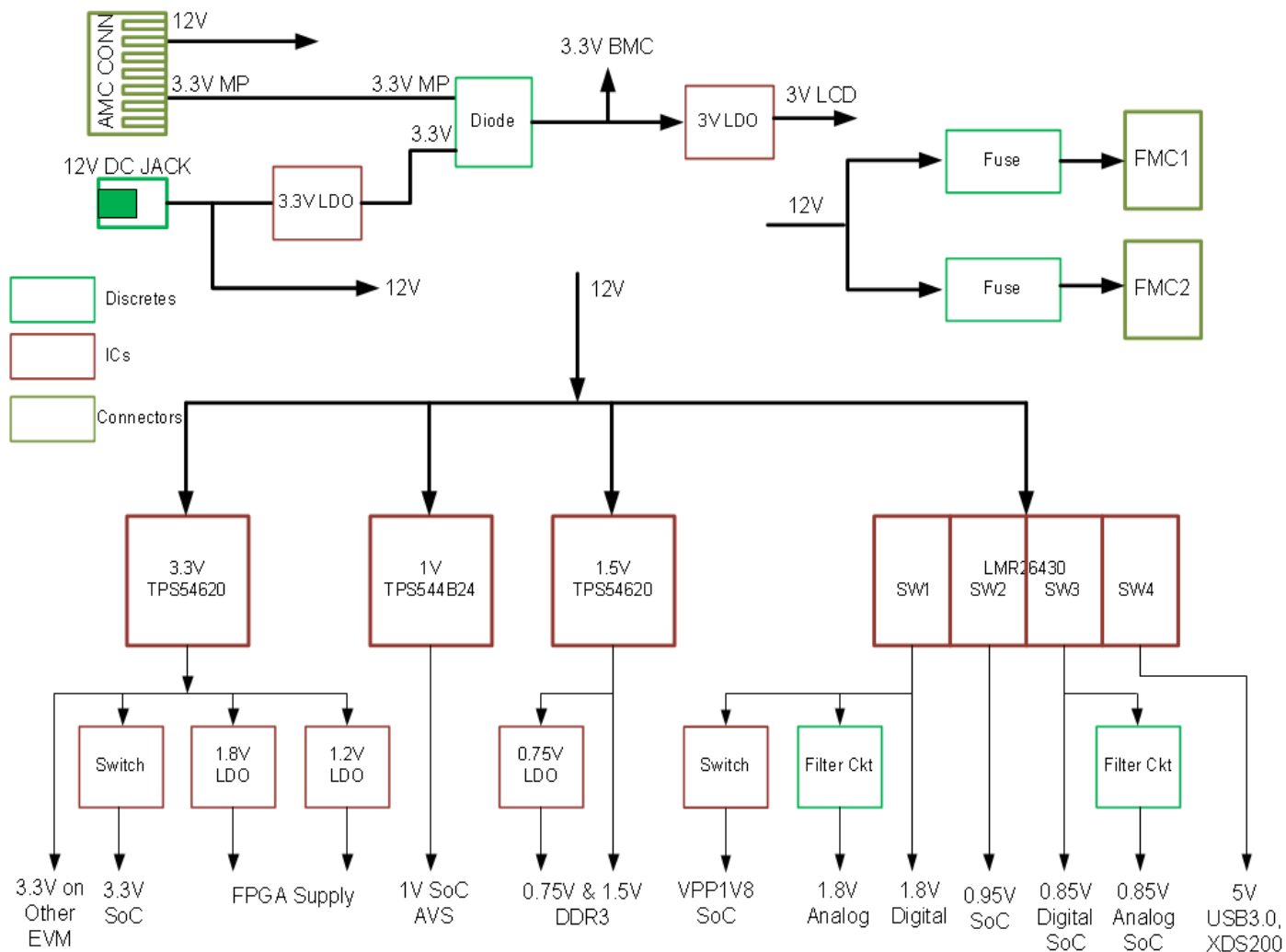
POWER SEQUENCE



Project K2L EVM		Designed for TI by elnfochips	
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POWER DISTRIBUTION

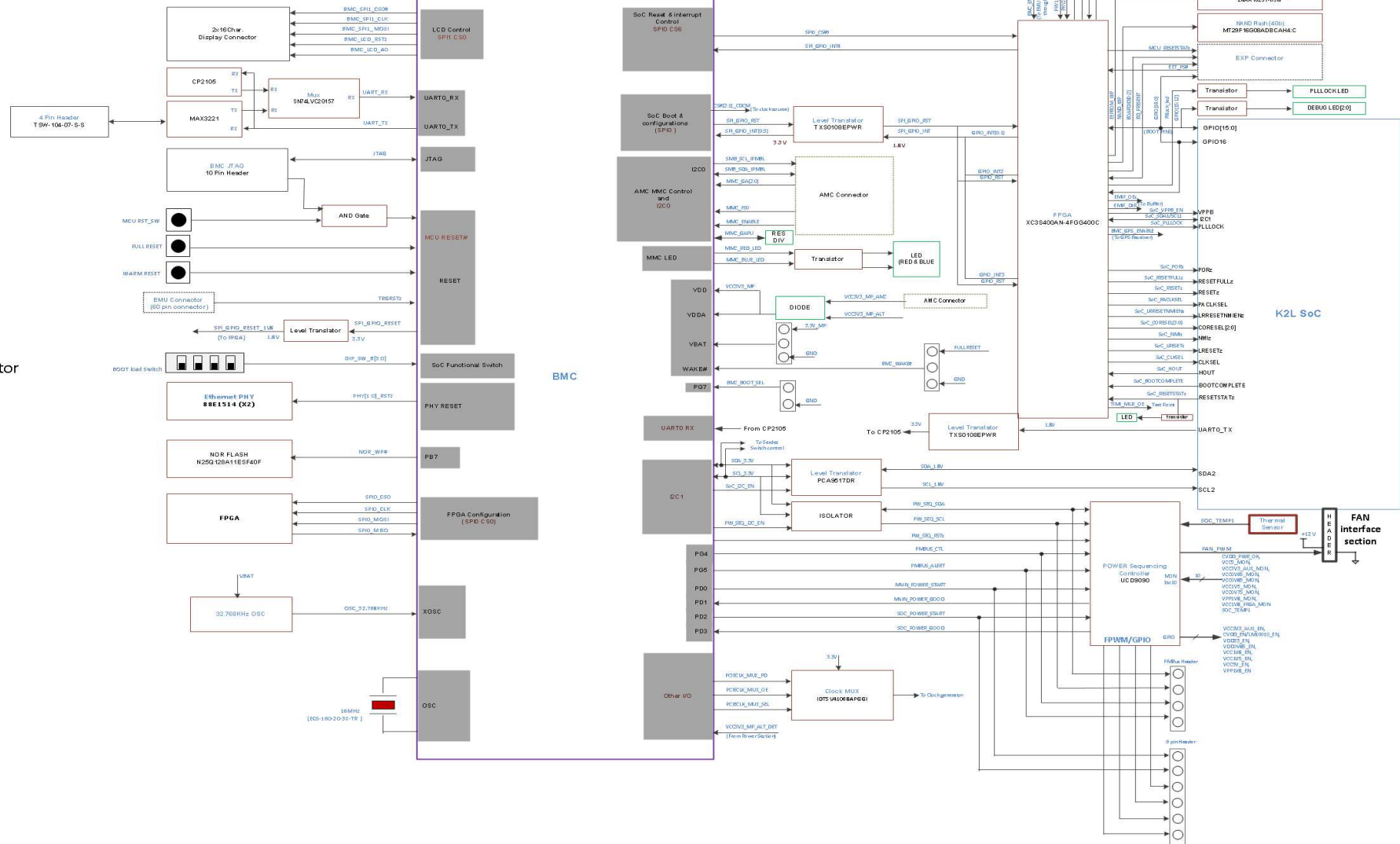
Power Supply Block Diagram



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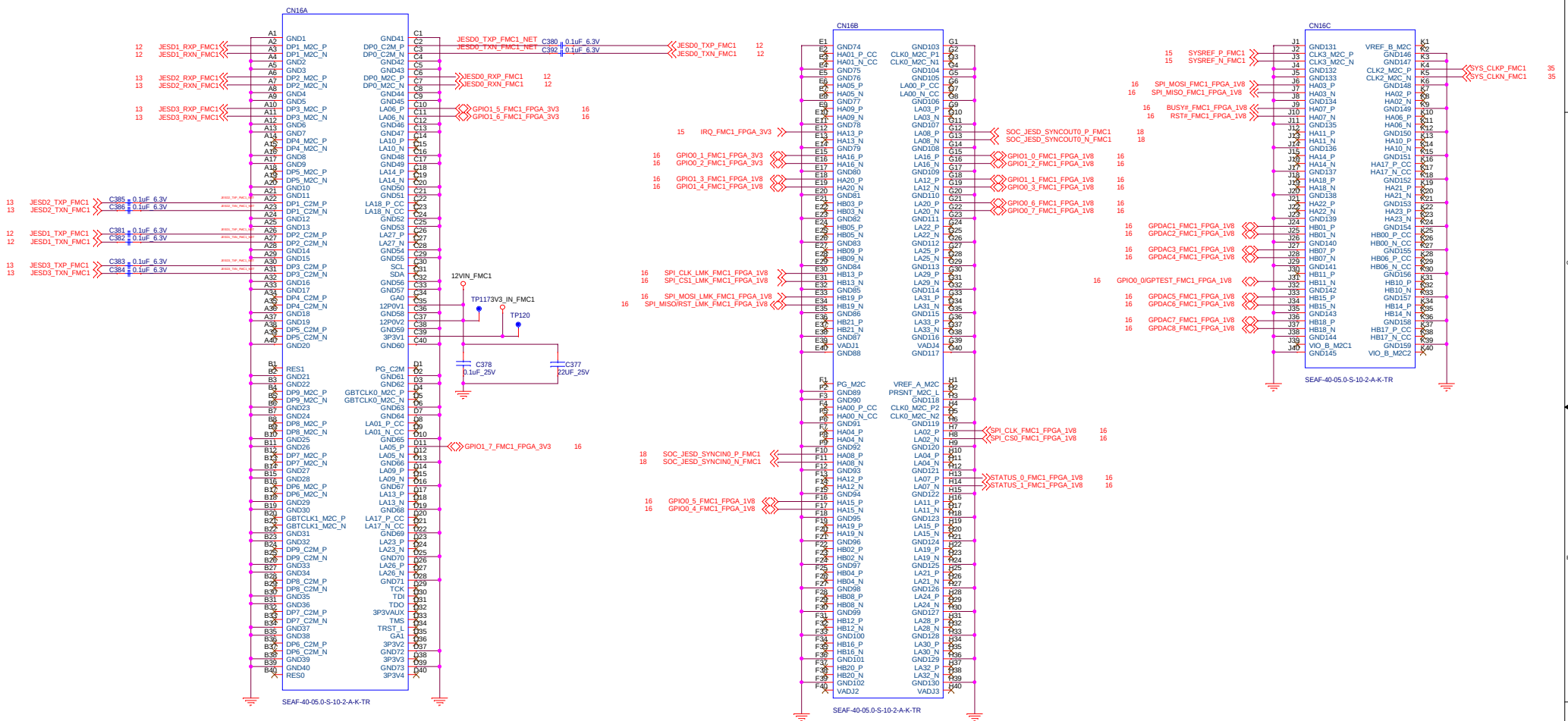


BMC SECTION



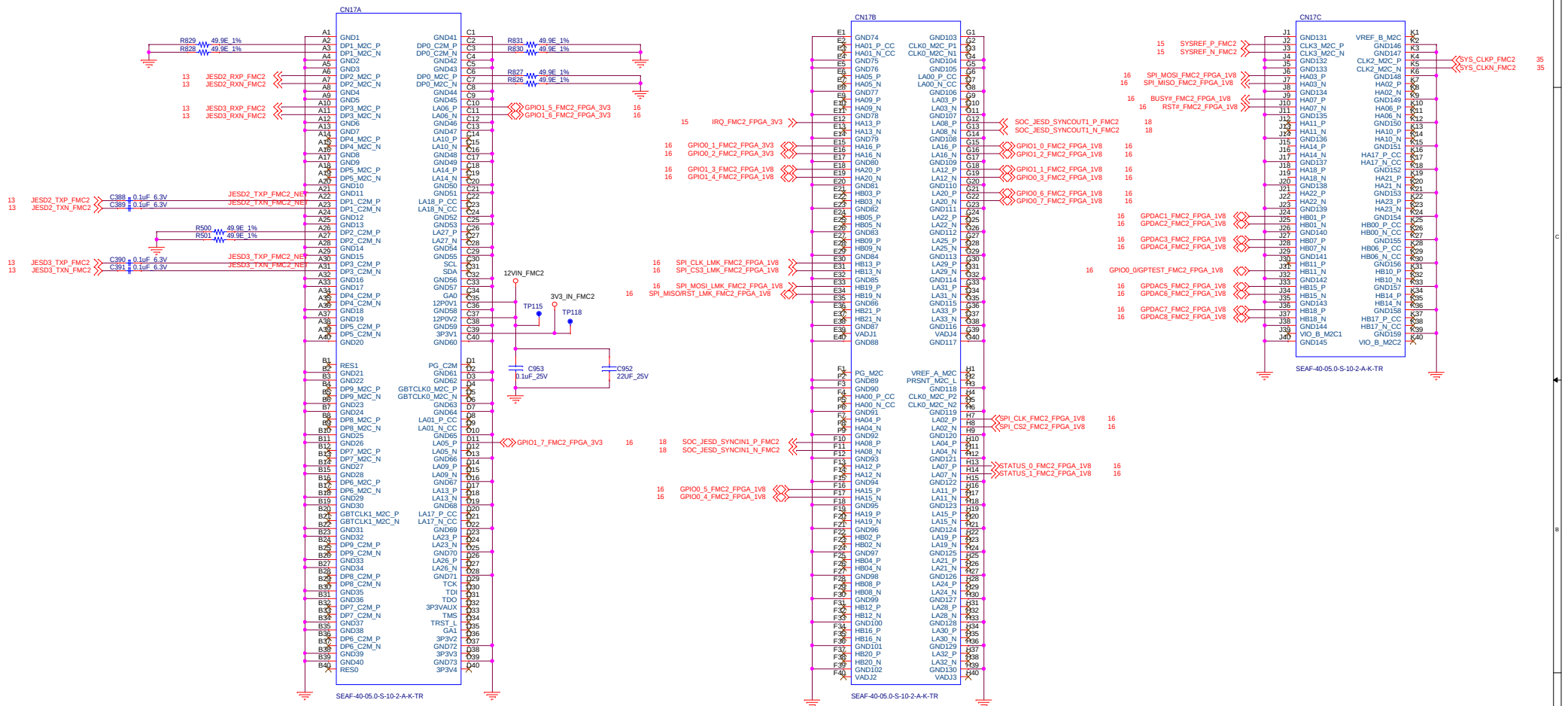
Project K2E EVM		Designed for TI by elfinfochips	
Title BMC BLOCK DIAGRAM		  The Solutions People	
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FMC Interface to JESD/RF devices - 1



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FMC Interface to JESD/RF devices - 2



Project K2L EVM		Designed for TI by elfinochips	
Title FMC Interface to JESD/RF devices - 2		  The Solutions People	
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JESD Serdes switch - 1

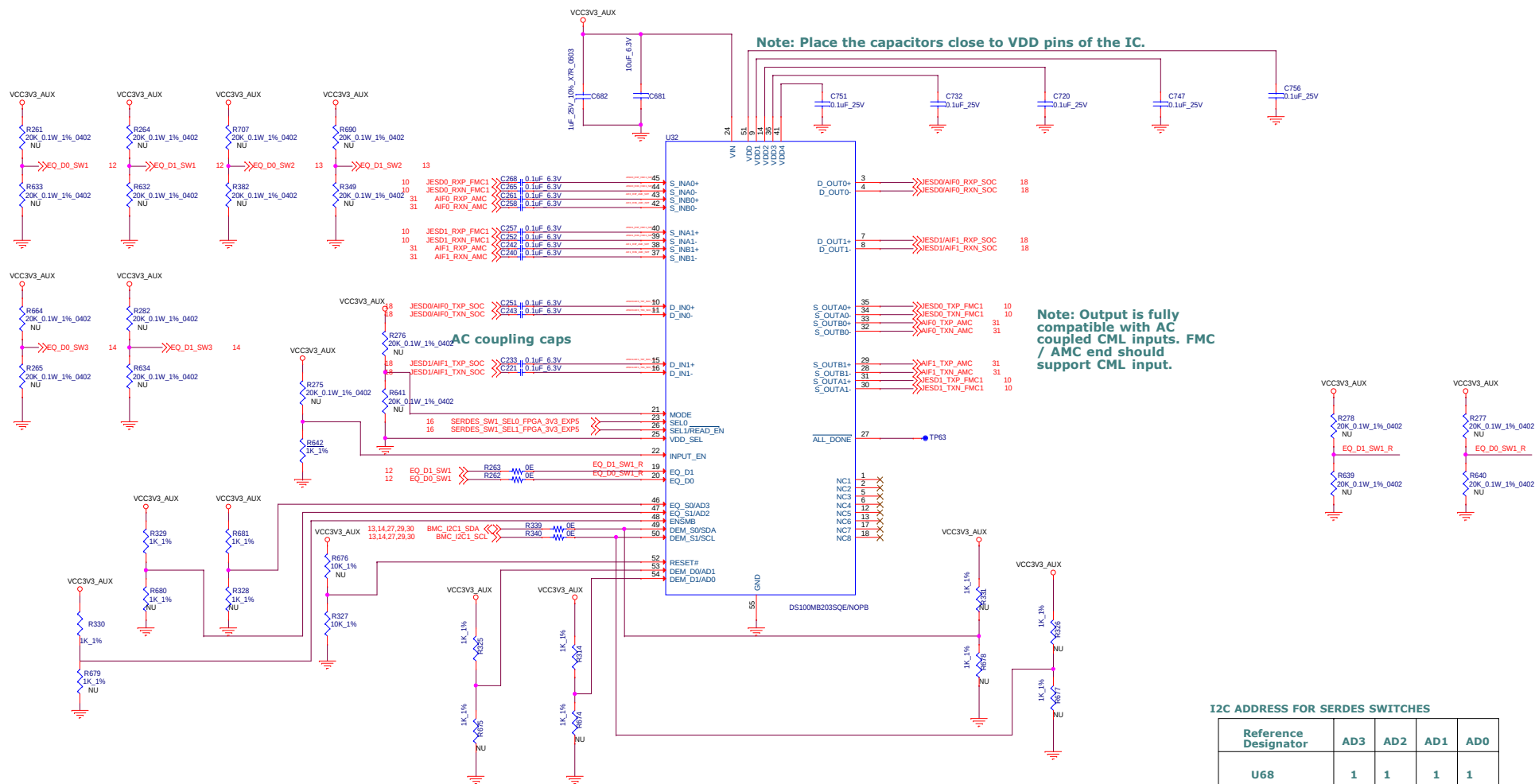


TABLE FOR SERDES CONNECTIONS

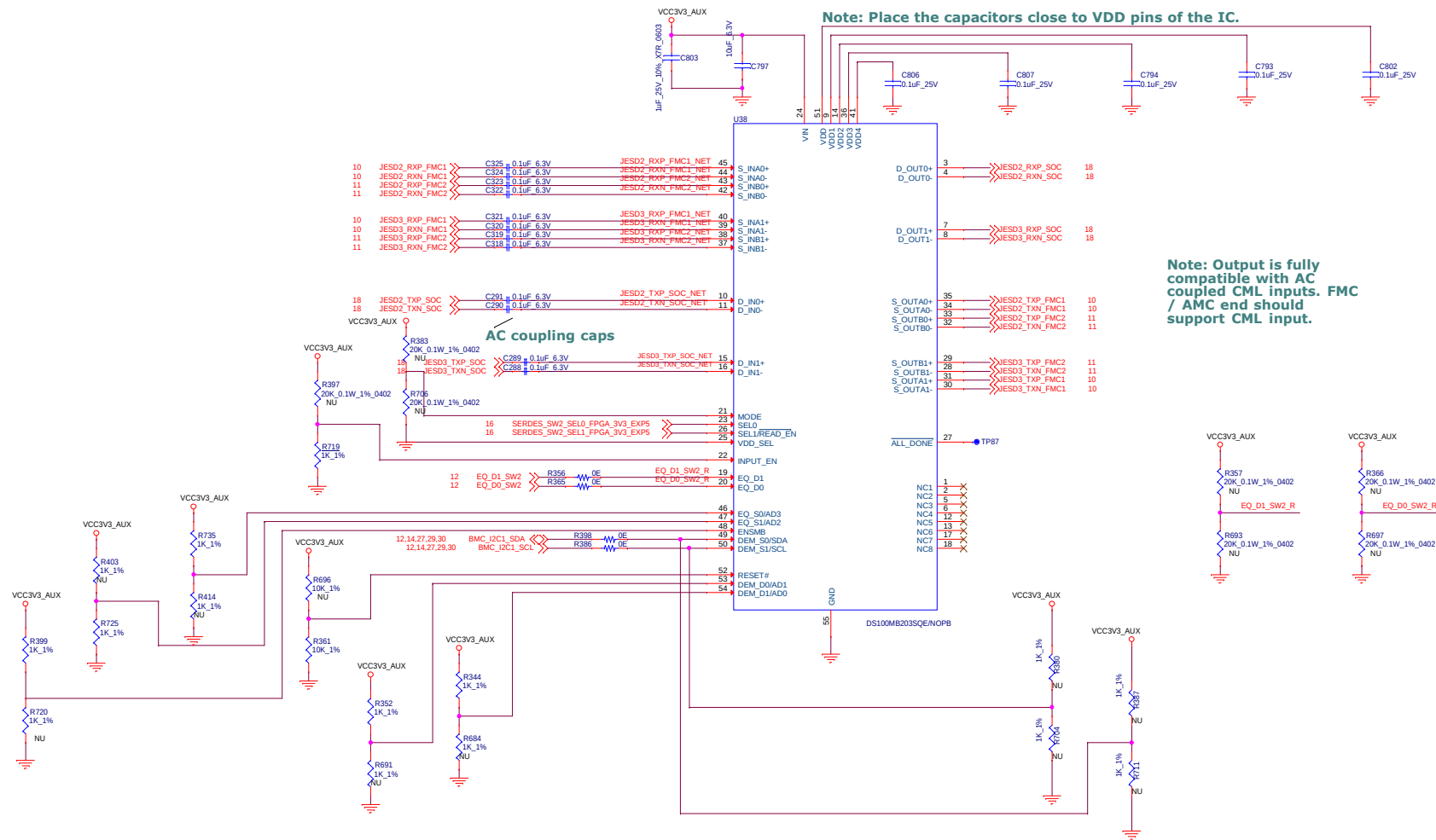
Lamarr Ballname	Lamarr Direction	Lamarr Ball	Lamarr SOC Net name to switch	Sw/SOC	Switch Inputs	Switch Outputs	FMC1 Name	FMC1 Pin	FMC2 Name	FMC2 Pin	Marconi Name	AMC Name	AMC Pin
CSISC2_0_RXN0	Diff In	AJ19	JESD0/AIF0_RXN_SOC	Sw Out	JESD0_RXN_FMC1 or AIF0_RXN_AMC	-	JESD0_RXN_FMC1	C7			TXN_S1	AIF0_RXN_AMC	141
CSISC2_0_RXP0	Diff In	AJ18	JESD0/AIF0_RXP_SOC	Sw Out	JESD0_RXP_FMC1 or AIF0_RXP_AMC	-	JESD0_RXP_FMC1	C6			TXP_S1	AIF0_RXP_AMC	142
CSISC2_0_RXN1	Diff In	AK20	JESD1/AIF1_RXN_SOC	Sw Out	JESD1_RXN_FMC1 or AIF1_RXN_AMC	-	JESD1_RXN_FMC1	A3			TXN_S2	AIF1_RXN_AMC	147
CSISC2_0_RXP1	Diff In	AK19	JESD1/AIF1_RXP_SOC	Sw Out	JESD1_RXP_FMC1 or AIF1_RXP_AMC	-	JESD1_RXP_FMC1	A2			TXP_S2	AIF1_RXP_AMC	148
CSISC2_0_TXN0	Diff Out	AH17	JESD0/AIF0_TXN_SOC	Sw In		JESD0_TXN_FMC1 or AIF0_TXN_AMC	JESD0_TXN_FMC1	C3	NU	C3	RXN_S1	AIF0_TXN_AMC	144
CSISC2_0_TXP0	Diff Out	AH18	JESD0/AIF0_TXP_SOC	Sw In		JESD0_TXP_FMC1 or AIF0_TXP_AMC	JESD0_TXP_FMC1	C2	NU	C2	RXP_S1	AIF0_TXP_AMC	145
CSISC2_0_TXN1	Diff Out	AG18	JESD1/AIF1_TXN_SOC	Sw In		JESD1_TXN_FMC1 or AIF1_TXN_AMC	JESD1_TXN_FMC1	A27	NU	A27	RXN_S2	AIF1_TXN_AMC	150
CSISC2_0_TXP1	Diff Out	AG19	JESD1/AIF1_TXP_SOC	Sw In		JESD1_TXP_FMC1 or AIF1_TXP_AMC	JESD1_TXP_FMC1	A26	NU	A26	RXP_S2	AIF1_TXP_AMC	151

I2C ADDRESS FOR SERDES SWITCHES

Reference Designator	AD3	AD2	AD1	AD0
U68	1	1	1	1
U69	1	0	1	1
U70	0	1	1	1

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Title JESD Serdes switch - 1			
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JESD Serdes switch - 2



SGMII/PCIe Serdes switch

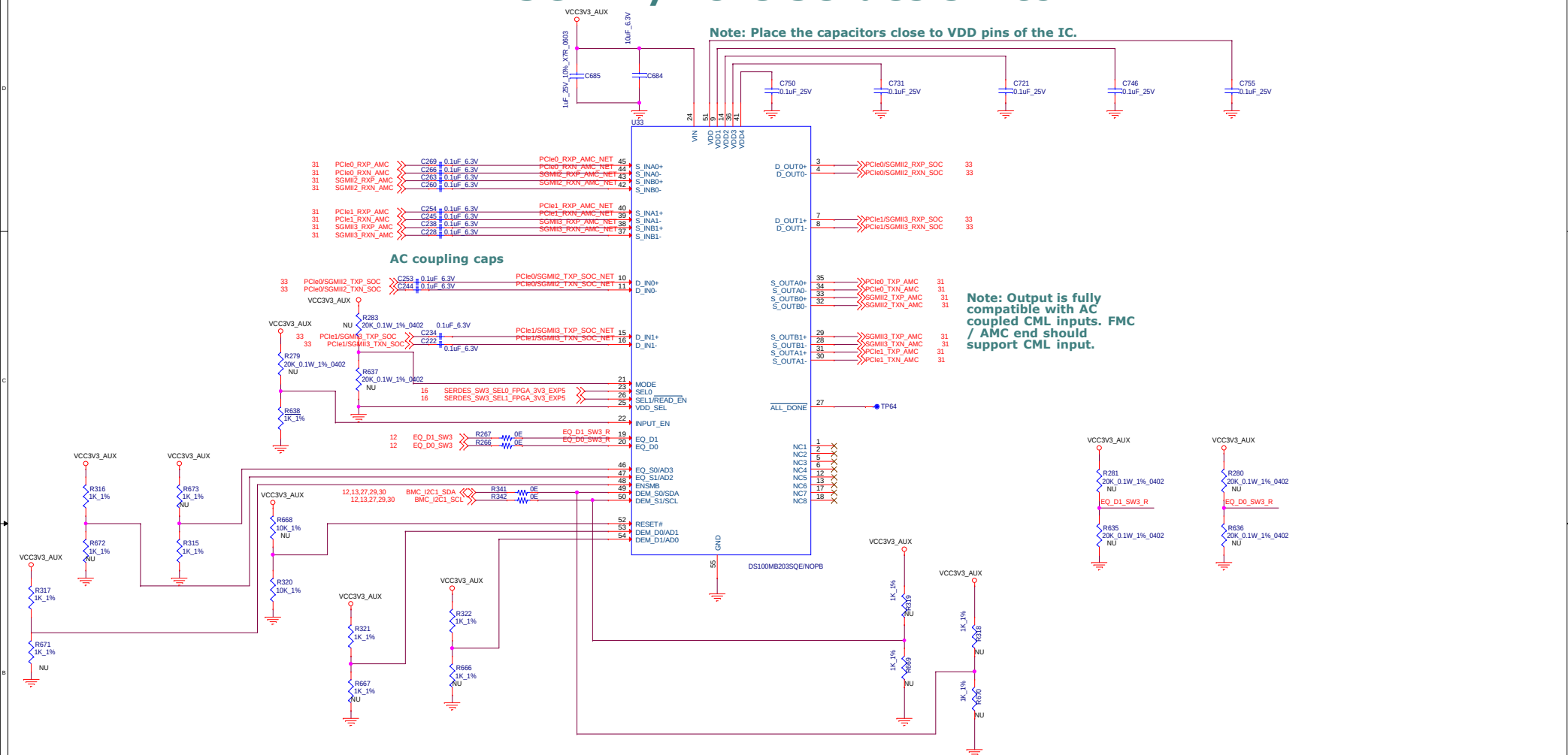
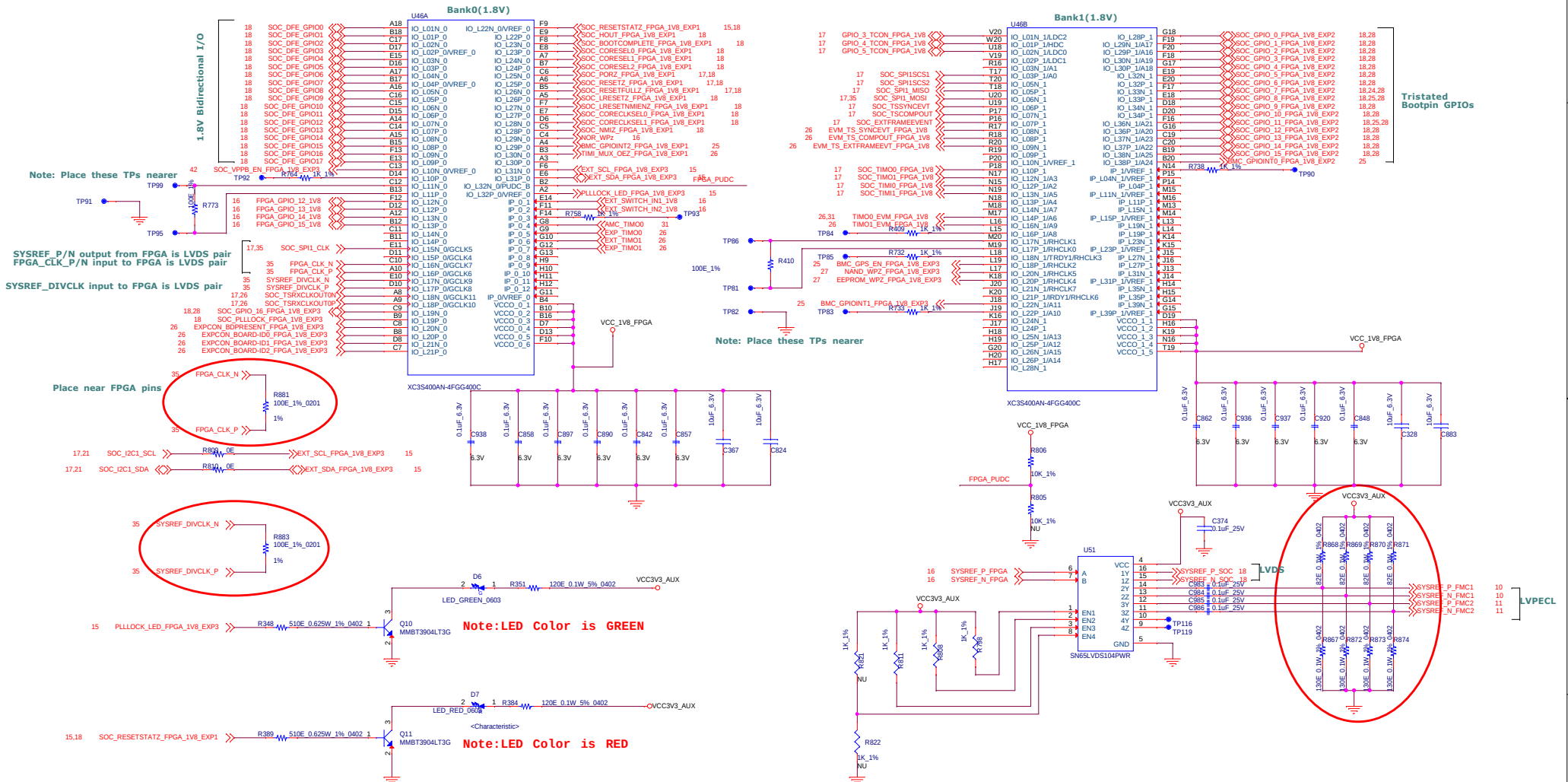


TABLE FOR SERDES CONNECTIONS

Lamarr Ballname	Lamarr Direction	Lamarr Ball	Lamarr SOC Net name to switch	Sw/SOC	Switch Inputs	Switch Outputs	AMC PCIe conn	AMC Pin	AMC SGMII conn	AMC Pin
CSISC2_3_RXN0	Diff In	AJ22	PCIe0/SGMII2_RXN_SOC	Sw Out	PCIe0_RXN_AMC or SGMII2_RXN_AMC	-	PCIe0_RXN_AMC	48	SGMII2_RXN_AMC	15
CSISC2_3_RXP0	Diff In	AJ21	PCIe0/SGMII2_RXP_SOC	Sw Out	PCIe0_RXP_AMC or SGMII2_RXP_AMC	-	PCIe0_RXP_AMC	47	SGMII2_RXP_AMC	14
CSISC2_3_RXN1	Diff In	AK23	PCIe1/SGMII3_RXN_SOC	Sw Out	PCIe1_RXN_AMC or SGMII3_RXN_AMC	-	PCIe1_RXN_AMC	63	SGMII3_RXN_AMC	24
CSISC2_3_RXP1	Diff In	AK22	PCIe1/SGMII3_RXP_SOC	Sw Out	PCIe1_RXP_AMC or SGMII3_RXP_AMC	-	PCIe1_RXP_AMC	62	SGMII3_RXP_AMC	23
CSISC2_1_TXN0	Diff Out	AH20	PCIe0/SGMII2_TXN_SOC	Sw In	-	PCIe0_TXN_AMC or SGMII2_TXN_AMC	PCIe0_TXN_AMC	45	SGMII2_TXN_AMC	12
CSISC2_1_TXP0	Diff Out	AH21	PCIe0/SGMII2_TXP_SOC	Sw In	-	PCIe0_TXP_AMC or SGMII2_TXP_AMC	PCIe0_TXP_AMC	44	SGMII2_TXP_AMC	11
CSISC2_1_TXN1	Diff Out	AG21	PCIe1/SGMII3_TXN_SOC	Sw In	-	PCIe1_TXN_AMC or SGMII3_TXN_AMC	PCIe1_TXN_AMC	60	SGMII3_TXN_AMC	21
CSISC2_1_TXP1	Diff Out	AG22	PCIe1/SGMII3_TXP_SOC	Sw In	-	PCIe1_TXP_AMC or SGMII3_TXP_AMC	PCIe1_TXP_AMC	59	SGMII3_TXP_AMC	20

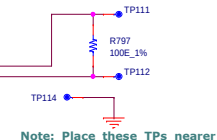
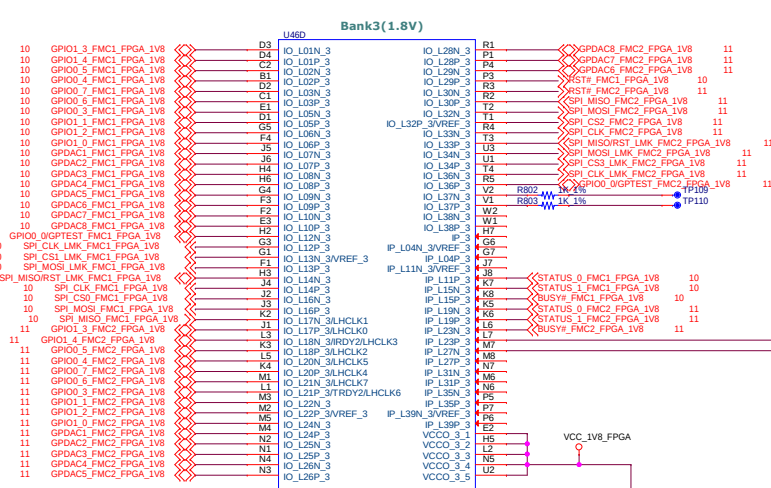
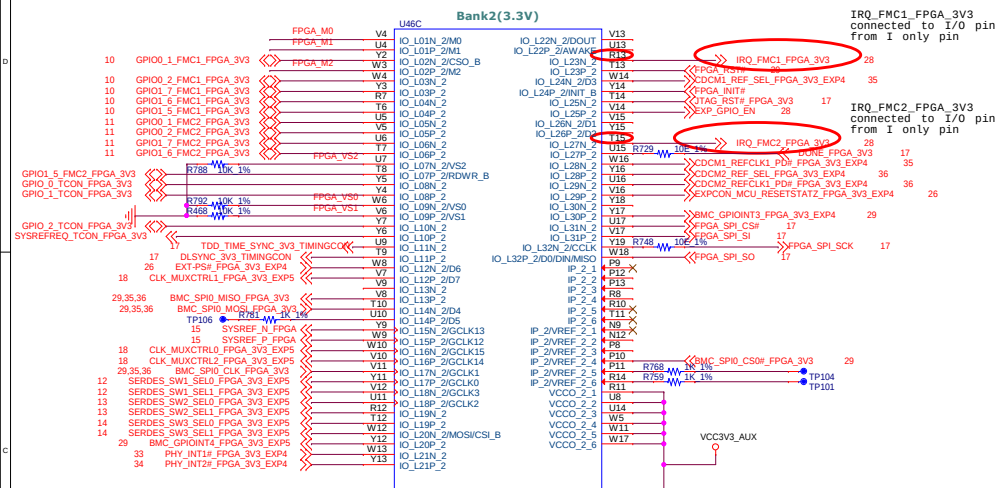
Project K2L EVM		Designed for TI by elnfochips	
Title SGMII/PCIe Serdes switch		 TEXAS INSTRUMENTS  The Solutions People	
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FPGA, SYSREF Buffering, LEDs

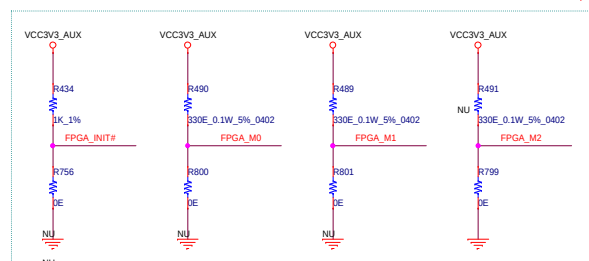
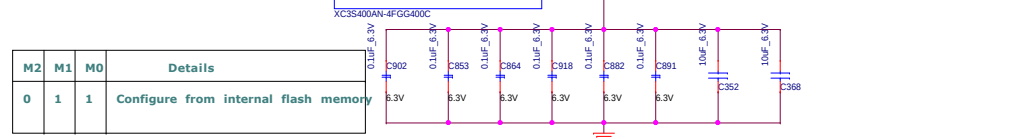


Project		K2L EVM		Designed for TI by elfinochips	
Title		FPGA, SYSREF Buffering, LEDs		 TEXAS INSTRUMENTS  The Solutions People	
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FPGA, FPGA 2pin conn, SPI Flash, LEDs

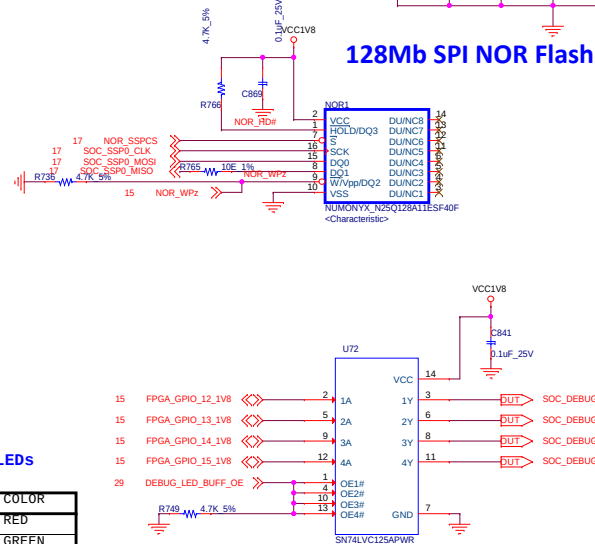
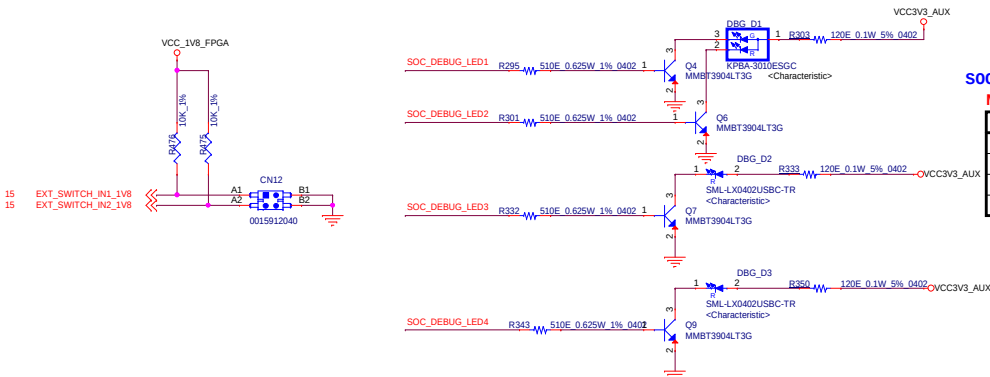


Note: Place these TPs nearer



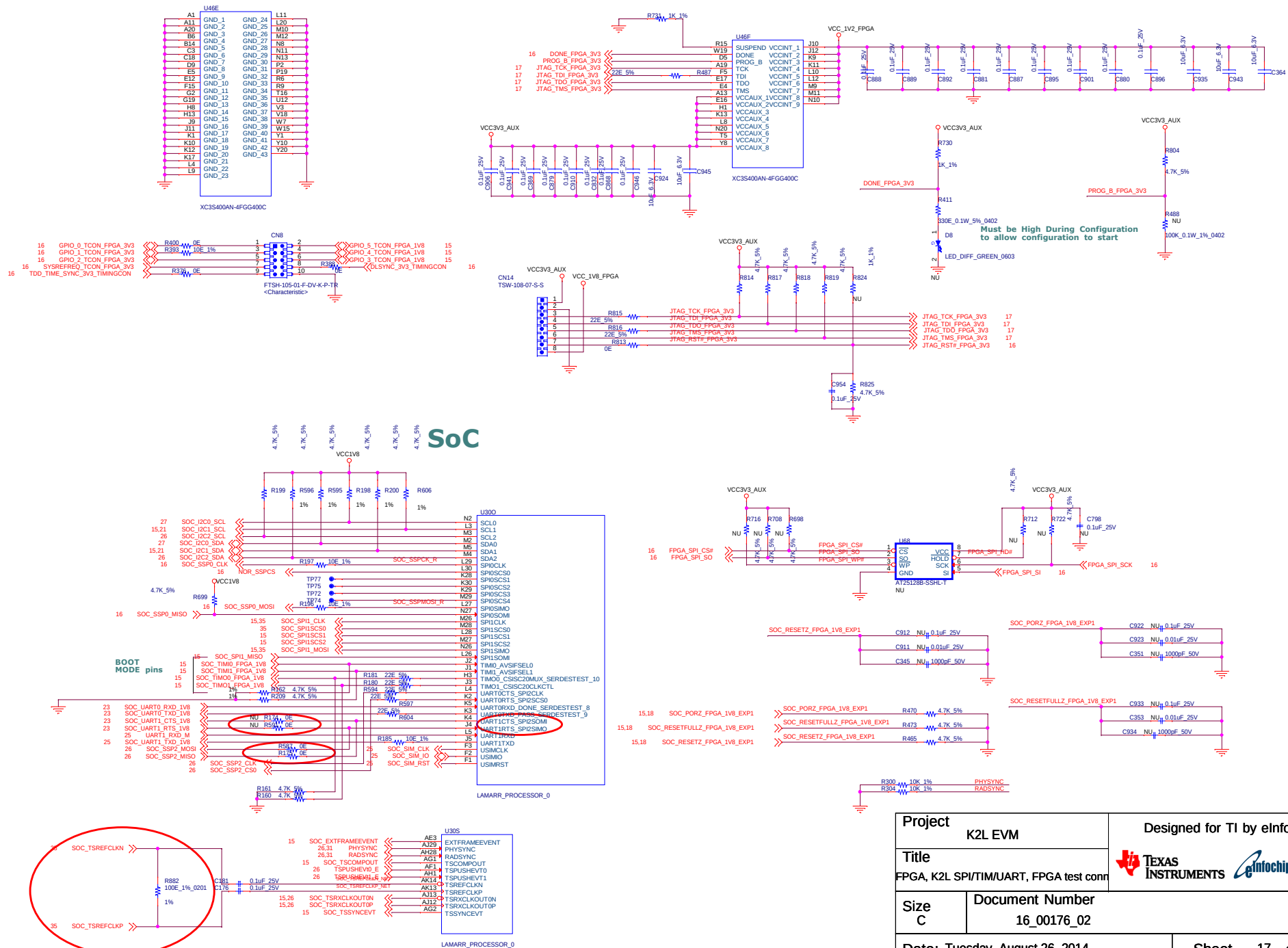
Note:

	COLOR
LED1	RED
LED2	GREEN
LED3	BLUE
LED4	BLUE



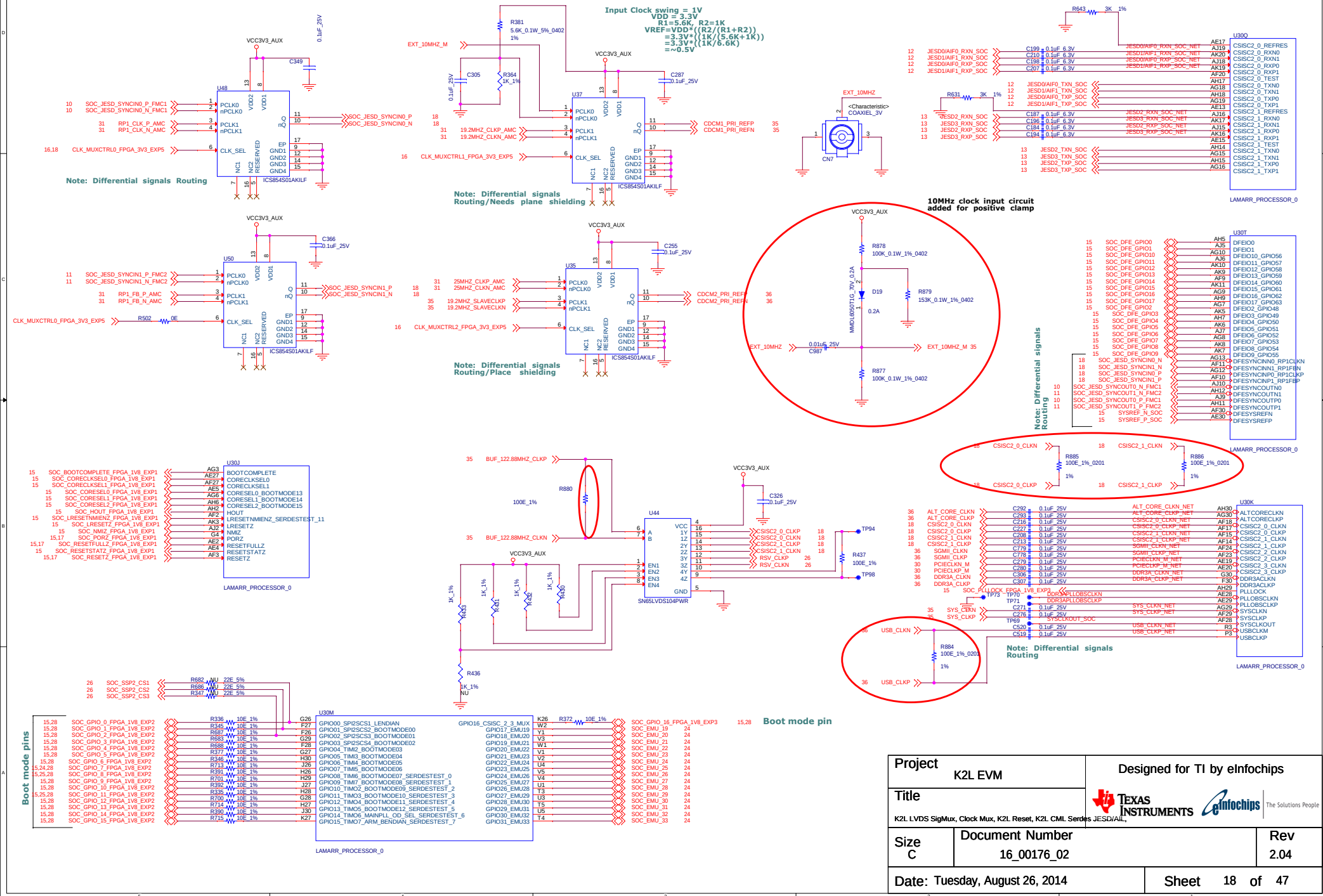
Project K2L EVM		Designed for TI by elfinfochips	
Title FPGA, FPGA 2pin conn, SPI Flash, LEDs		  The Solutions People	
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FPGA, FPGA JTAG, FPGA-Flash, FPGA Programmer, K2L SPI/TIM/UART, FPGA test conn

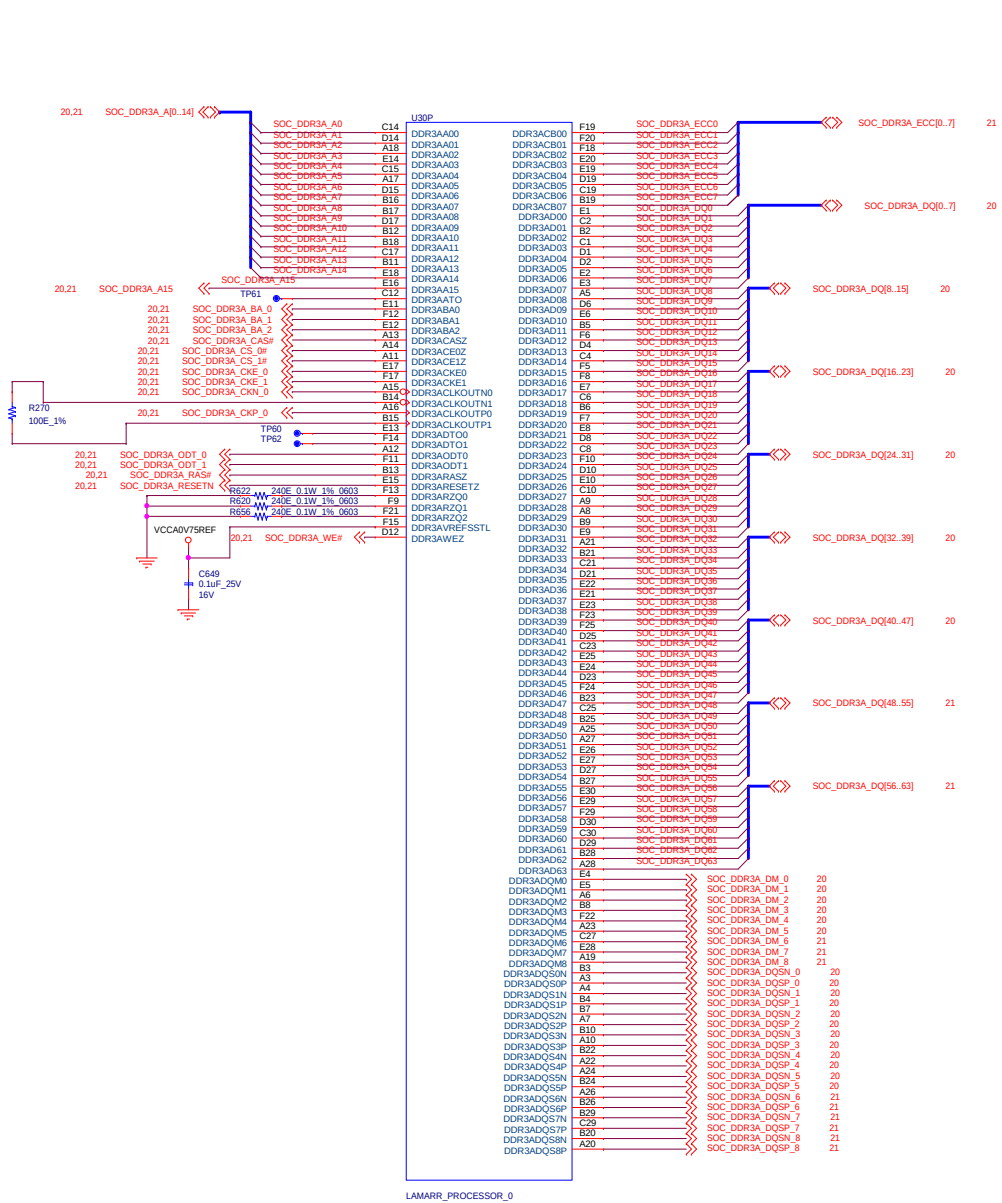


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Title FPGA, K2L SPI/TIM/UART, FPGA test contr		  The Solutions People	
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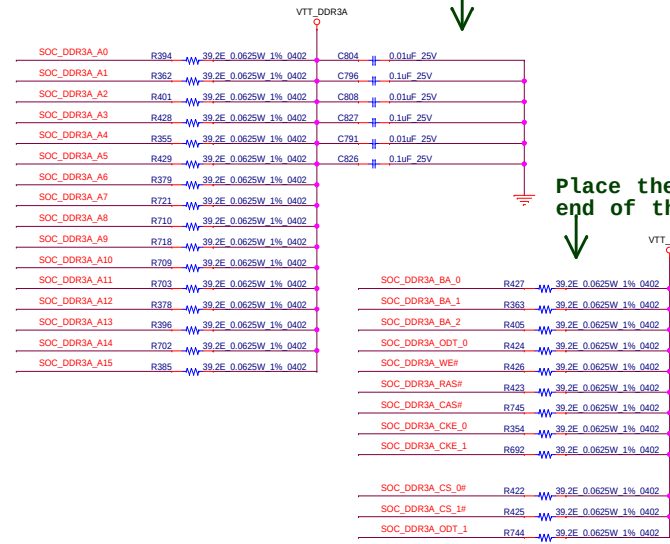
K2L LVDS SigMux, Clock Mux, K2L Reset, K2L CML Serdes JESD/AIL, K2L DFE GPIO, K2L DFE Syncs/SysRef, K2L Clkin



K2L DDR3



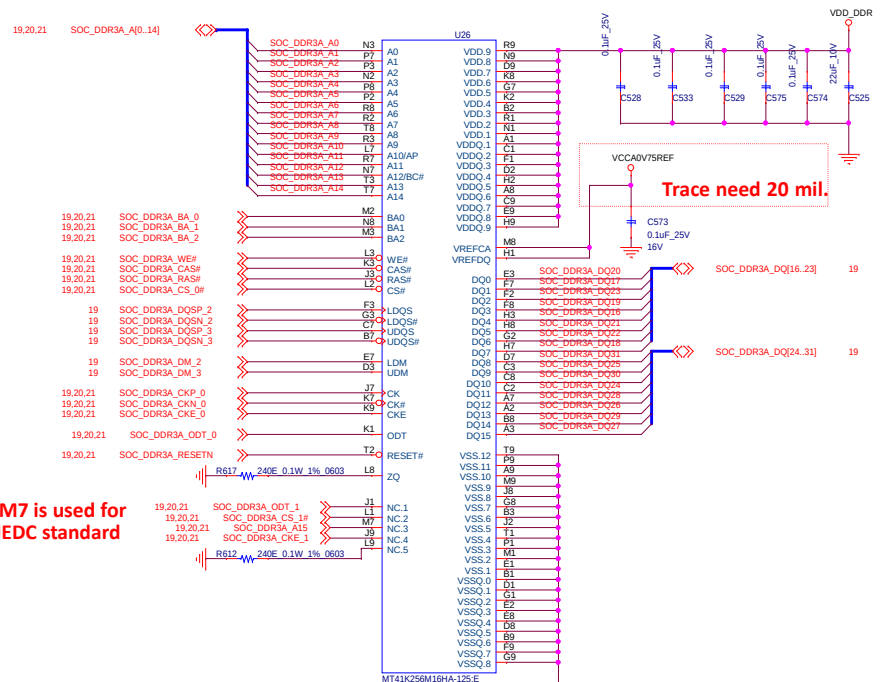
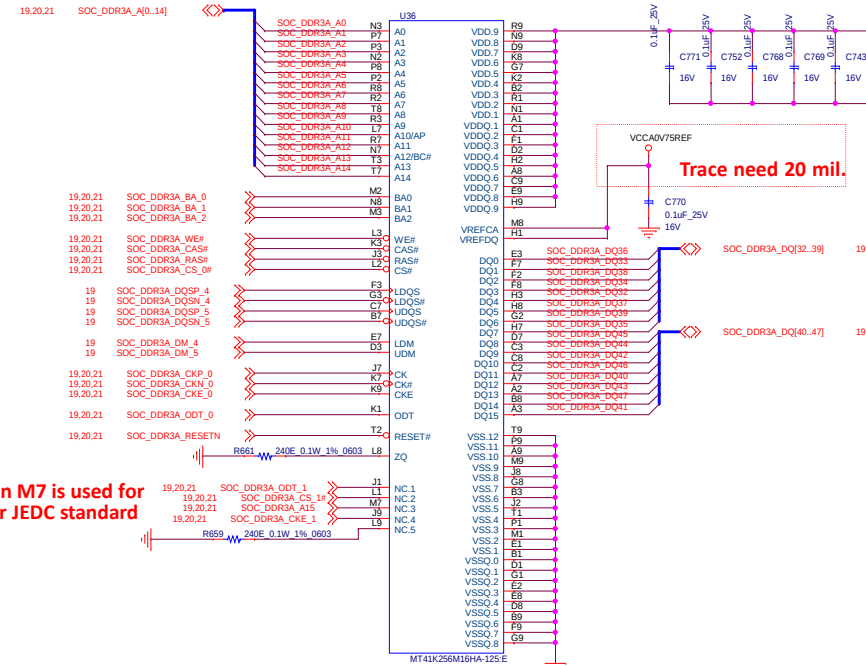
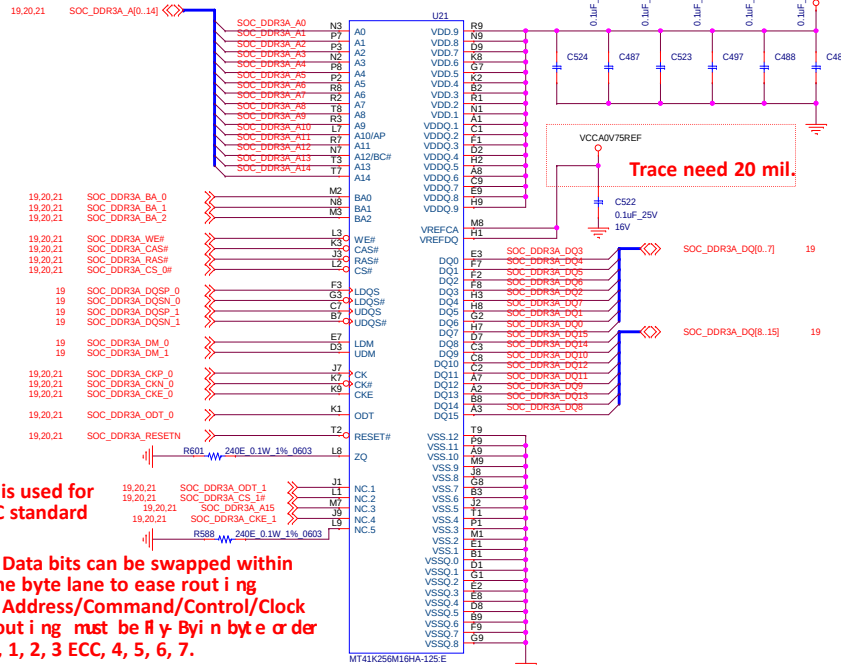
Place these resistors at the end of the trace.



Place these resistors at the end of the trace.

Project K2L EVM		Designed for TI by einfochips	
Title K2L DDR3		 TEXAS INSTRUMENTS  The Solutions People	
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 19 of 47	

DDR3(3)



Project K2L EVM		Designed for TI by elfinfochips	
Title DDR3(3)		 TEXAS INSTRUMENTS  The Solutions People	
Size C	Document Number 16_00176_02		Rev 2.04
Date: Tuesday, August 26, 2014		Sheet 20 of 47	

DDR3(2), 3.3vaux -> .75v DDR3 Vt, DDR3 SPD EEPROM

Trace need 20 mil.

*** DDR3 pin M7 is used for A15 as per JEDC standard**

DDR3-XXXX DiscreteSDRAM Array

FOR ECC USE

Trace needs 20 mil.

*** DDR3 pin M7 is used for A15 as per JEDC standard**

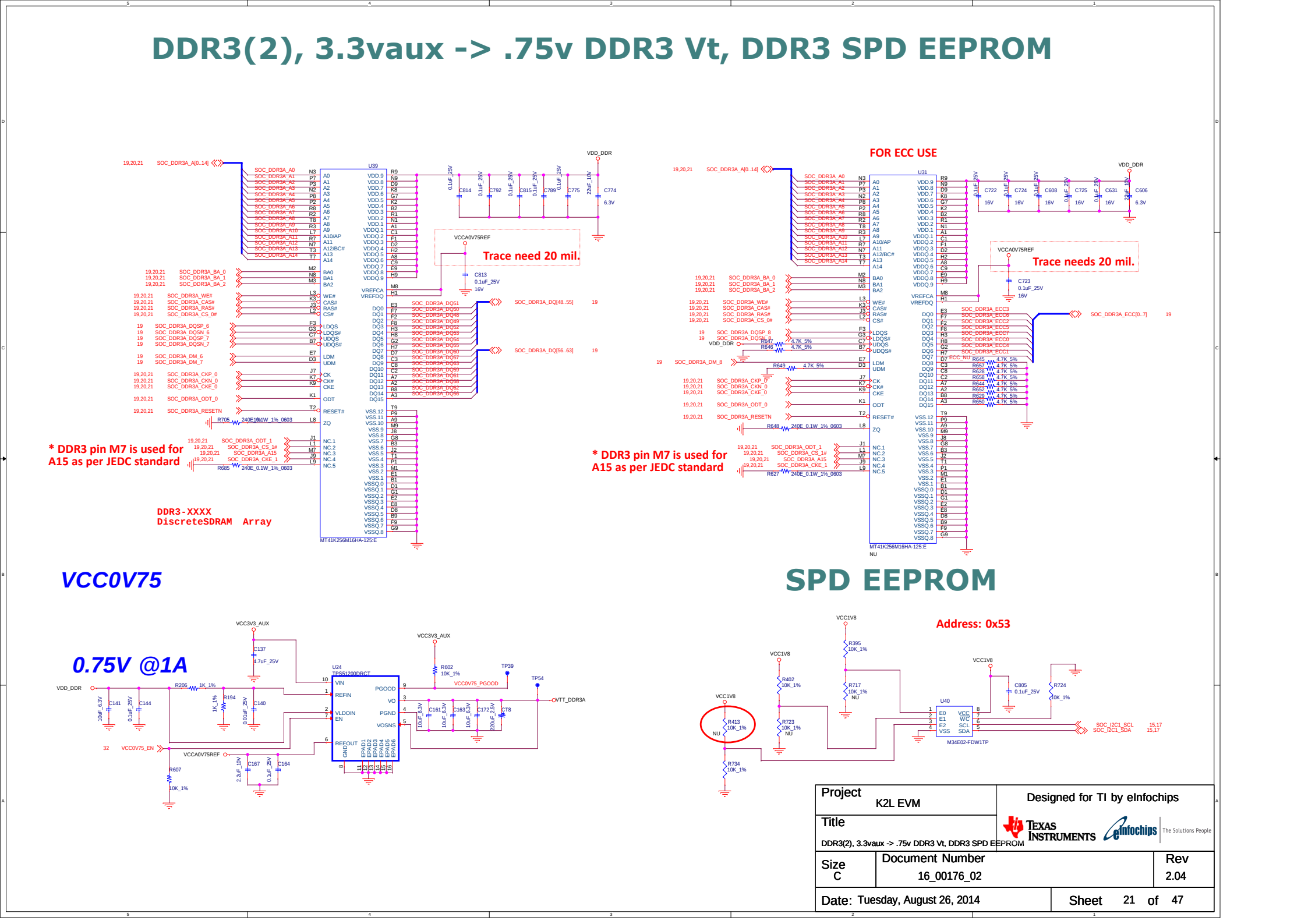
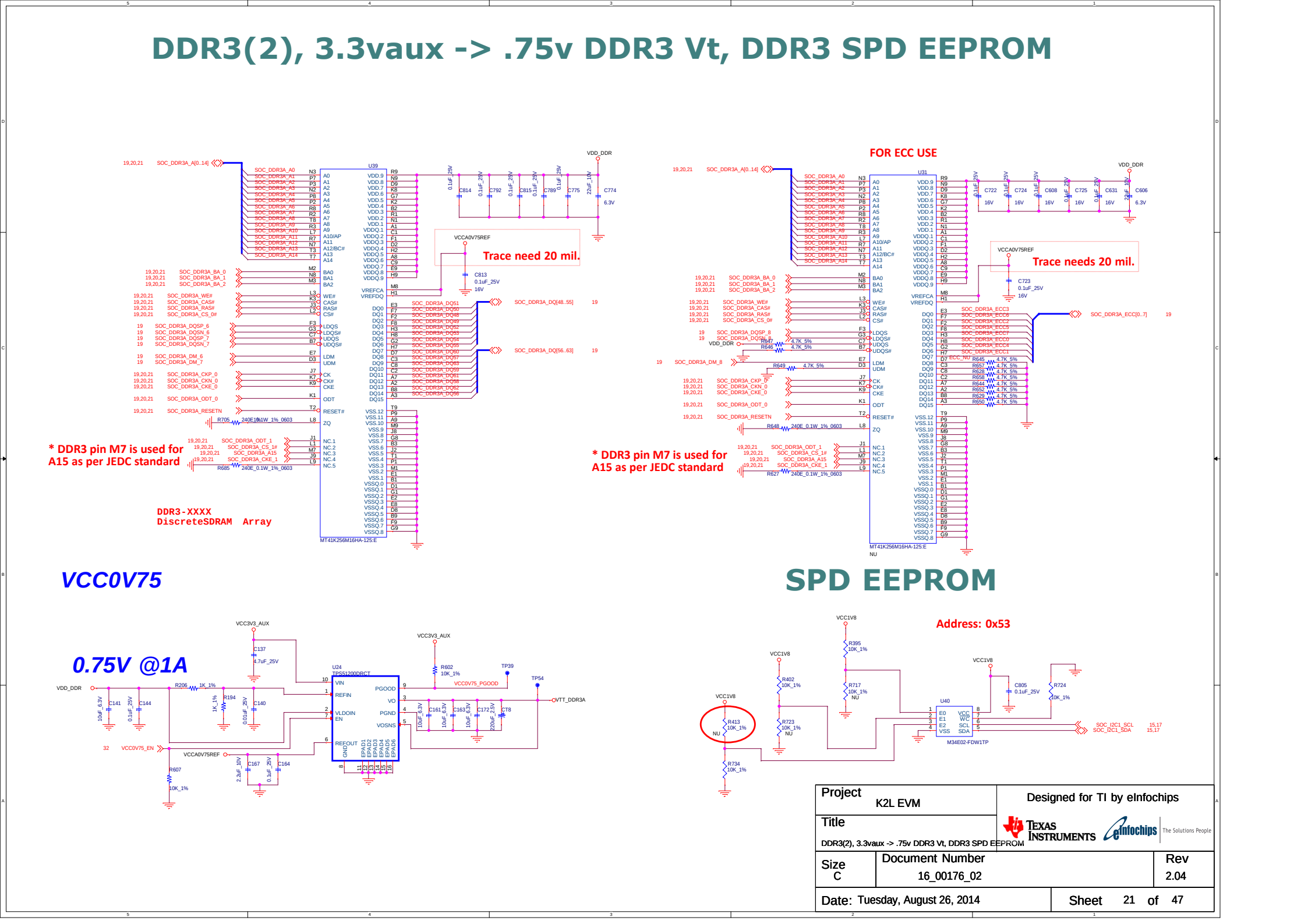
VCC0V75

0.75V @1A

SPD EEPROM

Address: 0x53

Project		Designed for TI by elfinichips	
K2L EVM			
Title		DDR3(2), 3.3vaux -> .75v DDR3 Vt, DDR3 SPD EEPROM	
Size C	Document Number	Rev	
	16_00176_02	2.04	
Date: Tuesday, August 26, 2014		Sheet 21 of 47	



DDR3(2), 3.3vaux -> .75v DDR3 Vt, DDR3 SPD EEPROM

Trace need 20 mil.

*** DDR3 pin M7 is used for A15 as per JEDC standard**

Trace needs 20 mil.

*** DDR3 pin M7 is used for A15 as per JEDC standard**

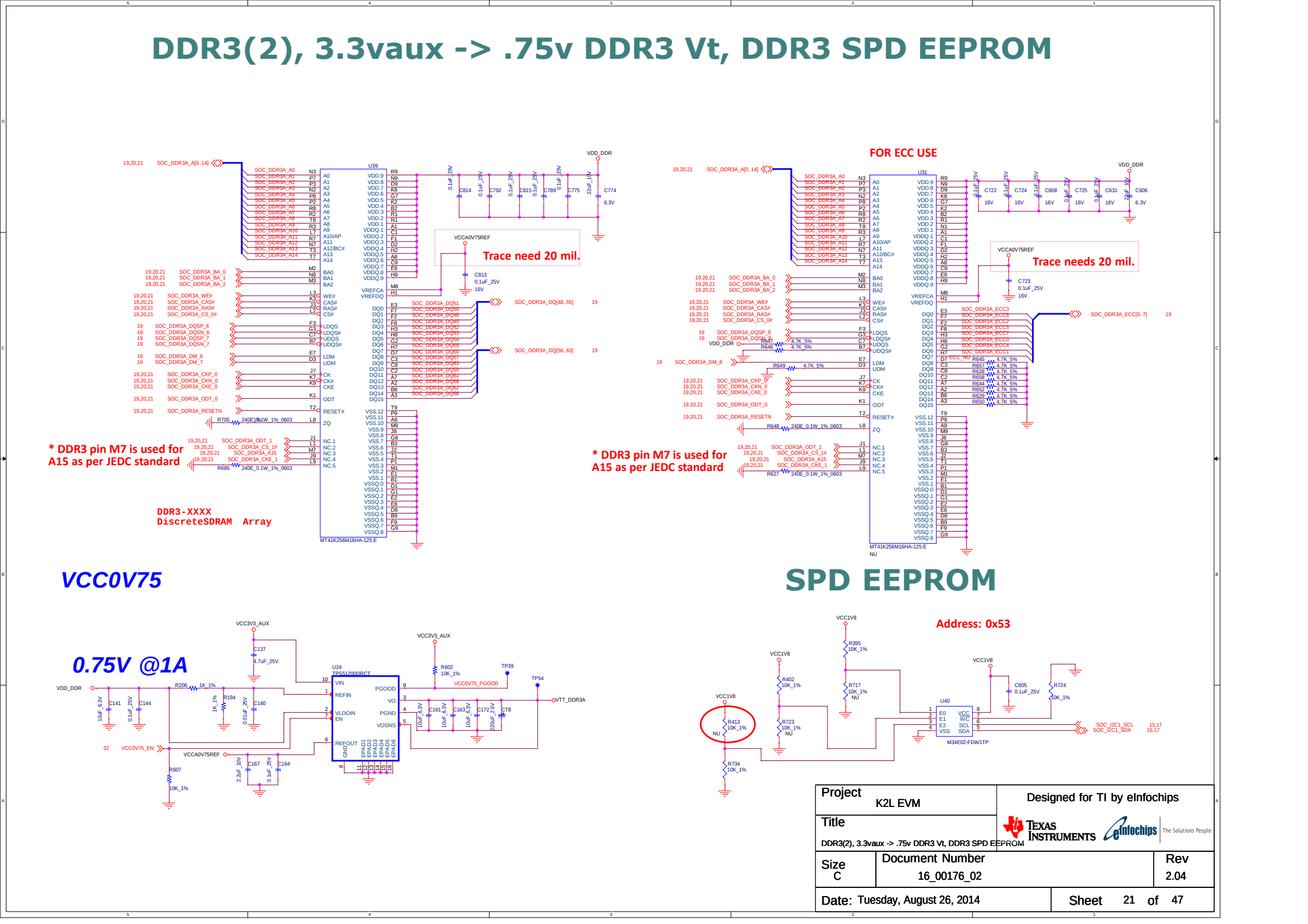
VCC0V75

0.75V @1A

SPD EEPROM

Address: 0x53

Project		Designed for TI by elfinichips	
K2L EVM			
Title		DDR3(2), 3.3vaux -> .75v DDR3 Vt, DDR3 SPD EEPROM	
Size	Document Number	Rev	
C	16_00176_02	2.04	
Date: Tuesday, August 26, 2014		Sheet 21 of 47	



DDR3(2), 3.3vaux -> .75v DDR3 Vt, DDR3 SPD EEPROM

Trace need 20 mil.

*** DDR3 pin M7 is used for A15 as per JEDC standard**

Trace needs 20 mil.

*** DDR3 pin M7 is used for A15 as per JEDC standard**

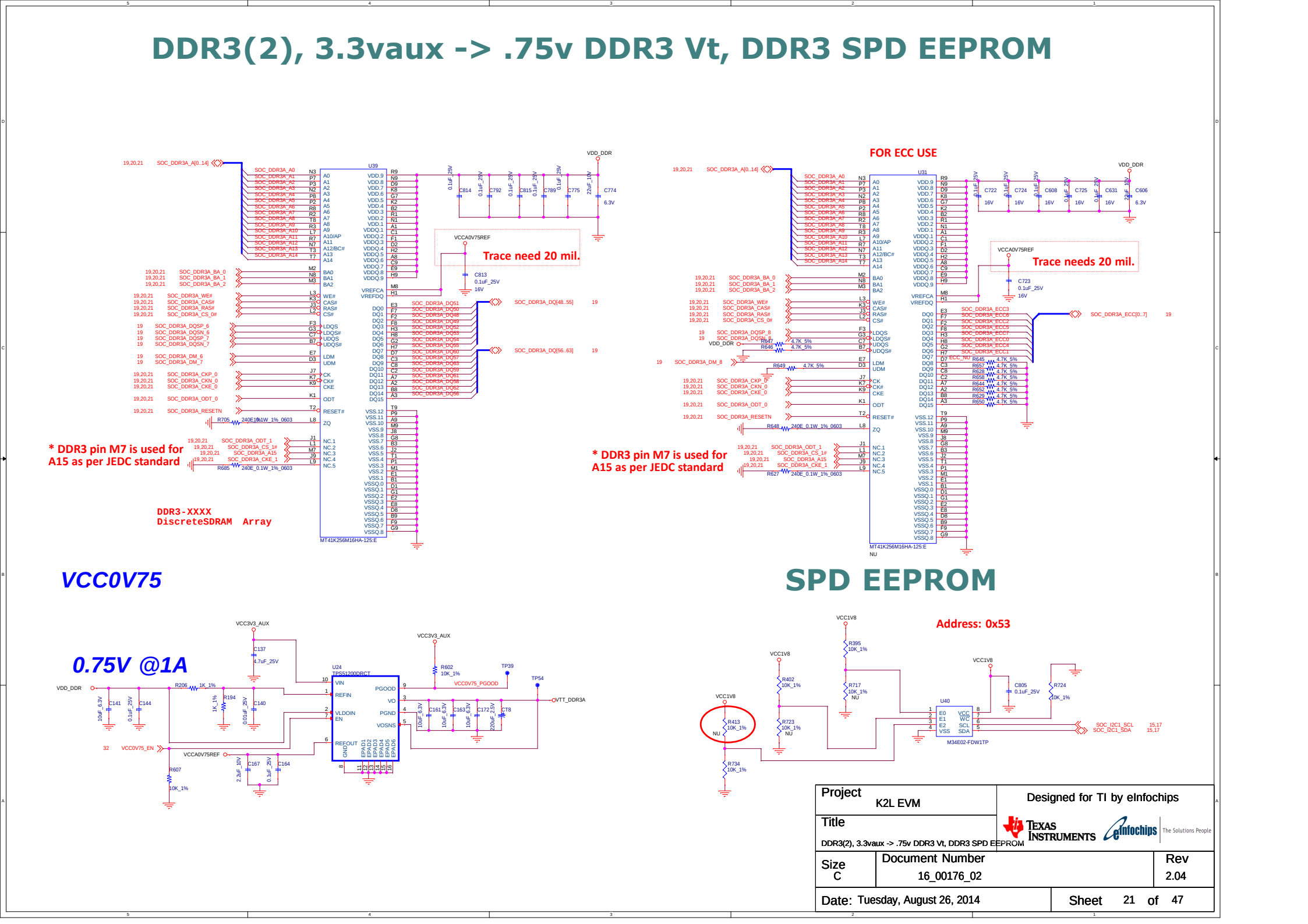
VCC0V75

0.75V @1A

SPD EEPROM

Address: 0x53

Project		Designed for TI by elfinichips	
K2L EVM			
Title		DDR3(2), 3.3vaux -> .75v DDR3 Vt, DDR3 SPD EEPROM	
Size	Document Number	Rev	
C	16_00176_02	2.04	
Date: Tuesday, August 26, 2014		Sheet 21 of 47	



DDR3(2), 3.3vaux -> .75v DDR3 Vt, DDR3 SPD EEPROM

Trace need 20 mil.

*** DDR3 pin M7 is used for A15 as per JEDC standard**

DDR3-XXXX DiscreteSDRAM Array

FOR ECC USE

Trace needs 20 mil.

*** DDR3 pin M7 is used for A15 as per JEDC standard**

VCC0V75

0.75V @1A

SPD EEPROM

Address: 0x53

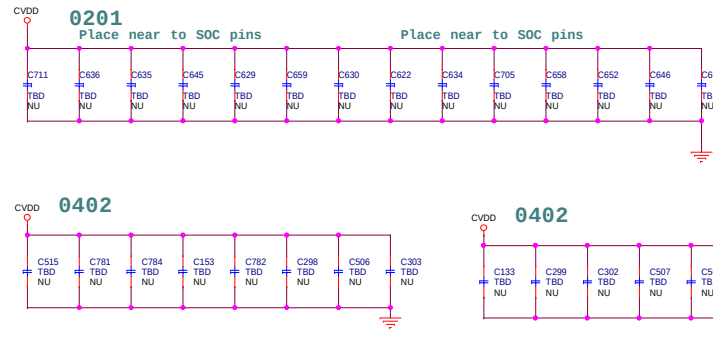
Project K2L EVM		Designed for TI by elfinichips	
Title DDR3(2), 3.3vaux -> .75v DDR3 Vt, DDR3 SPD EEPROM			
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 21 of 47	

K2L GND AND POWER

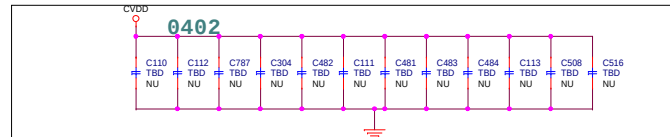
U30A		
A1	VSS_1	VSS_134
AA10	VSS_2	VSS_135
AA12	VSS_3	VSS_136
AA14	VSS_4	VSS_137
AA16	VSS_5	VSS_138
AA18	VSS_6	VSS_139
AA20	VSS_7	VSS_140
AA22	VSS_8	VSS_141
AA24	VSS_9	VSS_142
AA26	VSS_10	VSS_143
AA6	VSS_11	VSS_144
AA8	VSS_12	VSS_145
AB1	VSS_13	VSS_146
AB11	VSS_14	VSS_147
AB13	VSS_15	VSS_148
AB15	VSS_16	VSS_149
AB17	VSS_17	VSS_150
AB19	VSS_18	VSS_151
AB21	VSS_19	VSS_152
AB23	VSS_20	VSS_153
AB25	VSS_21	VSS_154
AB7	VSS_22	VSS_155
AB9	VSS_23	VSS_156
AC10	VSS_24	VSS_157
AC12	VSS_25	VSS_158
AC14	VSS_26	VSS_159
AC16	VSS_27	VSS_160
AC18	VSS_28	VSS_161
AC20	VSS_29	VSS_162
AC22	VSS_30	VSS_163
AC24	VSS_31	VSS_164
AC6	VSS_32	VSS_165
AC8	VSS_33	VSS_166
AD11	VSS_34	VSS_167
AD13	VSS_35	VSS_168
AD15	VSS_36	VSS_169
AD17	VSS_37	VSS_170
AD19	VSS_38	VSS_171
AD21	VSS_39	VSS_172
AD23	VSS_40	VSS_173
AD25	VSS_41	VSS_174
AD9	VSS_42	VSS_175
AD3	VSS_43	VSS_176
AD7	VSS_44	VSS_177
AD9	VSS_45	VSS_178
AE10	VSS_46	VSS_179
AE12	VSS_47	VSS_180
AE14	VSS_48	VSS_181
AE16	VSS_49	VSS_182
AE18	VSS_50	VSS_183
AE24	VSS_51	VSS_184
AE6	VSS_52	VSS_185
AE8	VSS_53	VSS_186
AF13	VSS_54	VSS_187
AF16	VSS_55	VSS_188
AF19	VSS_56	VSS_189
AF21	VSS_57	VSS_190
AF25	VSS_58	VSS_191
AF7	VSS_59	VSS_192
AG11	VSS_60	VSS_193
AG14	VSS_61	VSS_194
AG17	VSS_62	VSS_195
AG20	VSS_63	VSS_196
AG23	VSS_64	VSS_197
AG26	VSS_65	VSS_198
AG28	VSS_66	VSS_199
AG4	VSS_67	VSS_200
AH10	VSS_68	VSS_201
AH13	VSS_69	VSS_202
AH16	VSS_70	VSS_203
AH19	VSS_71	VSS_204
AH22	VSS_72	VSS_205
AH25	VSS_73	VSS_206
AJ11	VSS_74	VSS_207
AJ14	VSS_75	VSS_208
AJ17	VSS_76	VSS_209
AJ20	VSS_77	VSS_210
AJ23	VSS_78	VSS_211
AJ26	VSS_79	VSS_212
AJ8	VSS_80	VSS_213
AK1	VSS_81	VSS_214
AK12	VSS_82	VSS_215
AK15	VSS_83	VSS_216
AK18	VSS_84	VSS_217
AK21	VSS_85	VSS_218
AK24	VSS_86	VSS_219
AK27	VSS_87	VSS_220
AK30	VSS_88	VSS_221
C13	VSS_89	VSS_222
C18	VSS_90	VSS_223
C22	VSS_91	VSS_224
C26	VSS_92	VSS_225
C5	VSS_93	VSS_226
C9	VSS_94	VSS_227
D11	VSS_95	VSS_228
D16	VSS_96	VSS_229
D20	VSS_97	VSS_230
D24	VSS_98	VSS_231
D28	VSS_99	VSS_232
D3	VSS_100	VSS_233
D7	VSS_101	VSS_234
F16	VSS_102	VSS_235
F4	VSS_103	VSS_236
G1	VSS_104	VSS_237
G10	VSS_105	VSS_238
G12	VSS_106	VSS_239
G14	VSS_107	VSS_240
G16	VSS_108	VSS_241
G18	VSS_109	VSS_242
G20	VSS_110	VSS_243
G22	VSS_111	VSS_244
G24	VSS_112	VSS_245
G3	VSS_113	VSS_246
G5	VSS_114	VSS_247
G6	VSS_115	VSS_248
G8	VSS_116	VSS_249
H11	VSS_117	VSS_250
H13	VSS_118	VSS_251
H15	VSS_119	VSS_252
H17	VSS_120	VSS_253
H19	VSS_121	VSS_254
H2	VSS_122	VSS_255
H21	VSS_123	VSS_256
H23	VSS_124	VSS_257
H4	VSS_125	VSS_258
H5	VSS_126	VSS_259
H7	VSS_127	VSS_260
H9	VSS_128	VSS_261
J10	VSS_129	VSS_262
J12	VSS_130	VSS_263
J16	VSS_131	VSS_264
J18	VSS_132	VSS_265
J19	VSS_133	VSS_266

LAMARR_PROCESSOR_0

THESE CAPS ARE ADDED FOR PROVISION ONLY. VALUES CAN BE CHANGED BASED ON PI ANALYSIS RESULT



THESE CAPS ARE ADDED TO SUPPORT PER PIN DECAP. BASED ON PI ANALYSIS RESULT, IT WILL BE CHANGED (# OF CAPACITORS, VALUES, ETC)



NEWLY ADDED DECAPS FOR PI (12NOS ADDED)

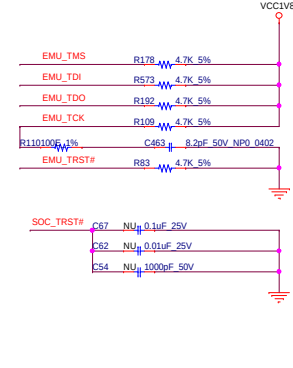
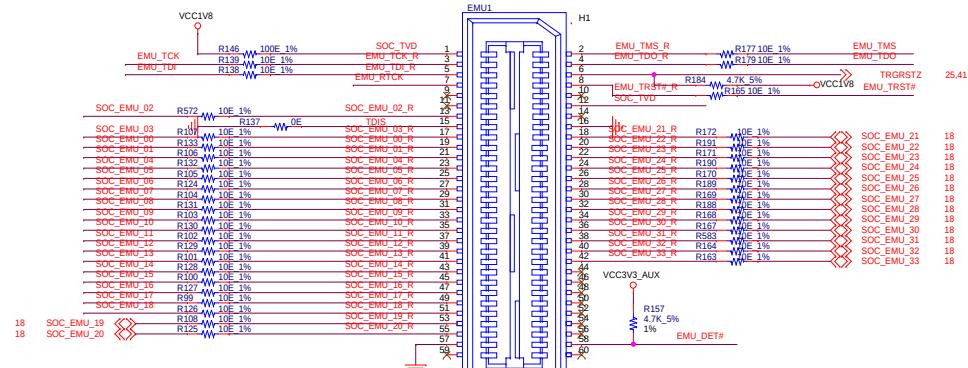
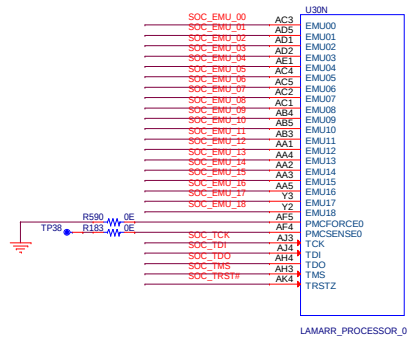
Project K2L EVM		Designed for TI by elfinfochips	
Title K2L GND AND POWER		  The Solutions People	
Size C	Document Number 16_00176_02		Rev 2.04
Date: Tuesday, August 26, 2014		Sheet 22 of 47	

Project K2L EVM		Designed for TI by eInfochips	
Title K2L USB3, TPS USB 5v isolation, USB Type A connector,		 The Solutions People	
Size C	Document Number 16_00176_02	magnetics, filter, SOC UART 1.8/3.3v, USB to dual UART	
Date: Thursday, September 25, 2014		Sheet 23 of 47	

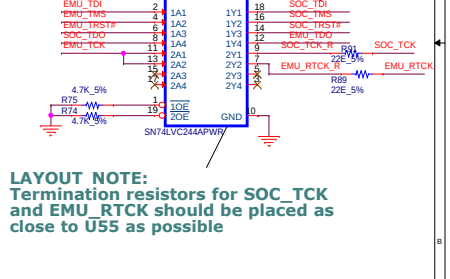
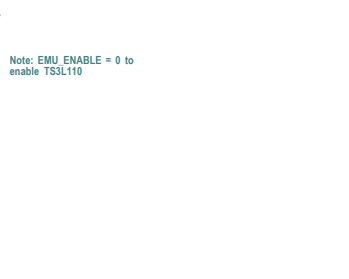
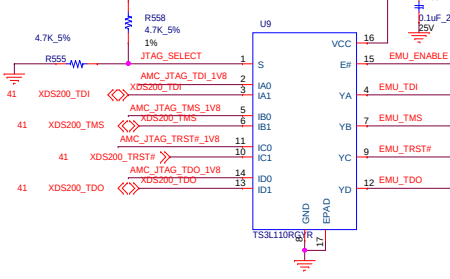
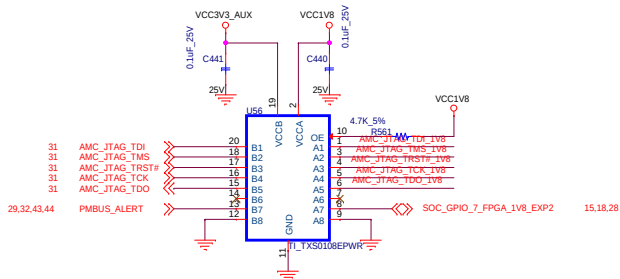
K2L EMU, K2L JTAG, EMU MIPI 60, EMU Detect, AMC/XDS200 JTAG sw, AMC JTAG 3.3 to 1.8v, SOC miniUSB, SOC 4pin hdr

EMU MIPI60

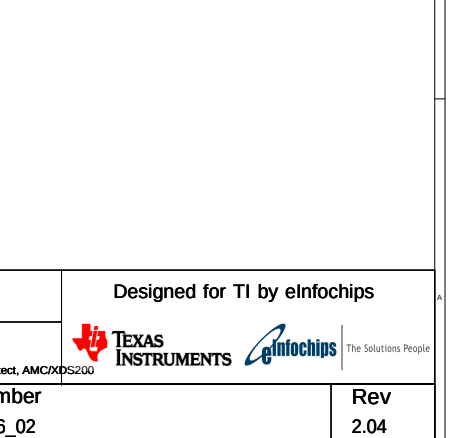
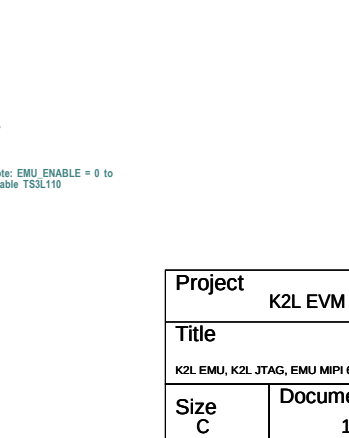
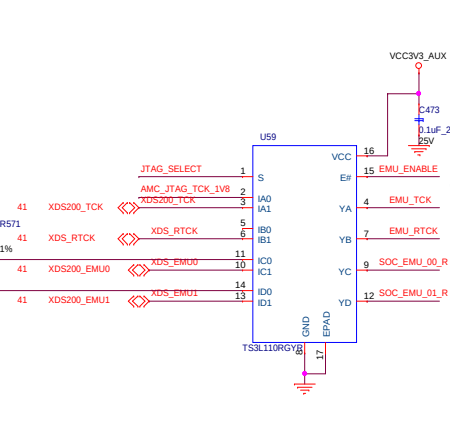
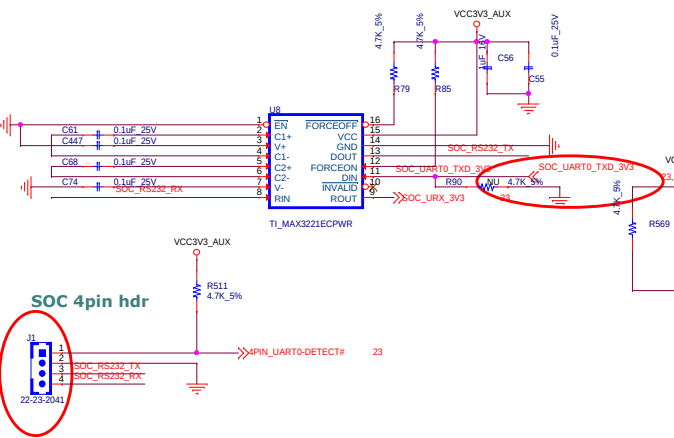
K2L EMU



AMC JTAG 3V3 to 1V8 CONVERTER

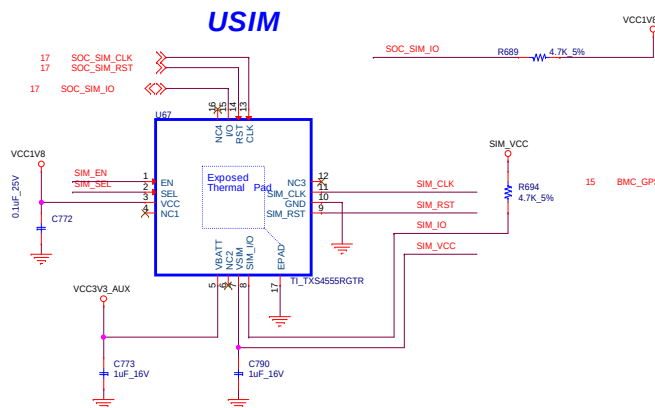


LAYOUT NOTE:
Termination resistors for SOC_TCK and EMU_RTCK should be placed as close to U55 as possible

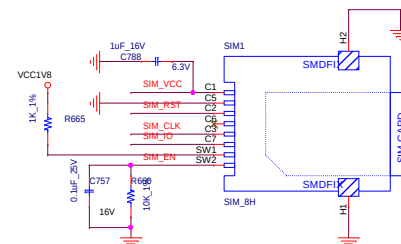
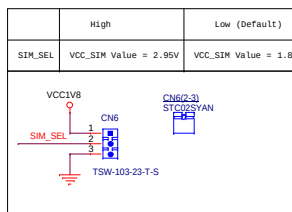
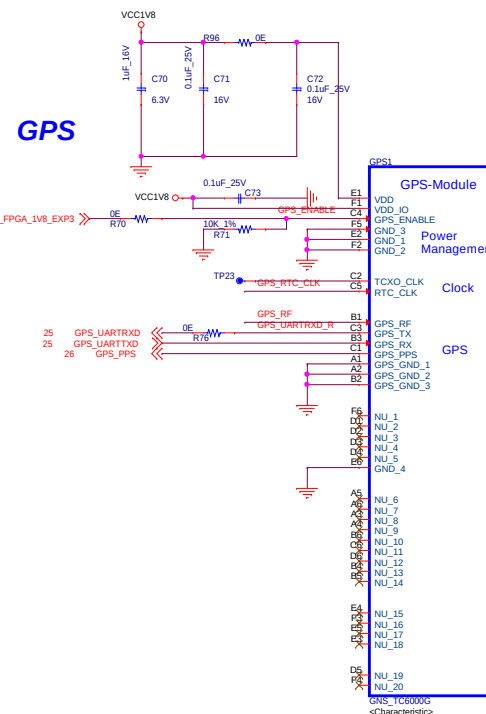


Project		K2L EVM	
Title		Designed for TI by einfochips	
Size		Document Number	
C		16_00176_02	
Date: Tuesday, August 26, 2014		Rev	
		2.04	
Sheet		24 of 47	

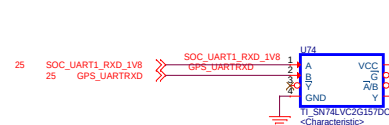
USIM, SOC UART 1.8v switching, 1.8v/3.3v GPIO INT, SOC UART, GPS



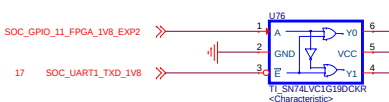
GPS



SOC UART 1.8v switching

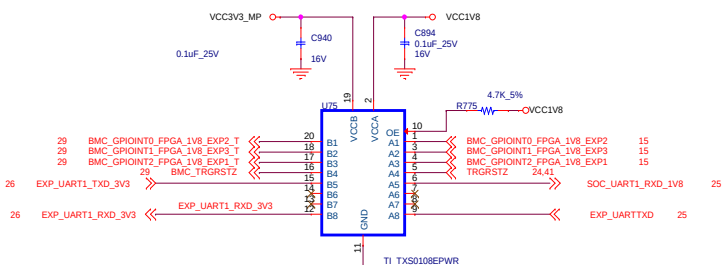


Note:GPIO8
0, SOC_UART0_Rxd -> UART1_Rxd
1, GPS_UARTRxd -> UART1_Rxd

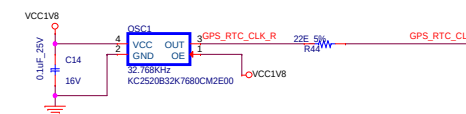
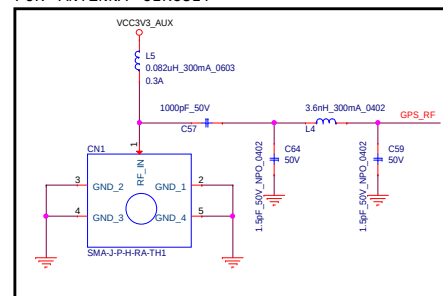


Note:GPIO11
0, SOC_UART1 -> EXP_UARTTX0
1, SOC_UART1 -> GPS_UARTTX0

SPI level shift 3.3V <=> 1.8V



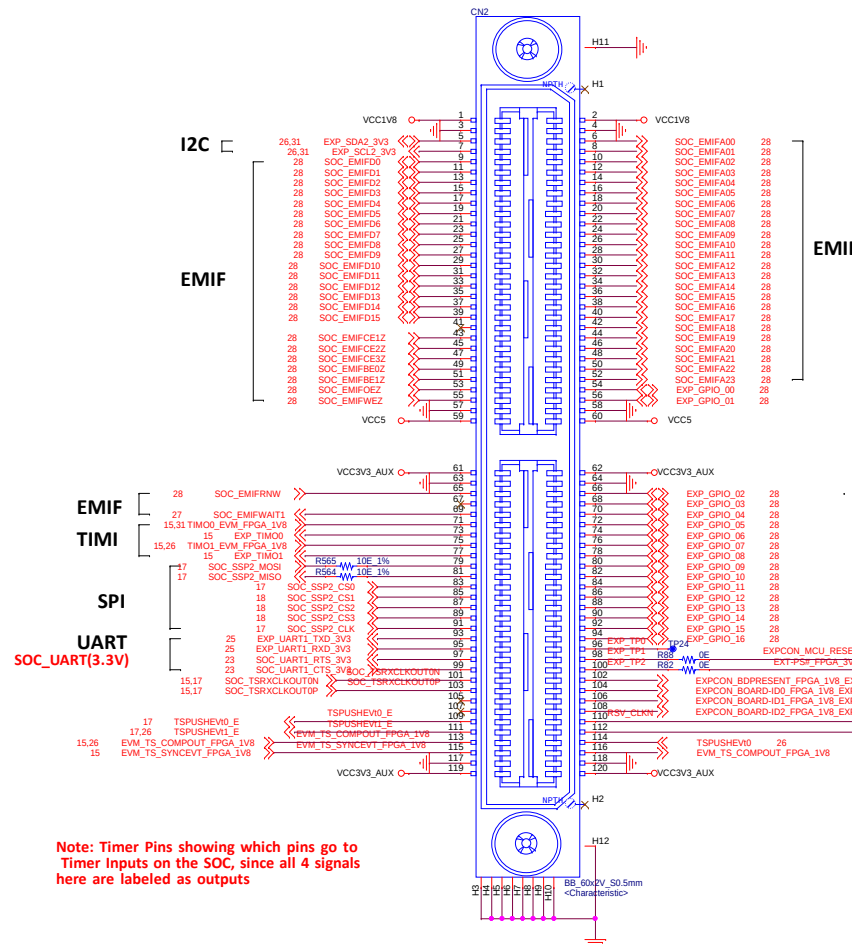
FOR ANTENNA CIRCUIT



Project K2L EVM		Designed for TI by elfinochips	
Title USIM, SOC UART 1.8v switching, 1.8v/3.3v GPIO INT, SOC UART, GPS		TEXAS INSTRUMENTS  The Solutions People	
Size C	Document Number 16_00176_02		Rev 2.04
Date: Tuesday, August 26, 2014		Sheet 25 of 47	

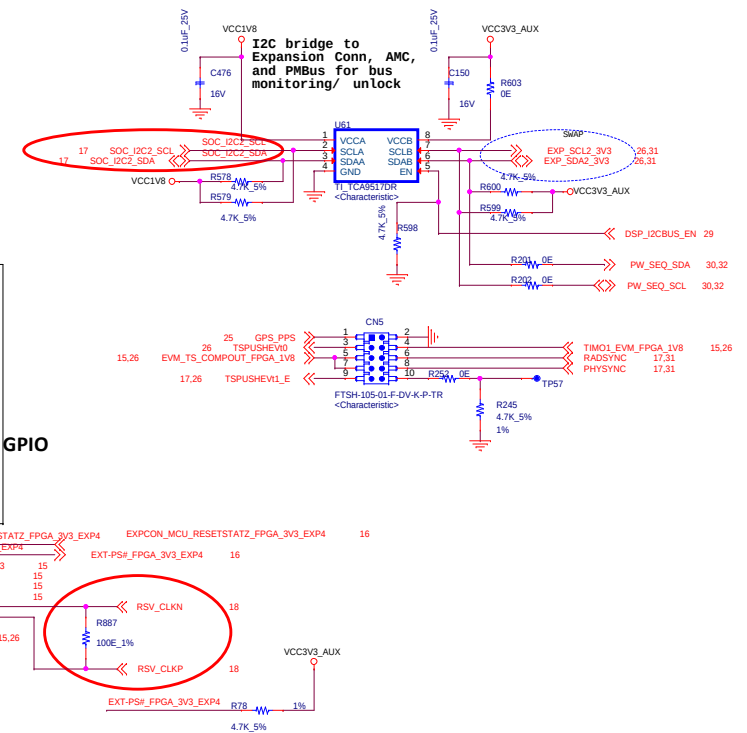
Expansion Connector, I2C SOC to Expander 1.8v/3.3vAux

Expansion Connector



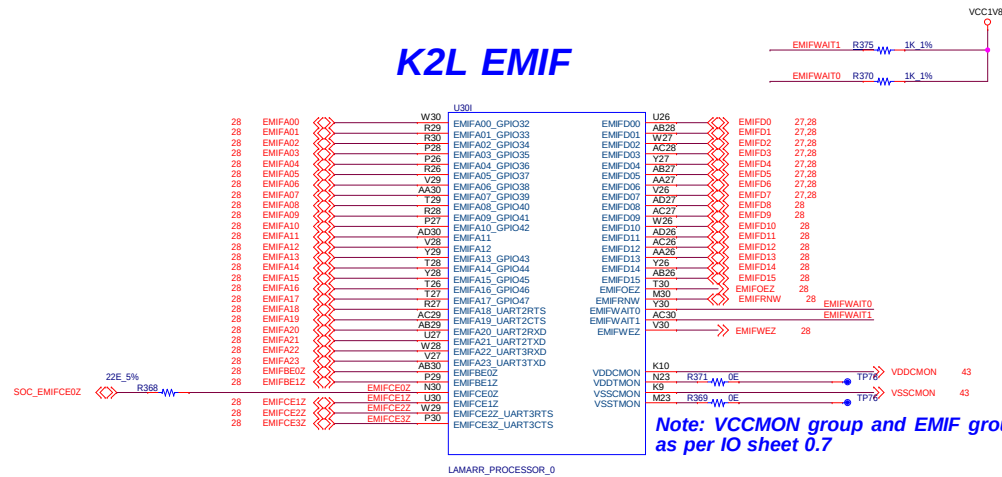
Note: Timer Pins showing which pins go to Timer Inputs on the SOC, since all 4 signals here are labeled as outputs

I2C SOC to Expander 1.8v/3.3vAux



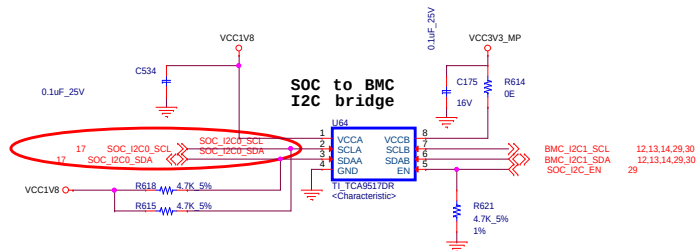
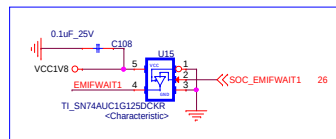
Project K2L EVM		Designed for TI by elfinichips	
Title Expansion Connector, I2C SOC to Expander 1.8v/3.3vAux			
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 26 of 47	

K2L EMIF

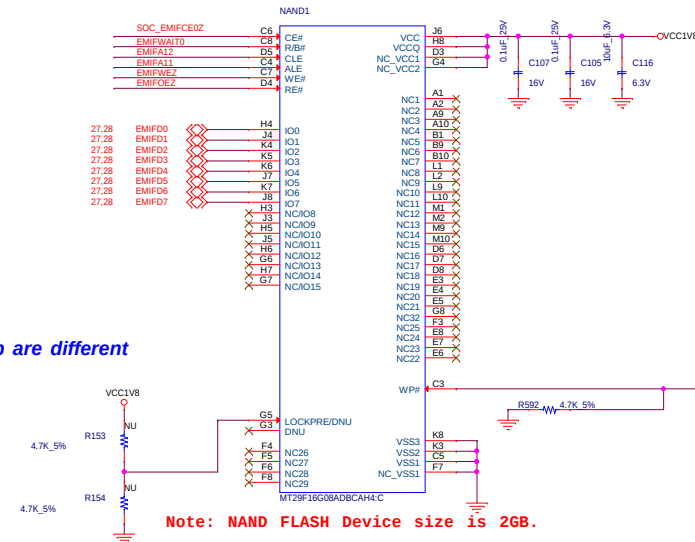


Note: VCCMON group and EMIF group are different as per IO sheet 0.7

EMIFWAIT1 bfr

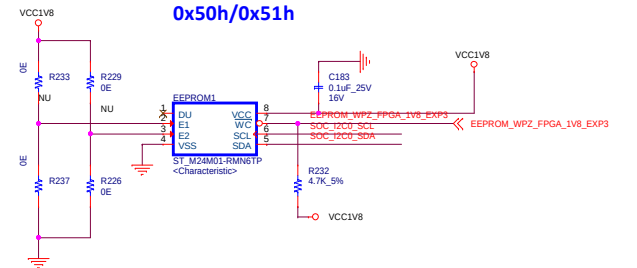


NAND FLASH



Note: NAND FLASH Device size is 2GB.

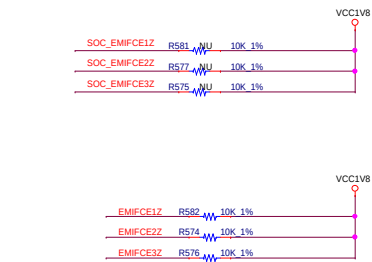
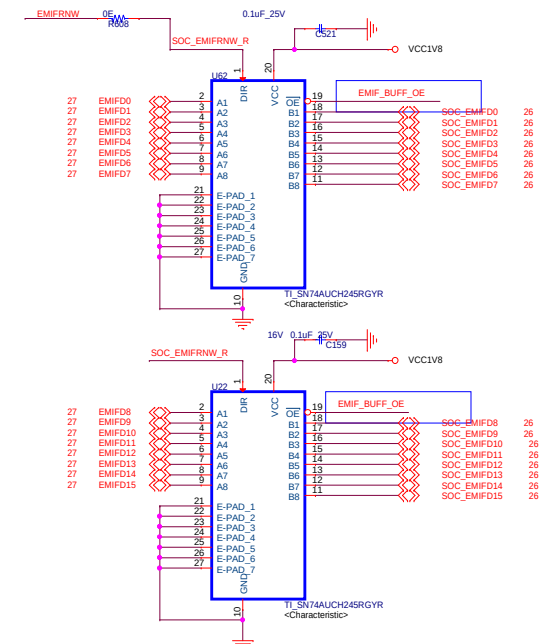
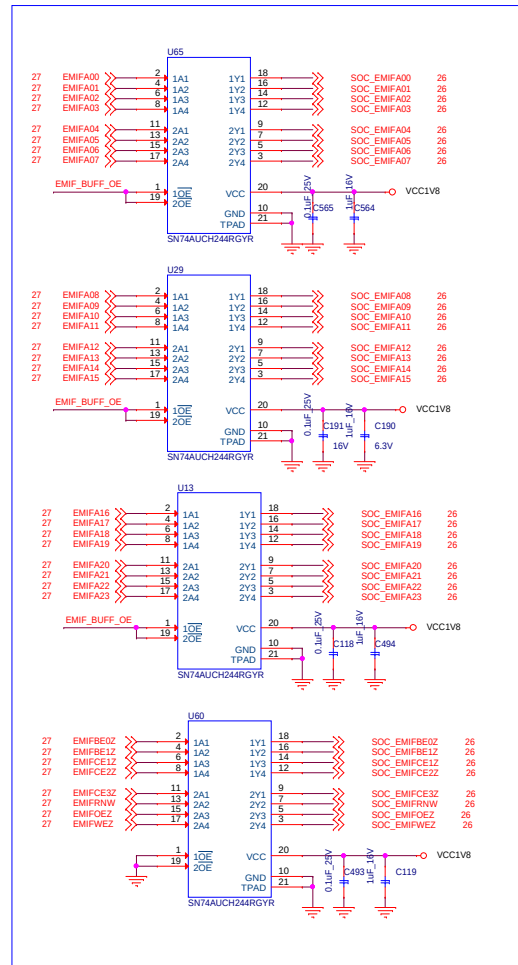
1M-bit I2C EEPROM
0x50h/0x51h



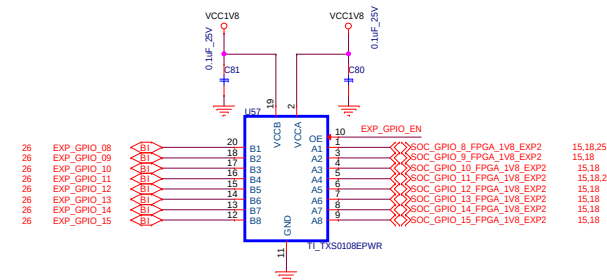
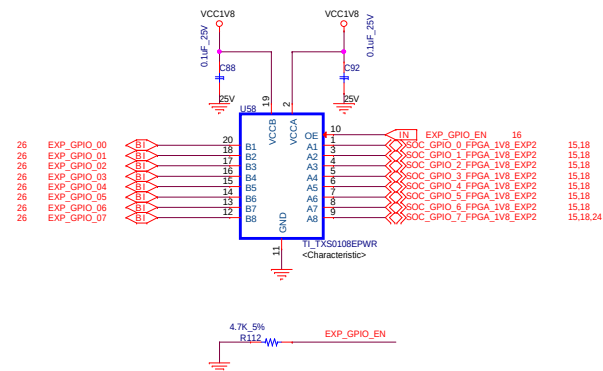
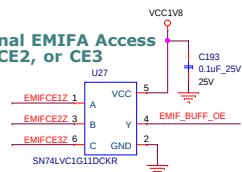
Project K2L EVM		Designed for T1 by einfochips	
Title K2L EMIF, VDD and VSSMON, EMIFWAIT1 bfr, NAND Flash, I2C EEPROM			
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 27 of 47	

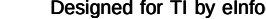
EMIF Addr/Cntl Buffer, Ext EMIF_OE, EMIF Data Transceiver

EMIF Addr/Cntl Buffer

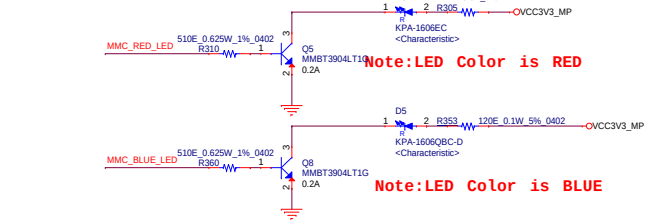
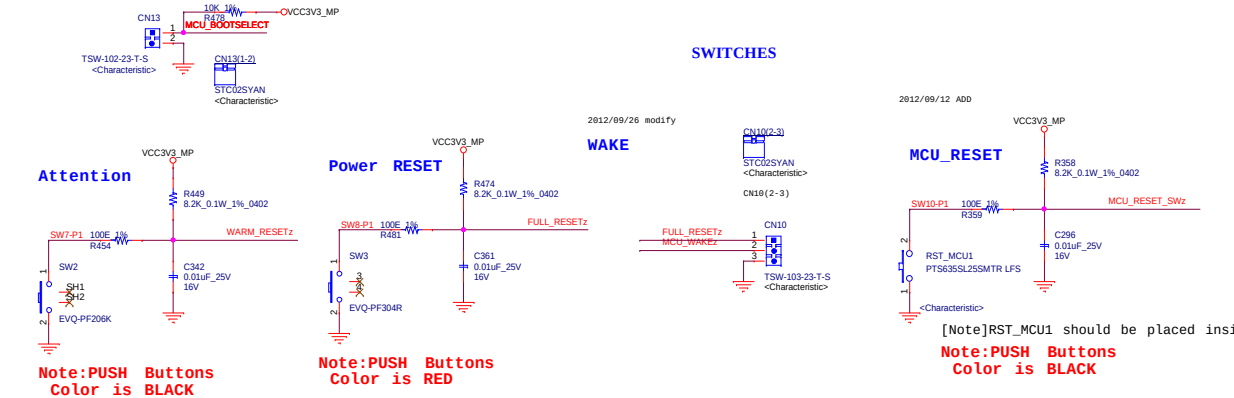
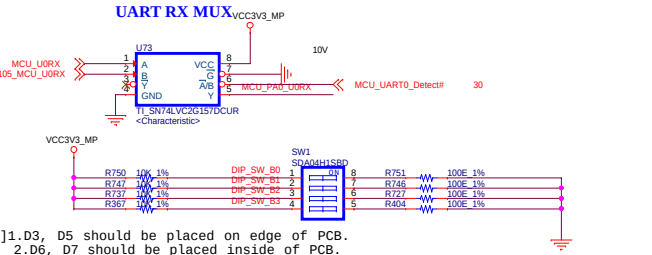
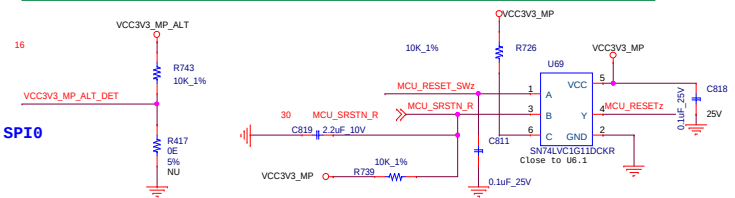
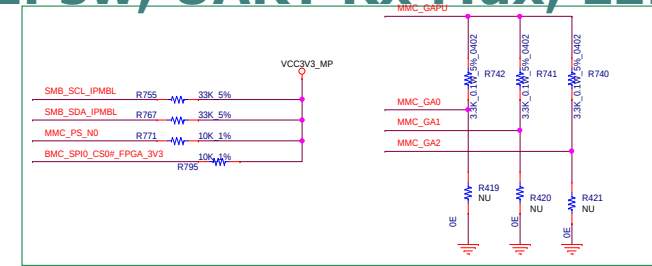
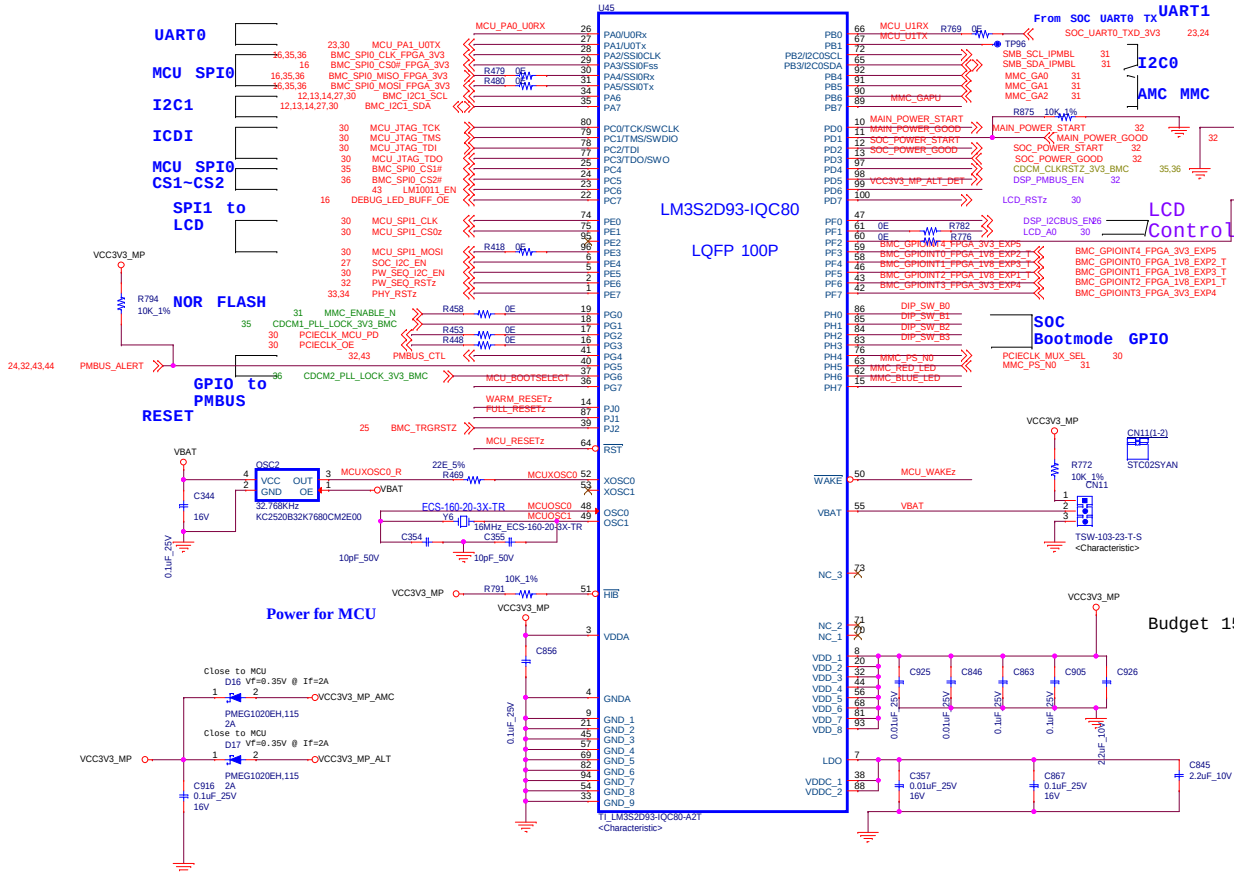


External EMIFA Access CE1, CE2, or CE3



Project K2L EVM		Designed for TI by elfinfochips	
Title EMIF Addr/Cnt/Buff, Ext EMIF_OE, EMIF Data Transceiver			
Size C	Document Number 16_00176_02		Rev 2.04
Date: Tuesday, August 26, 2014		Sheet 28 of 47	

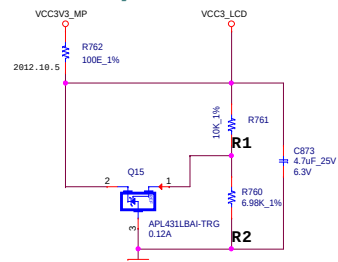
BMC Processor (LM3S2D93), switches, DIPsw, UART Rx Mux, LEDs



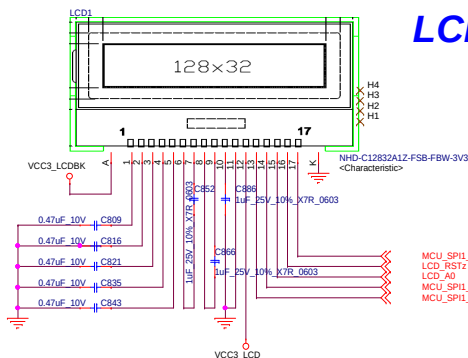
Project K2L EVM		Designed for TI by elfinfochips	
Title BMC Processor (LM3S2D93), switches, DIPsw, UART Rx Mux, LEDs		TEXAS INSTRUMENTS elfinfochips The Solutions People	
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 29 of 47	

NHD-C12832A1Z-FSB-FBW-3V3

LCD

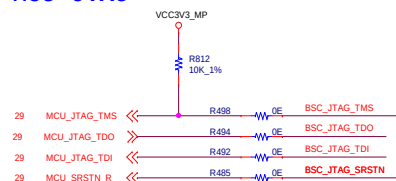
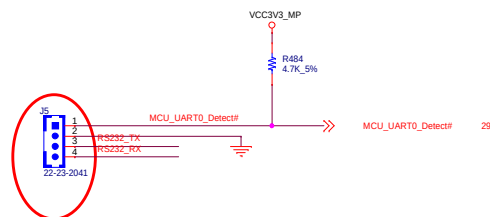
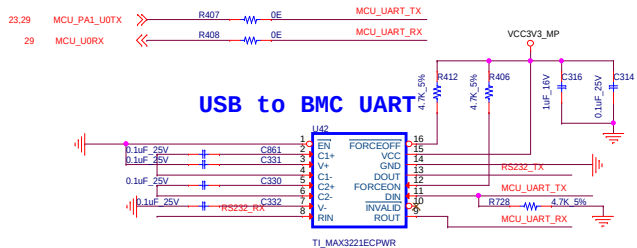


$$3.018V = 1.24 (1 + 10k/6.98k) + 0.15u \cdot 10k$$

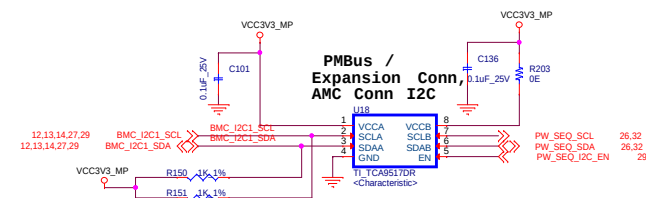
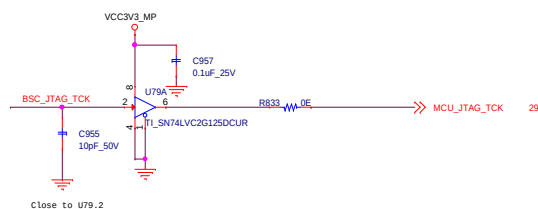


SPI1 CS0
LCD control

PCIe CLOCK MUX

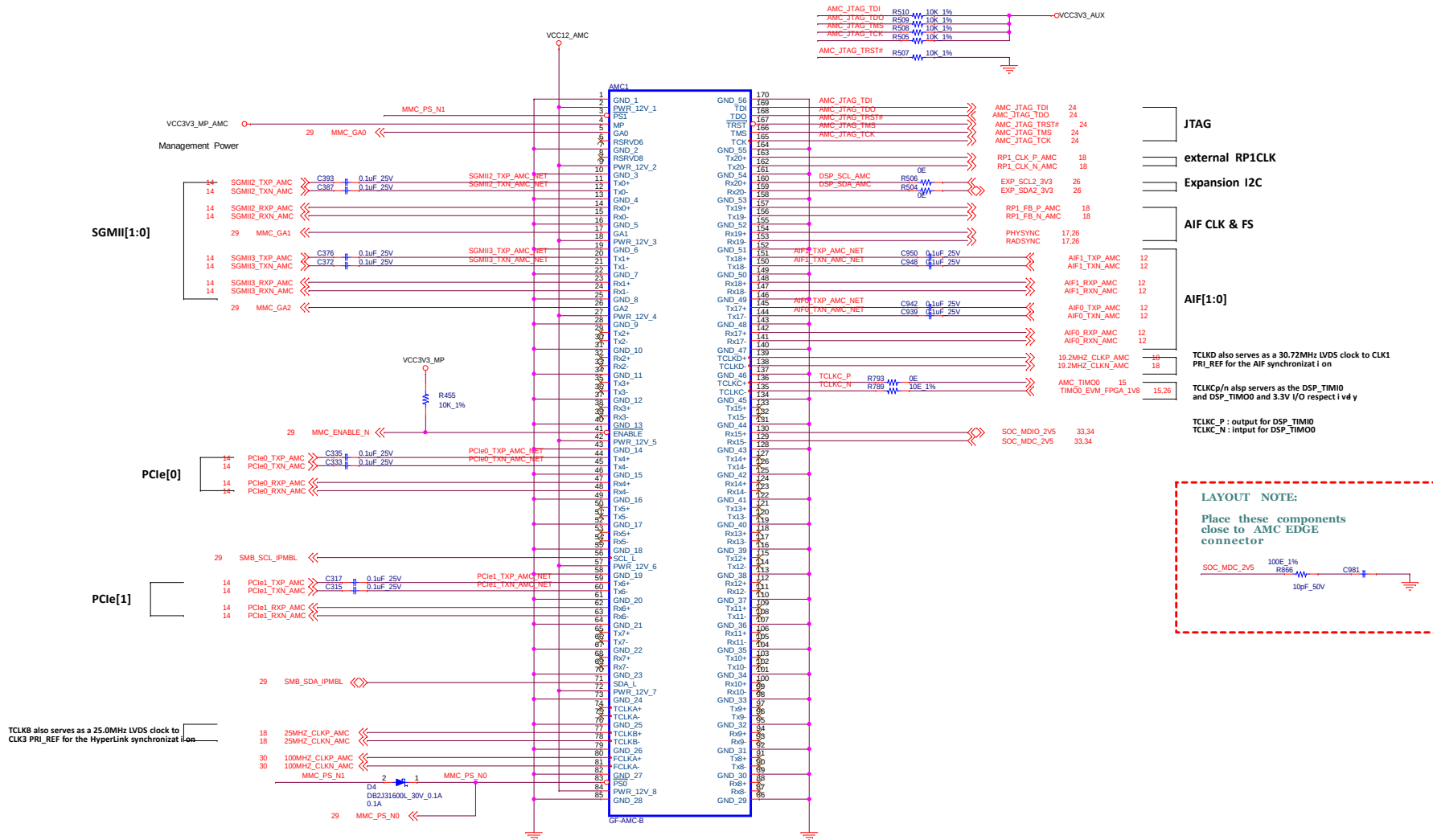


10 pos (50 mil pitch) connector



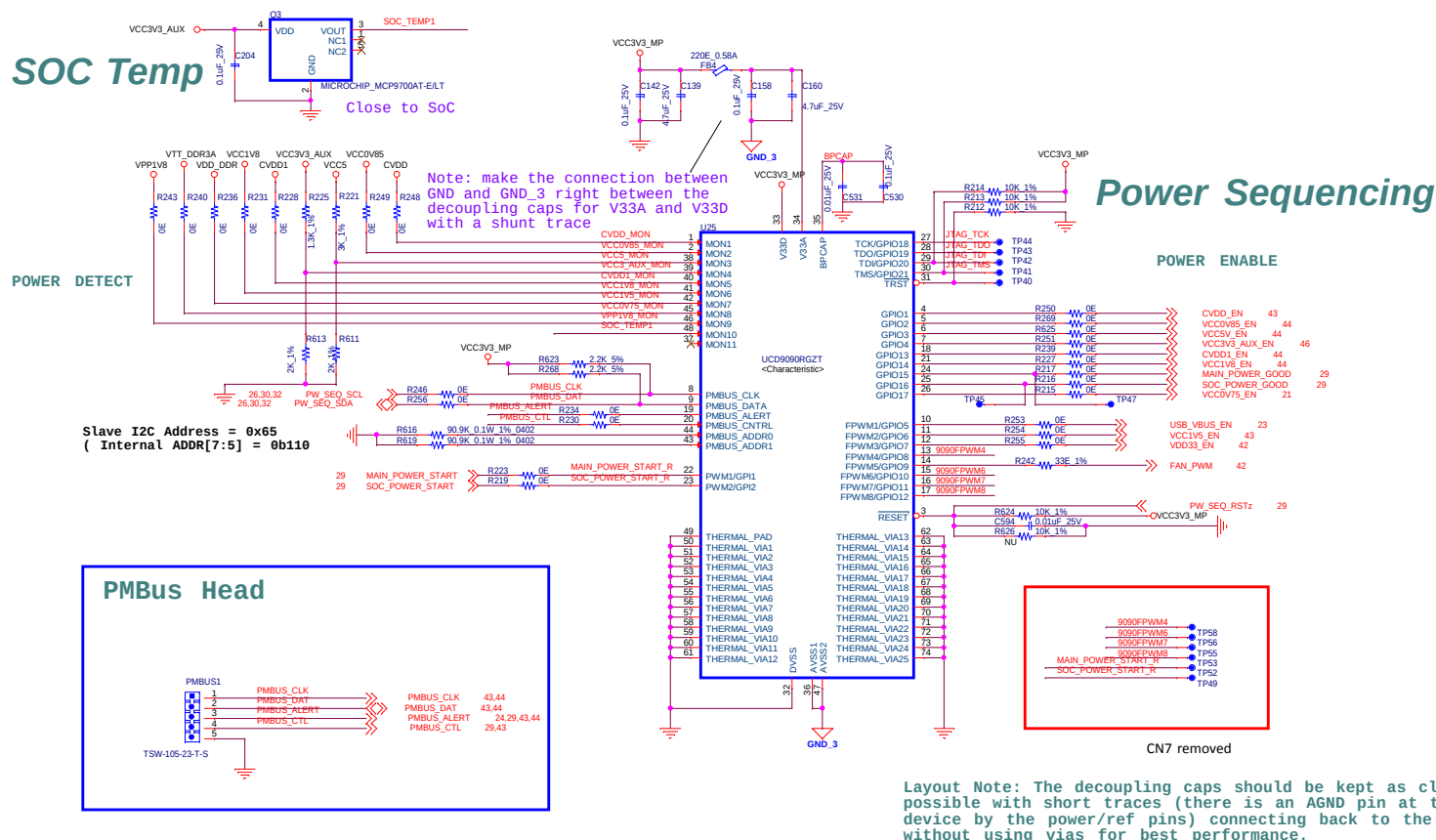
Project K2L EVM		Designed for TI by elnfochips	
Title LCD, LCD Power, BMC USB for UART, 4pin UART for BMC, BMC		  The Solutions People	
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 30 of 47	

AMC connector



Project		Designed for TI by elfinfochips	
K2L EVM		TEXAS INSTRUMENTS elfinfochips The Solutions People	
Title		AMC connector	
Size		Document Number	
C		16_00176_02	
Date: Tuesday, August 26, 2014		Sheet 31 of 47	
Rev		2.04	

SOC Temp, UCD9090, PMBus Pgm conn, VID Isolator for PMBus



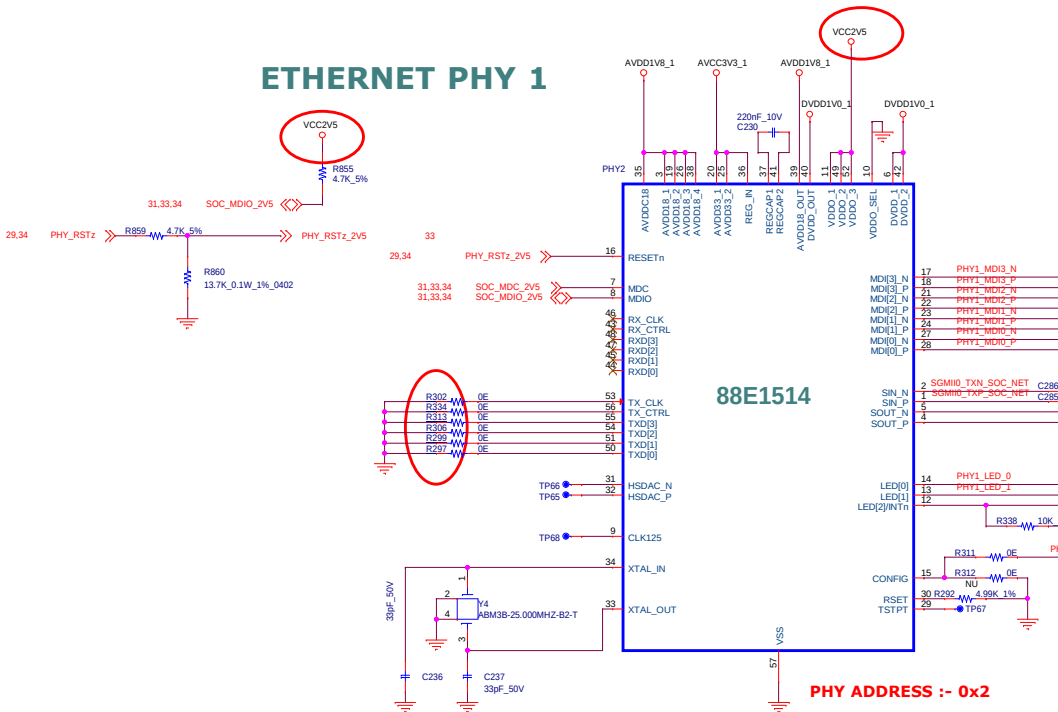
PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
SHORT	--

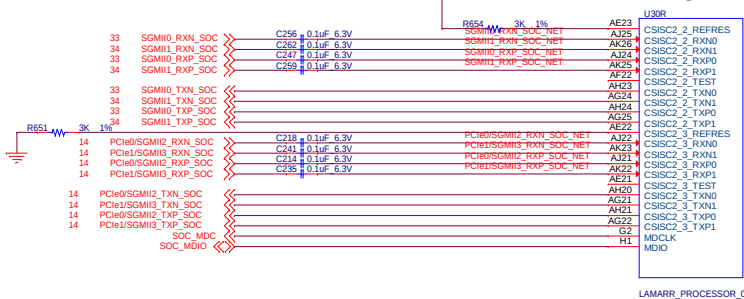
Project K2L EVM		Designed for TI by elnfochips	
Title SOC Temp, UCD9090, PMBus Pgm conn, VID Isolator for PMBus		 TEXAS INSTRUMENTS  The Solutions People	
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 32 of 47	

Ethernet PHY, Magnetics for 2 channel/ Tx/Rx, MDC/MDIO for AMC, K2L SGMII/ PCIe

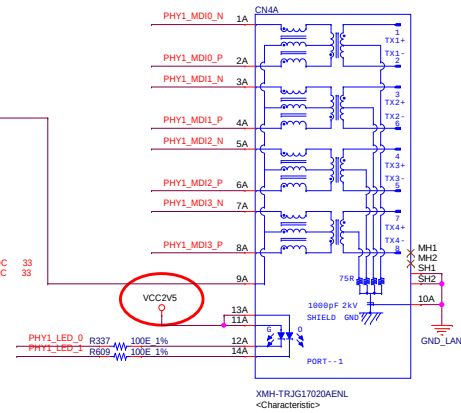
ETHERNET PHY 1



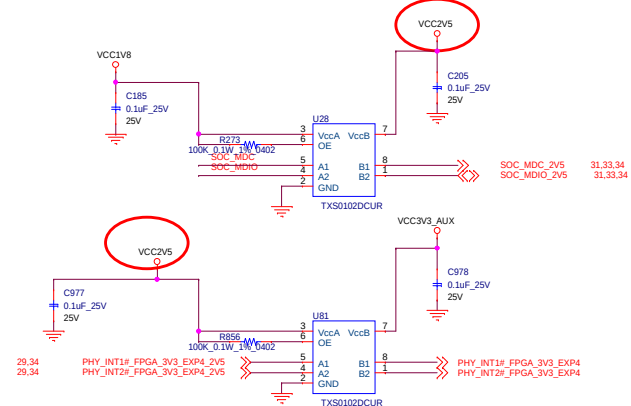
K2L SGMII/ PCIe



Magnetics for 2 channel/ Tx/Rx

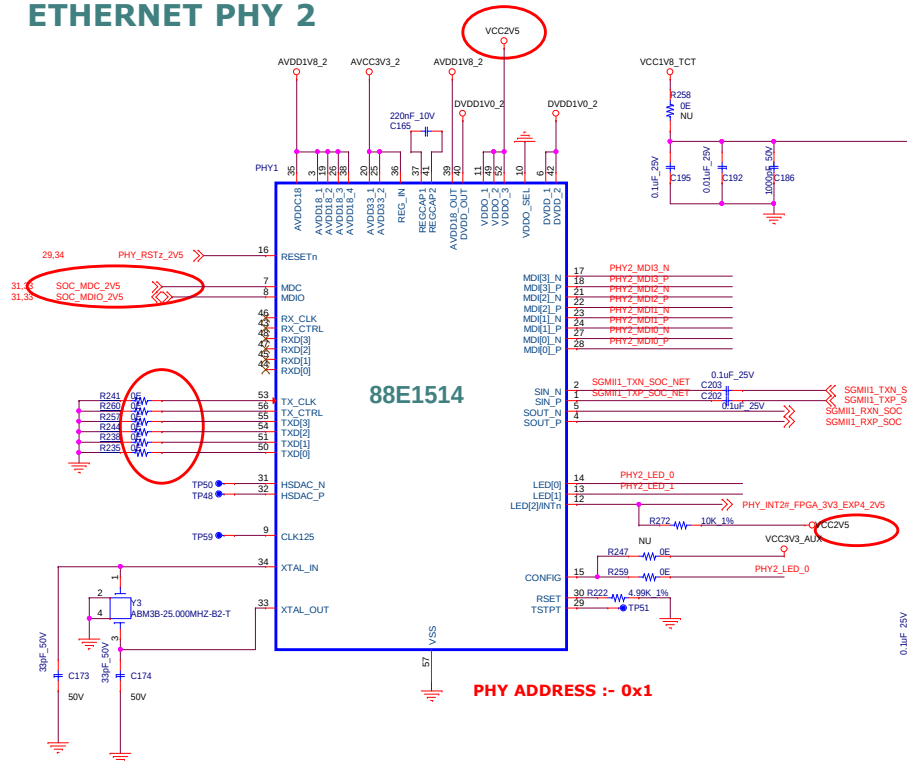


MDC/MDIO for AMC

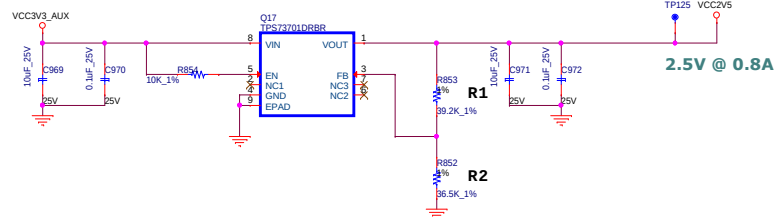


Project K2L EVM		Designed for TI by elfin chips	
Title Ethernet PHY, Magnetics for 2 channel/ Tx/Rx,		TEXAS INSTRUMENTS elfin chips The Solutions People	
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 33 of 47	

ETHERNET PHY 2

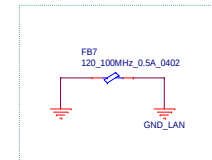
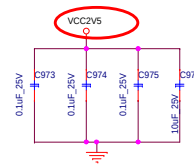
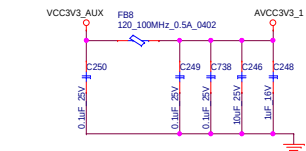
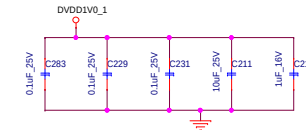
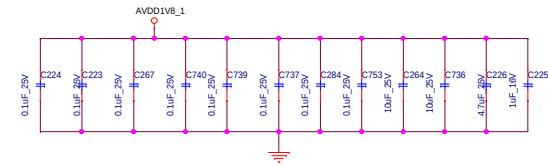
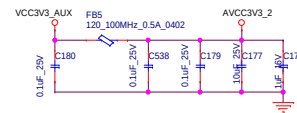
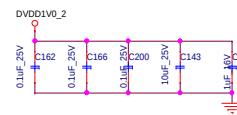
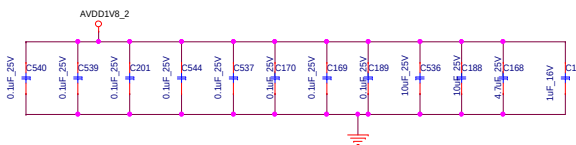
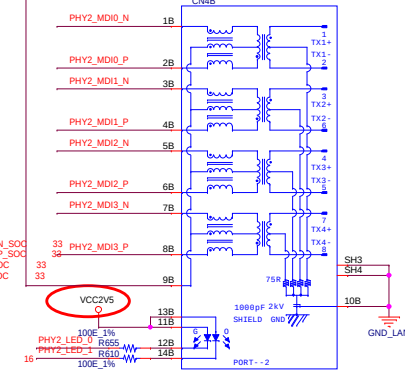


PHY ADDRESS :- 0x1



$$\begin{aligned} V_{out} &= (R_1 + R_2) \cdot V_{FB} / R_2 \\ &= (39.2 + 36.5k) \cdot 1.2 / 36.5k \\ &= 2.5V \end{aligned}$$

Magnetics for 2 channel/ Tx/Rx



Project K2L EVM		Designed for TI by elfinfochips	
Title Ethernet PHY, Magnetics for 2 channel/ Tx/Rx			
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 34 of 47	

CDCM62008 Clk2, 100 / 156.25, Power Filter for Clock

STATUS0 outputs the PLL_LOCK signal
STATUS1 the LOSS OF REFERENCE.

[Note] layout would place R757 and C327 close to U43.

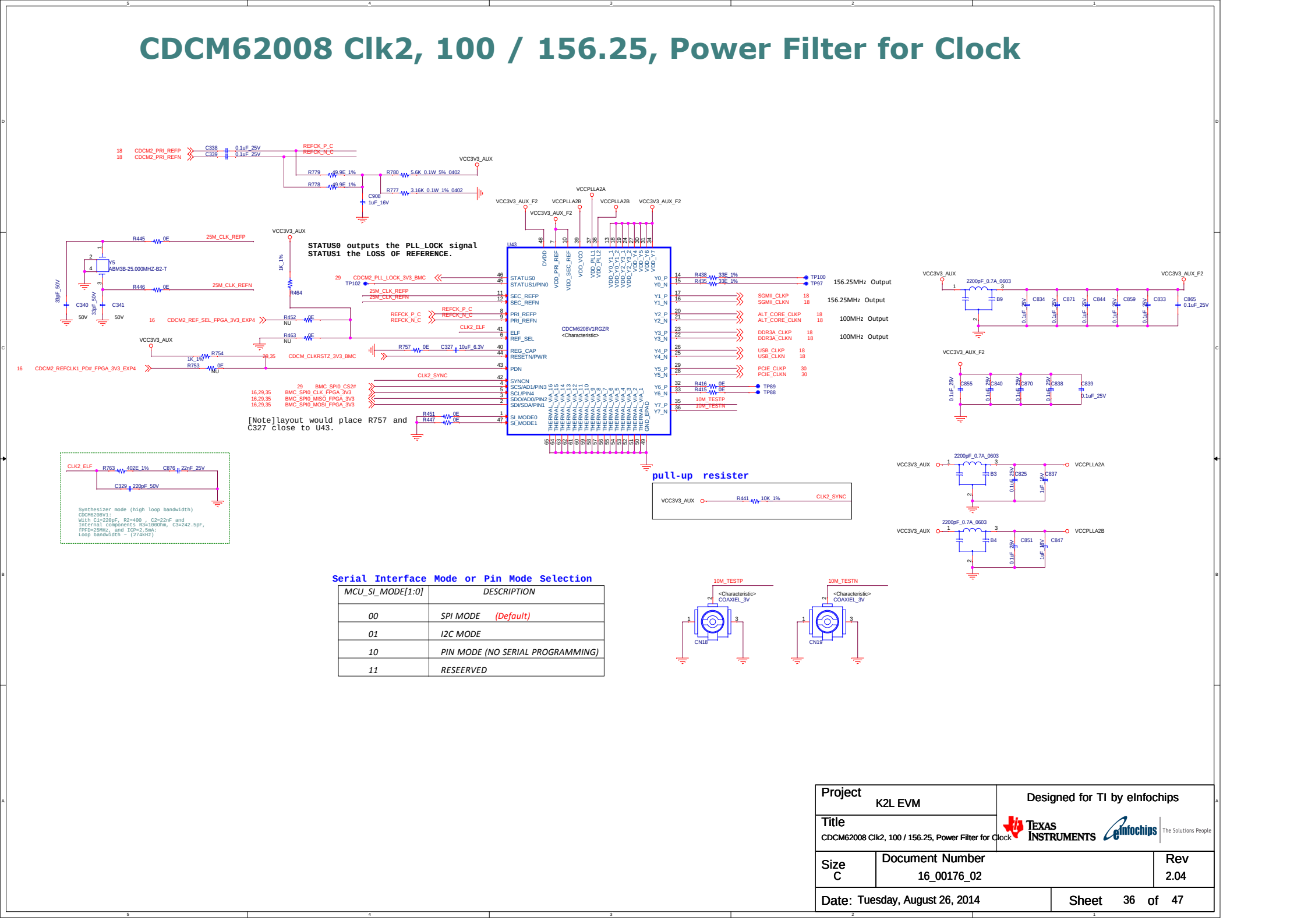
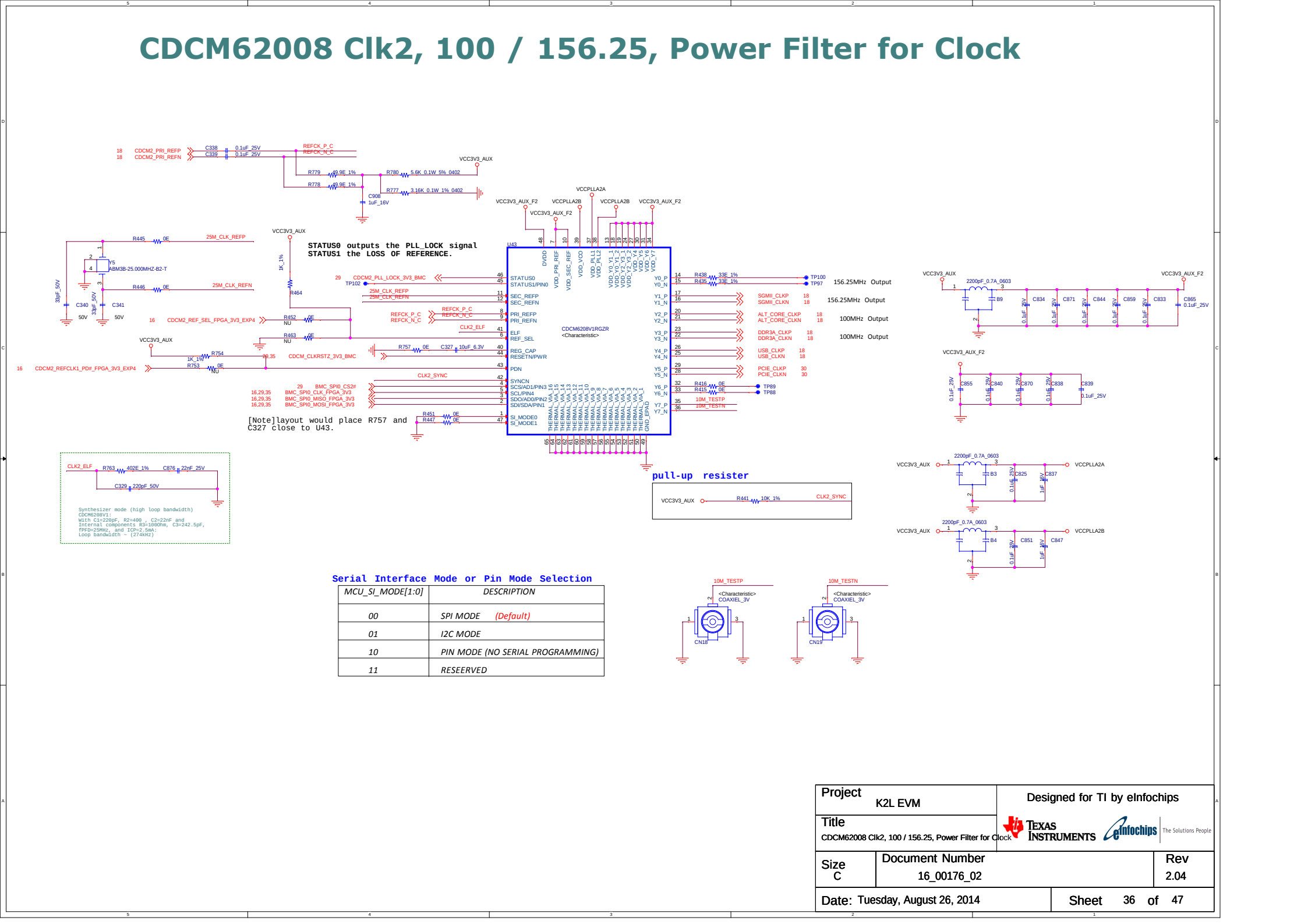
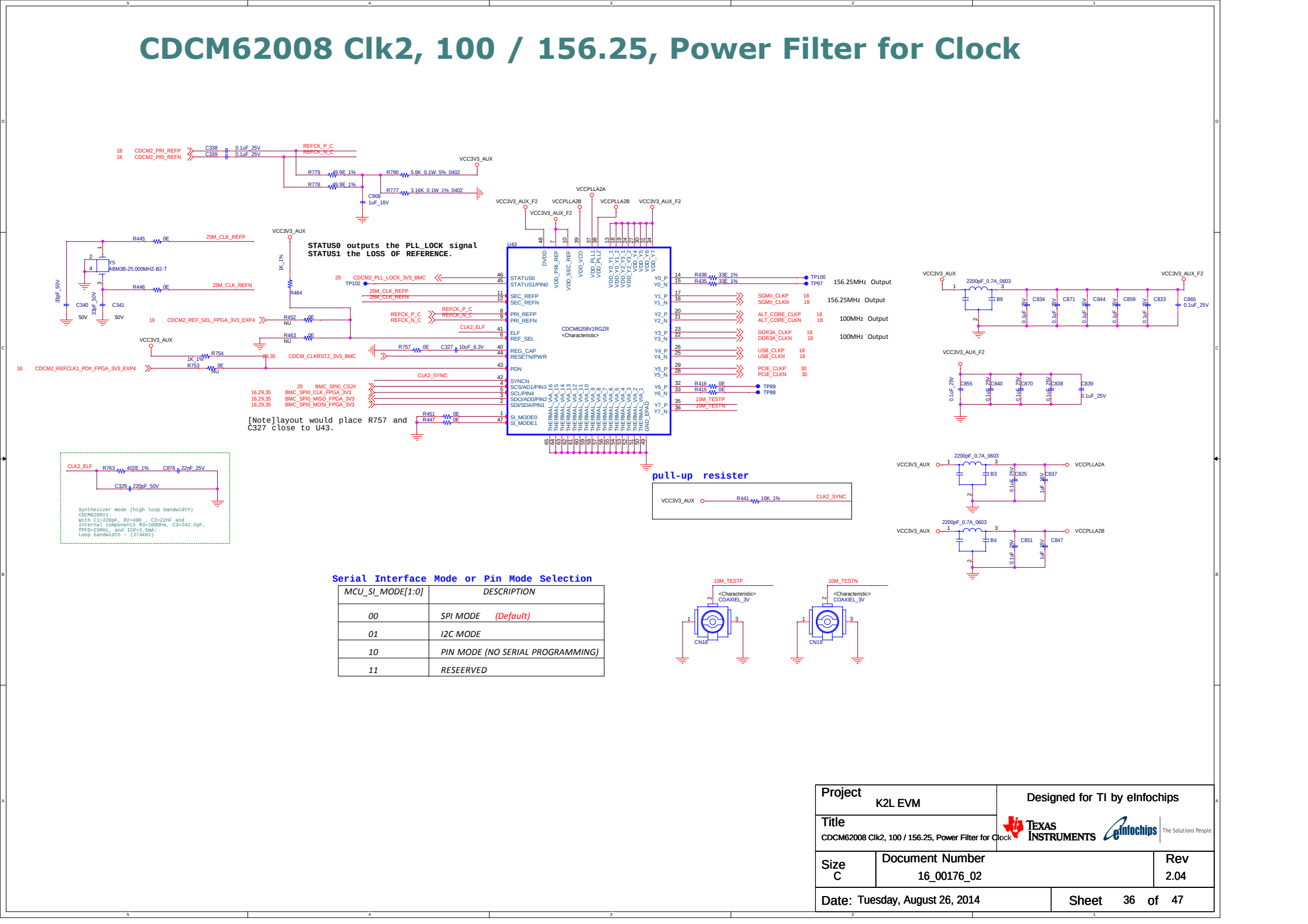
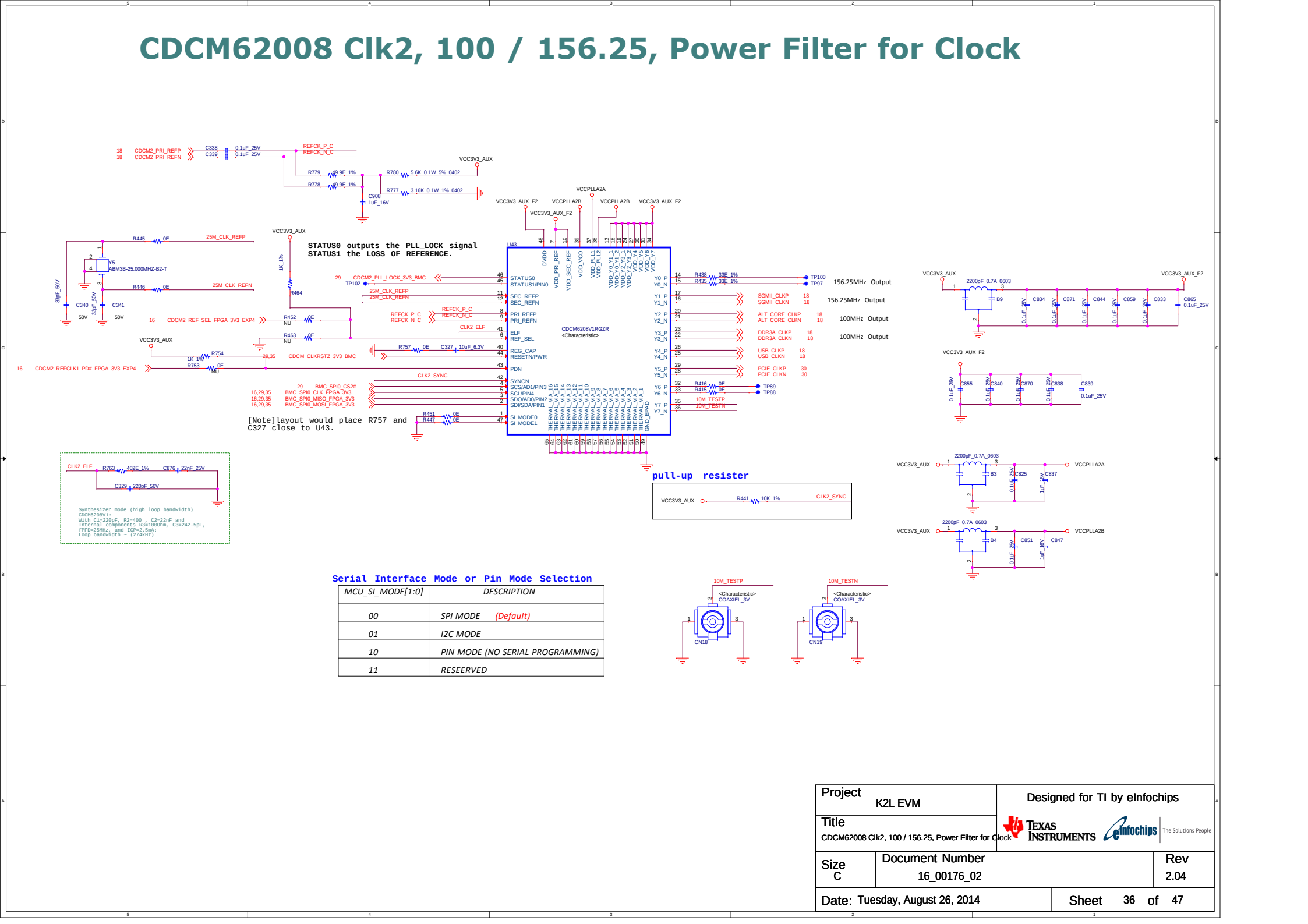
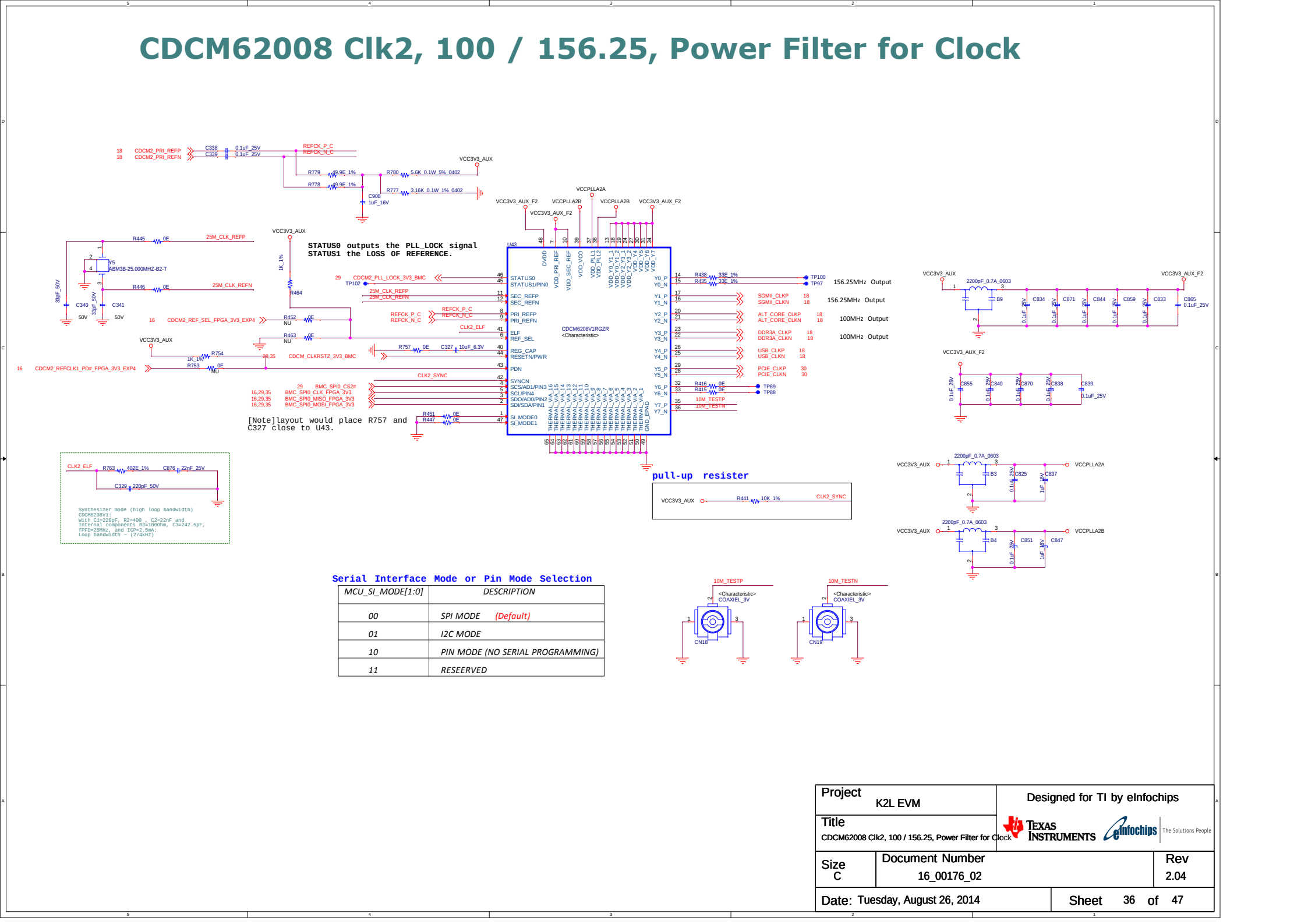
pull-up resistor

Serial Interface Mode or Pin Mode Selection

MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEVED

Project: K2L EVM
Title: CDCM62008 Clk2, 100 / 156.25, Power Filter for Clock
Size C
Document Number: 16_00176_02
Date: Tuesday, August 26, 2014

Designed for TI by elnfochips
TEXAS INSTRUMENTS
elinfochips The Solutions People
Rev: 2.04
Sheet 36 of 47



CDCM62008 Clk2, 100 / 156.25, Power Filter for Clock

STATUS0 outputs the PLL_LOCK signal
STATUS1 the LOSS OF REFERENCE.

[Note] layout would place R757 and C327 close to U43.

pull-up resistor

Serial Interface Mode or Pin Mode Selection

MCU_SI_MODE[1:0]	DESCRIPTION
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11	RESEVERVED

Project: K2L EVM
Title: CDCM62008 Clk2, 100 / 156.25, Power Filter for Clock
Size C
Document Number: 16_00176_02
Date: Tuesday, August 26, 2014

Designed for TI by elnfochips
TEXAS INSTRUMENTS
elinfochips The Solutions People
Rev: 2.04
Sheet 36 of 47

CDCM62008 Clk2, 100 / 156.25, Power Filter for Clock

STATUS0 outputs the PLL_LOCK signal
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[Note] layout would place R757 and C327 close to U43.

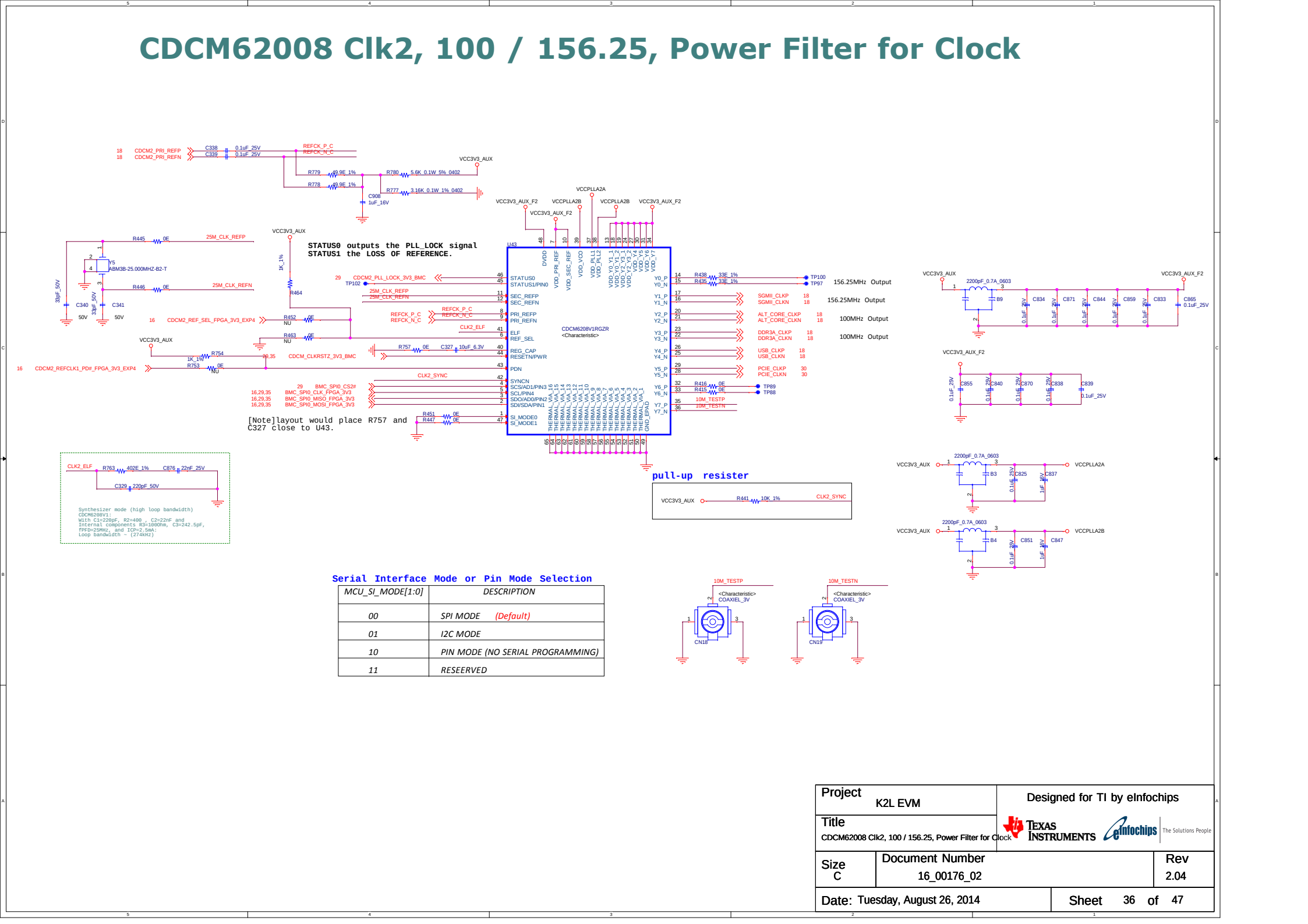
pull-up resistor

Serial Interface Mode or Pin Mode Selection

MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEVERVED

Project: K2L EVM
Title: CDCM62008 Clk2, 100 / 156.25, Power Filter for Clock
Size C
Document Number: 16_00176_02
Date: Tuesday, August 26, 2014

Designed for TI by elnfochips
TEXAS INSTRUMENTS
elinfochips The Solutions People
Rev: 2.04
Sheet 36 of 47



CDCM62008 Clk2, 100 / 156.25, Power Filter for Clock

STATUS0 outputs the PLL_LOCK signal
STATUS1 the LOSS OF REFERENCE.

[Note] layout would place R757 and C327 close to U43.

pull-up resistor

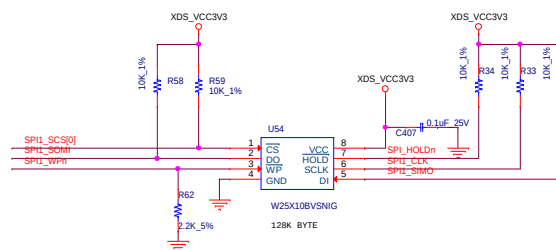
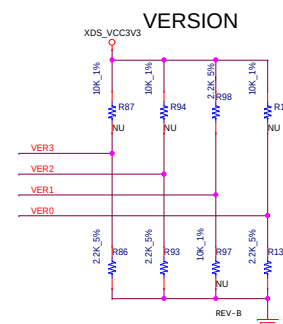
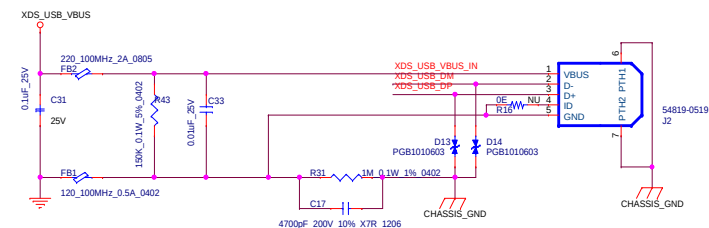
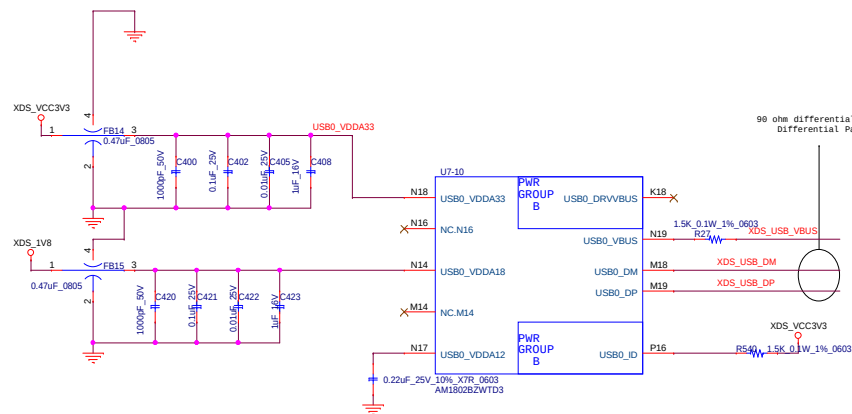
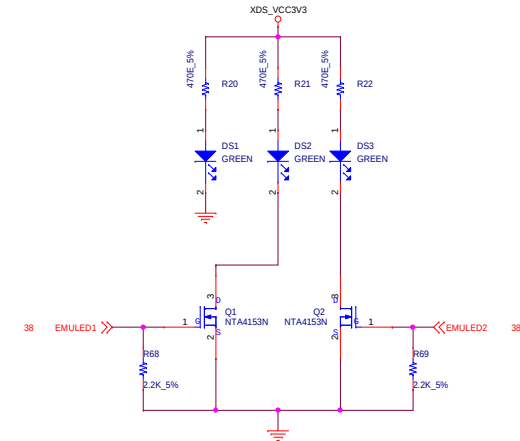
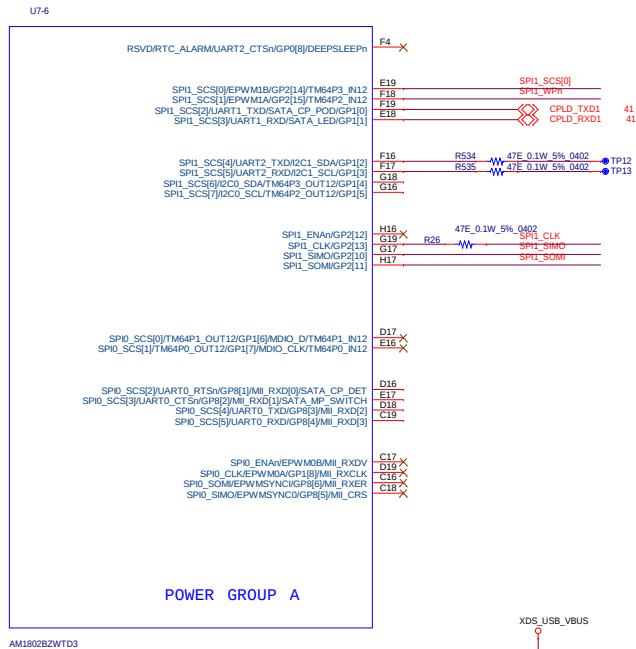
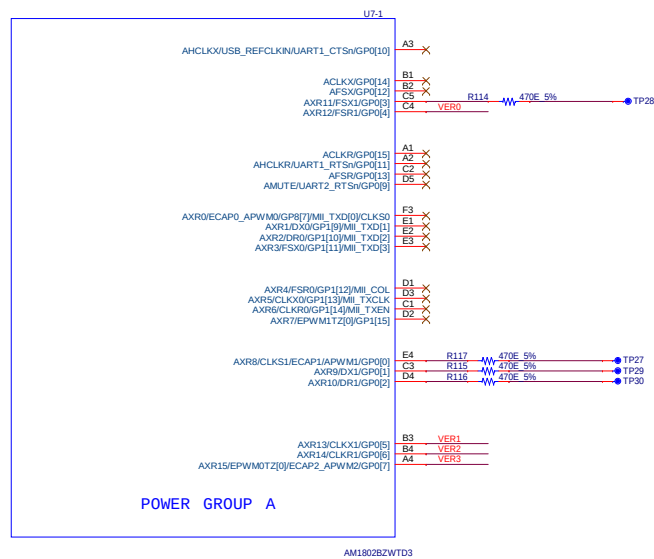
Serial Interface Mode or Pin Mode Selection

MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEVERVED

Project: K2L EVM
Title: CDCM62008 Clk2, 100 / 156.25, Power Filter for Clock
Size C
Document Number: 16_00176_02
Date: Tuesday, August 26, 2014

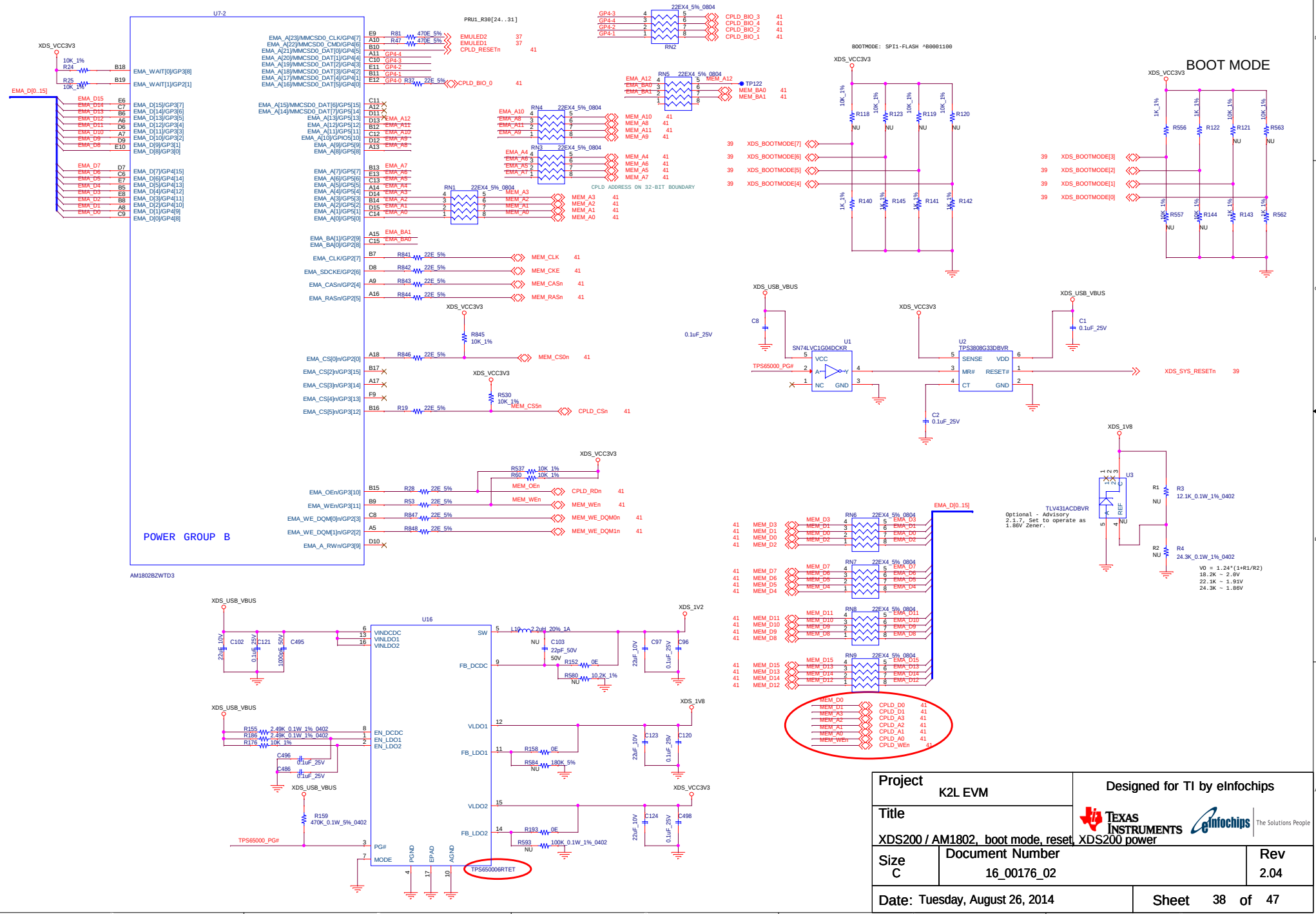
Designed for TI by elnfochips
TEXAS INSTRUMENTS
elinfochips The Solutions People
Rev 2.04
Sheet 36 of 47

XDS200 / AM1802, flash, USB connector for Emulator

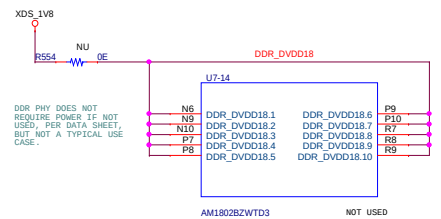
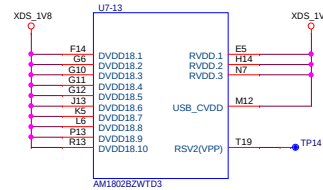
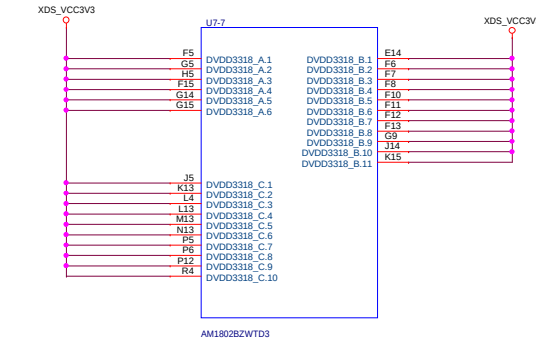
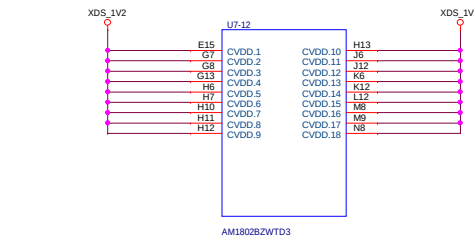
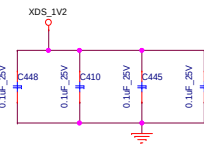
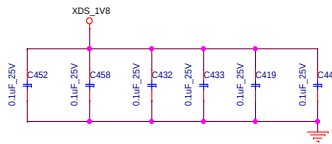
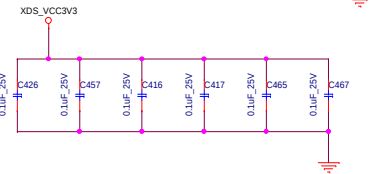
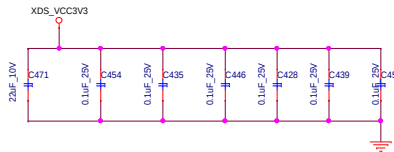
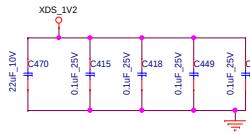
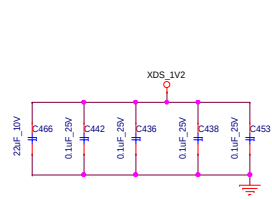


Project K2L EVM		Designed for TI by elnfochips	
Title XDS200 / AM1802, flash, USB connector for Emulator		  The Solutions People	
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 37 of 47	

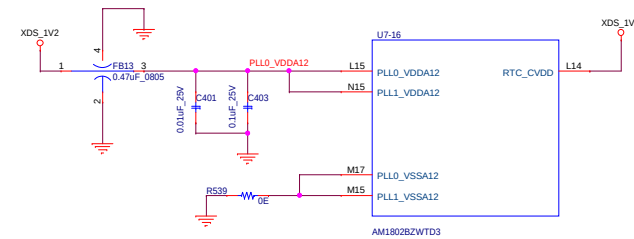
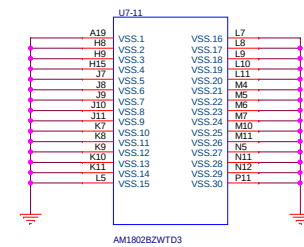
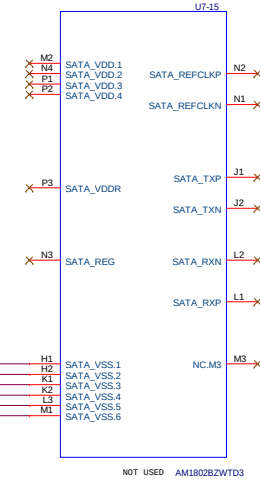
XDS200 / AM1802, boot mode, reset, XDS200 power



XDS200 Power

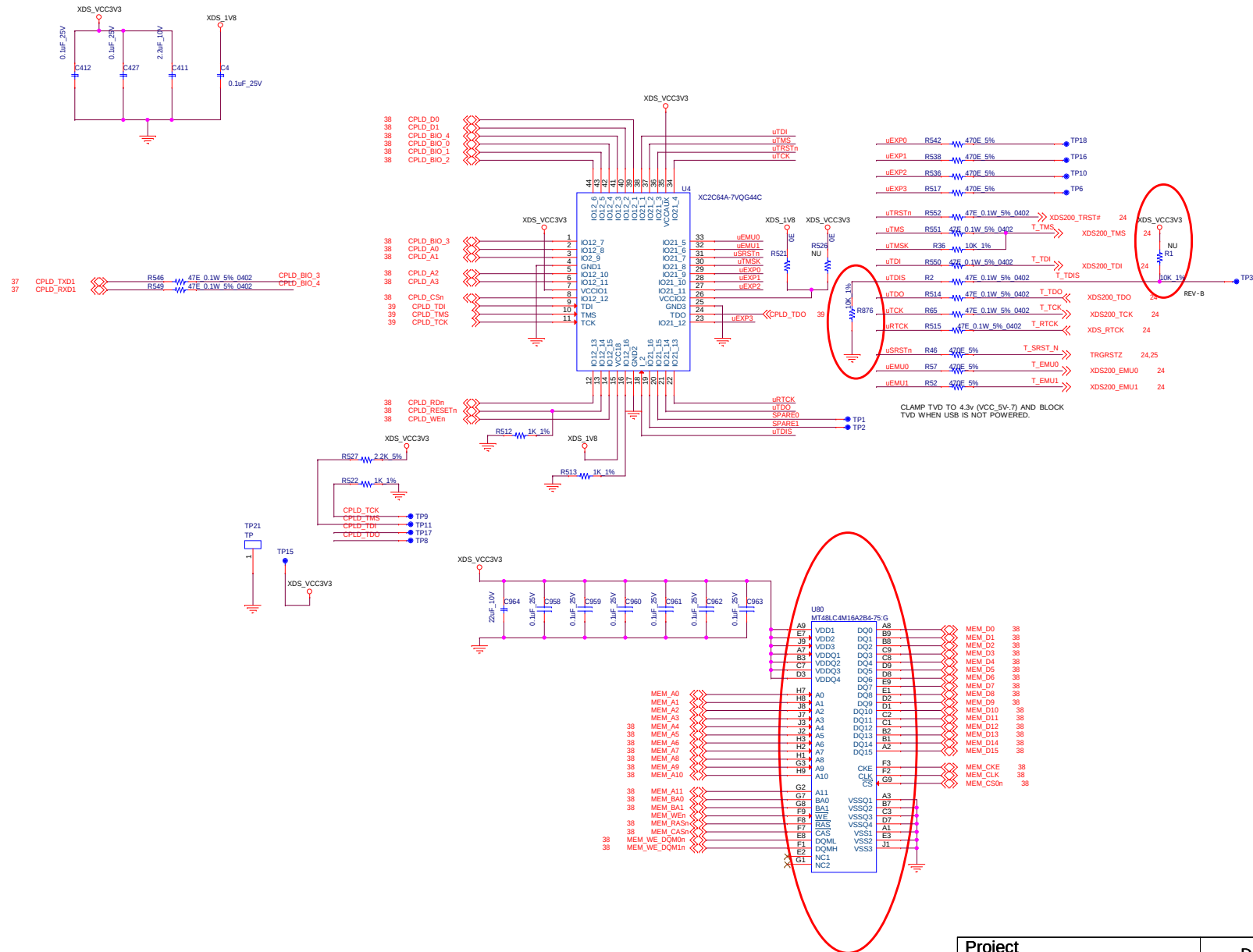


DDR PHY DOES NOT REQUIRE POWER IF NOT USED, PER DATA SHEET, BUT NOT A TYPICAL USE CASE.



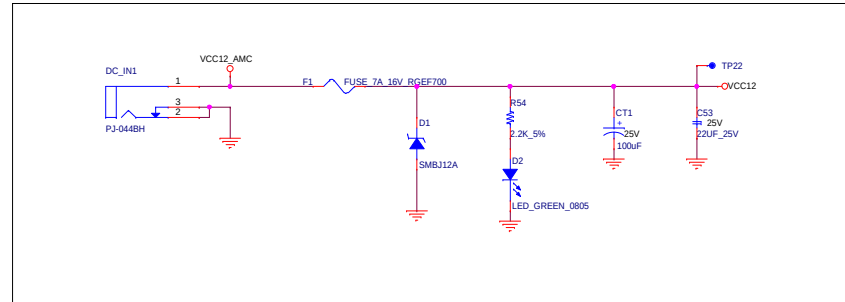
Project K2L EVM		Designed for TI by elnfochips	
Title XDS200 Power		 TEXAS INSTRUMENTS  The Solutions People	
Size C	Document Number 16_00176_02		Rev 2.04
Date: Tuesday, August 26, 2014		Sheet 40 of 47	

XDS200 Emulation CPLD

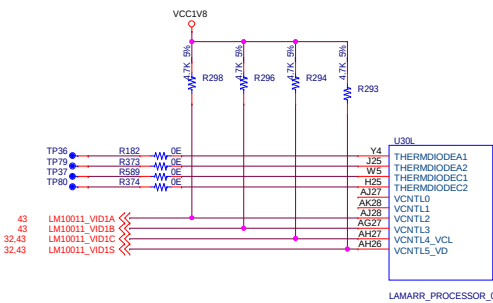
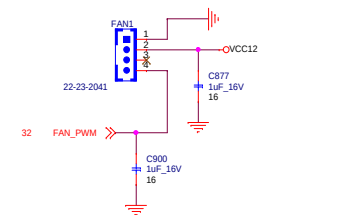


Project K2L EVM		Designed for TI by elnfochips	
Title XDS200 Emulation CPLD		 TEXAS INSTRUMENTS  The Solutions People	
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 41 of 47	

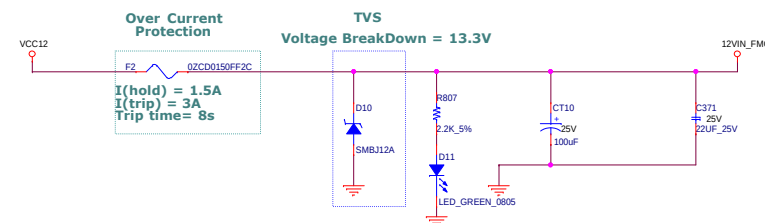
12v input (fused), 12v to 3p3v MP, K2L VID, 1p8 to VPP1p8 switch, 3v3Aux to 3v3, FMC1 Power (fuse), FMC2 Power (fuse), fan connector



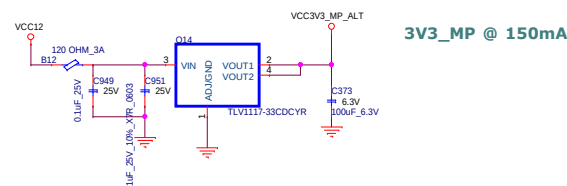
DC FAN Connector for SOC



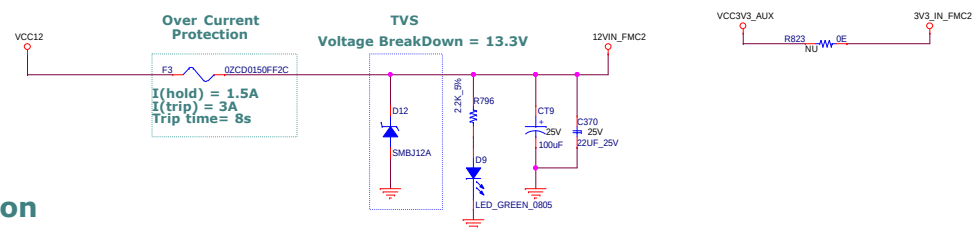
FMC1 POWER



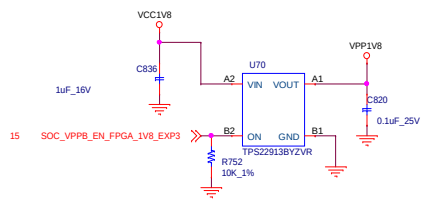
12V to VCC3V3_MP_ALT Generation



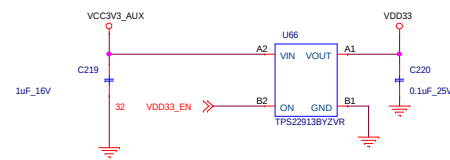
FMC2 POWER



VCC1V8 to VPP1V8



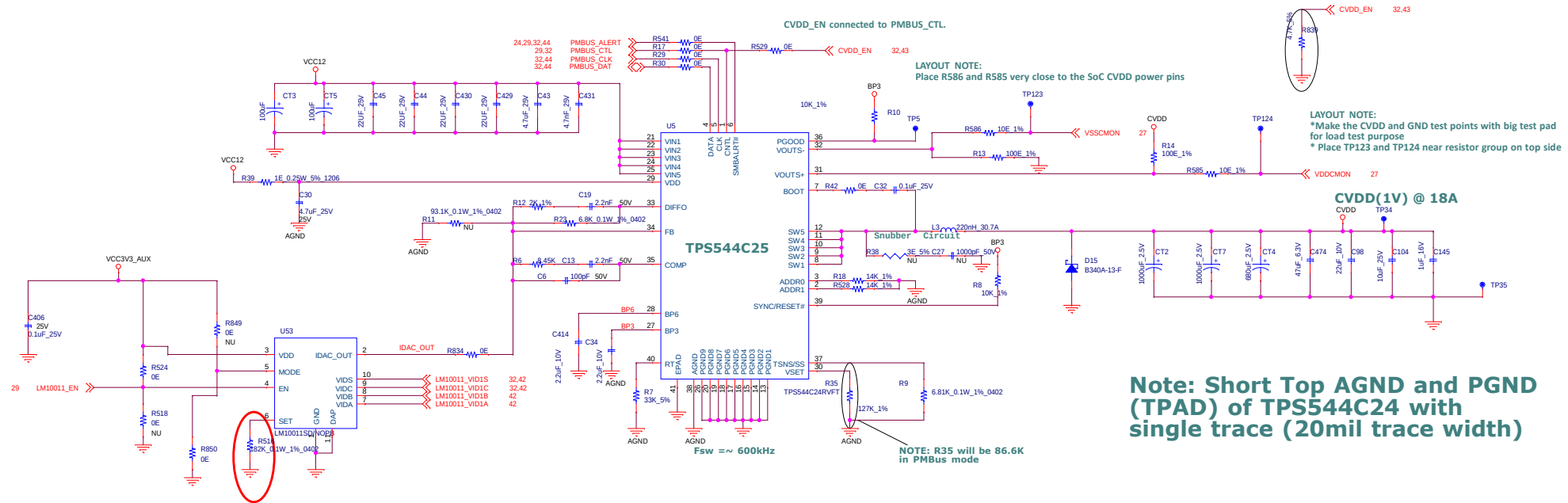
3V3_AUX to VDD33 Generation



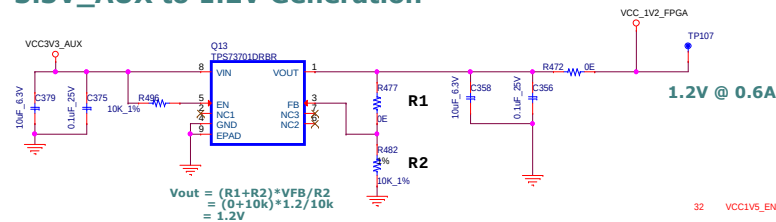
Project K2L EVM		Designed for TI by elnfochips	
Title 12v input (fused), 12v to 3p3v MP, K2L VID, 1p8 to VPP1p8 switch, 3v3Aux to 3v3, FMC1 Power (fuse), FMC2 Power (fuse), fan connector		 The Solutions People	
Size C	Document Number 16_00176_02	Rev 2.04	
Date: Tuesday, August 26, 2014		Sheet 42 of 47	

Top Avatar, 12v to CVVD , 12v to 1.5v, 3.3v aux -> 1.2v, 3.3v aux -> 1.8v

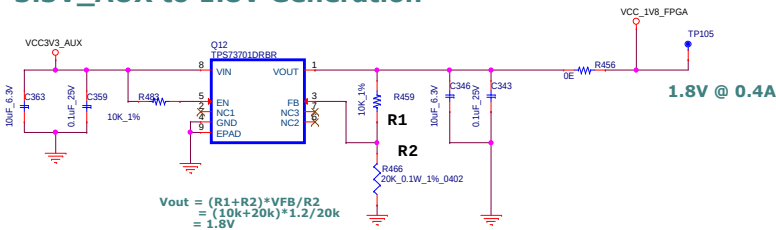
12V to CVDD Generation



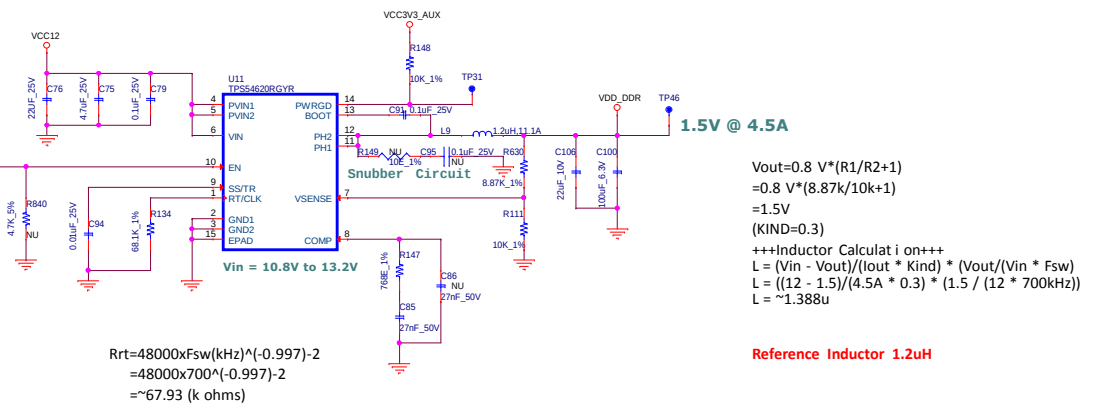
3.3V_AUX to 1.2V Generation



3.3V_AUX to 1.8V Generation



12V to 1.5V Generation

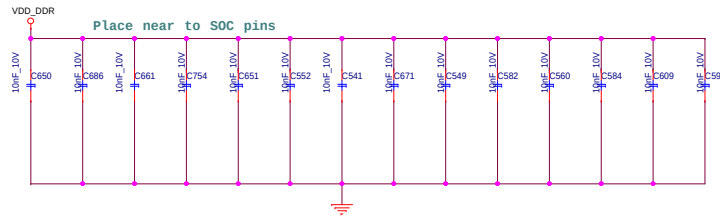
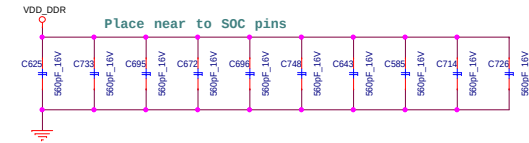
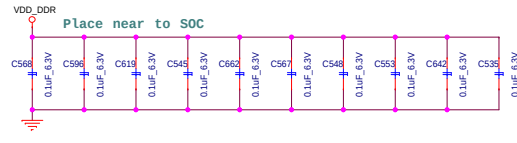
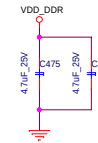
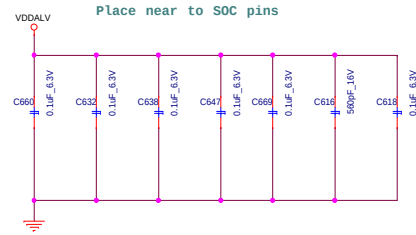
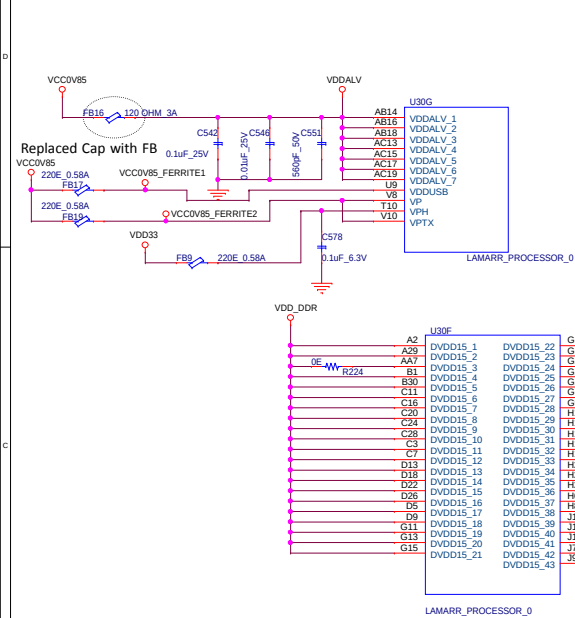


Project		Designed for TI by elfinohips	
K2L EVM		TEXAS INSTRUMENTS elfinohips The Solutions People	
Title		Top Avatar, 12v to CVDD , 12v to 1.5v, 3.3v aux -> 1.2v, 3.3v aux -> 1.8v	
Size C	Document Number	Rev	
	16_00176_02	2.04	
Date: Tuesday, August 26, 2014		Sheet 43 of 47	

D

A

K2L VDDALV, v85 filter, bypass caps, 12v -> 3.3vaux

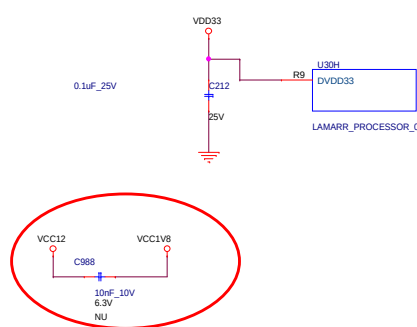
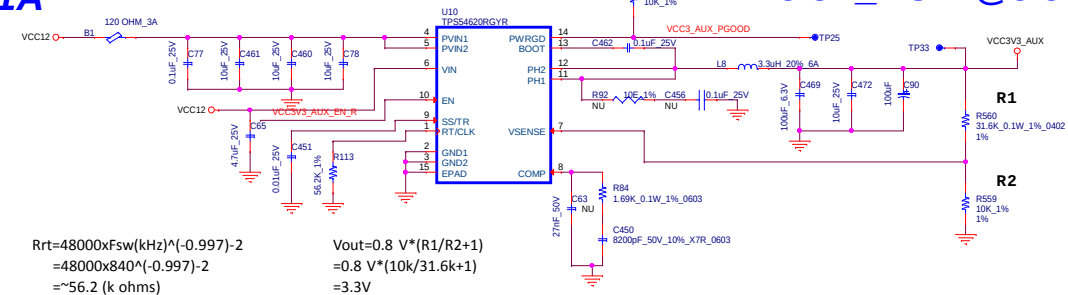


VCC3V3_AUX

Assume 90% Pe,
 $I_{in} = (3.3V * 3.5A) / 90\% / 12V = 1.1A$

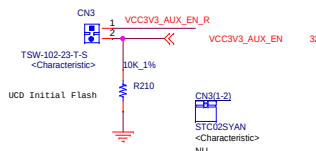
12V@1.1A

3.3V_AUX @3.5A



(Over all tolerance is 5%, DC tolerance is 2.5%) (KIND=0.3)
 +++output capacitor Calculat i on+++
 $C_{out} = (2 * \Delta I_{out}) / (F_{sw} * \Delta V_{out})$
 $C_{out} = (2 * 3.5) / (840kHz * 0.0825)$
 $C_{out} = 110.58uF$
 Reference Capacitor=100uF

+++Inductor Calculat i on+++
 $L = (V_{in} - V_{out}) / (I_{out} * Kind) * (V_{out} / (V_{in} * F_{sw}))$
 $L = ((12 - 3.3) / (3.5A * 0.3)) * (3.3 / (12 * 840kHz))$
 $L = 8.2857 * 0.327u$
 $L = 2.71uH$
 Reference Inductor 3.3uH

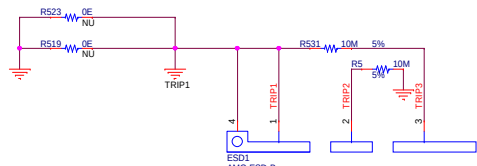


Project K2L EVM		Designed for TI by elfnchips	
Title K2L VDDALV, v85 filter, bypass caps, 12v -> 3.3vaux		 TEXAS INSTRUMENTS  elfnchips The Solutions People	
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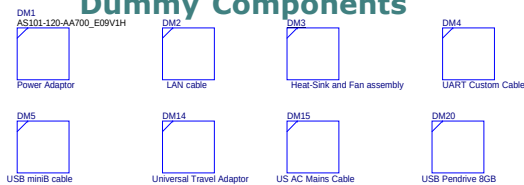
KEYSTONE2 LAMARR EVM - REVISION HISTORY

PCB. REV.	SCH. REV.	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	1.0	Release to Fabrication	24-DEC-2013	eInfochips
	1.01	1. SDRAM circuitry added in XDS section 2. TPS650006 is used instead of TPS650003 in XDS power section 3. Off page connectors used for SOC_I2C0_SDA, SOC_I2C0_SCL, SOC_I2C2_SDA, SOC_I2C2_SCL, LM10011_VID1C, LM10011_VID1S, SOC_UART0_TXD_3V3 nets 4. R626 made NU 5. J1 connector pin out details updated as per J5	23-JAN-2014	eInfochips
	1.02	1. Serdes switch settings changed to I2C mode from pin mode; [Pages - 12, 13, 14] 2. Ethernet configuration settings updated for 2.5V VDDO; [Pages - 31, 33, 34] 3. CP2105 - Self power mode option provided; [Page - 23]	12-MAR-2014	eInfochips
	1.03	1. Layout instruction is given for shorting AGND and PGND at a single point for Top Avatar section. [Page-43] 2. Termination provided for SOC_MDC_2V5 at AMC side. [Page-31] 3. Brightness reduced for the LEDs D5, DBG_D2 and DBG_D2., i.e, R353, R333 and R350 changed tp 120E from 10E [Page-16]	18-MAR-2014	eInfochips
	1.04	1. External networks provided for LVPECL logic implementation on U51 outputs. [Page-15] 2. Netname for the signal "CLK_MUXCTRL2_FPGA_3V3_EXP5" is changed to "CLK_MUXCTRL1_FPGA_3V3_EXP5". [Pages-16,18] 3. Netname for the signal "CLK_MUXCTRL3_FPGA_3V3_EXP5" is changed to "CLK_MUXCTRL2_FPGA_3V3_EXP5". [Pages-16,18]	25-MAR-2014	eInfochips
2.0	2.01	1. 10MHz clock circuit for clamping input signal to +1V. [Page18] 2. R1 made NU and C399 is replaced with R876. [Page41] 3. R90 made NU [Page24] 4. SPI2_MOSI/MISO option is mounted on board instead of UART1_TS/RTS - as UART1/SPI2 are multiplexed at SoC [Page17] 5. IRQ_FMC1_FPGA_3V3 is changed to pin R13 (I/O) from pin R8 (I) of FPGA; IRQ_FMC2_FPGA_3V3 is changed to pin T15 (I/O) from pin P13 (I) of FPGA. [Page16] 6. R413 made NU and R734 mounted with 10K 7. 100E resistor added to input of Clock buffer and other clocks 8. VBUS mode option provided instead of Self Powered Mode for CP2105 circuitry 9. In Cn14, Mfr Pno TSM-108-07-S-S is replaced with TSM-108-02-S-SV	1-MAY-2014	eInfochips
	2.02	1.CN21(2-3) changed to CN6(2-3); CN8(2-3) changed to CN10(2-3); CN2(1-2) changed to CN11(1-2) 2.CN24(1-2) changed to CN3(1-2)	10-JUL-2014	eInfochips
	2.03	DM21 to DM28 added	21-JUL-2014	eInfochips
	2.04	CN9(1-2) is replaced with CN13(1-2); R417 made NU.	4-AUG-2014	eInfochips

Front panel and ESD Strip



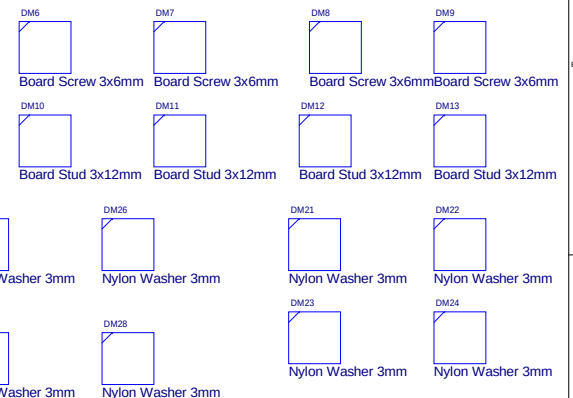
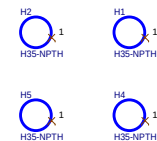
Dummy Components



On Board Fiducials



Mounting Holes



Project K2L EVM		Designed for TI by elnfochips	
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