K2E SCHEMATIC

MAJOR REVISION HISTORY:

<table>
<thead>
<tr>
<th>PCB REV.</th>
<th>SCH. REV.</th>
<th>DESCRIPTION</th>
<th>DATE</th>
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<td>1.0</td>
<td>1.0</td>
<td>Proto Build</td>
<td>15-NOV-2013</td>
</tr>
<tr>
<td>2.0</td>
<td>2.0</td>
<td>Alpha Build</td>
<td>05-MAR-2014</td>
</tr>
<tr>
<td>2.0</td>
<td>2.01</td>
<td>Alpha ECNs Implemented</td>
<td>24-APR-2014</td>
</tr>
</tbody>
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I2C ADDRESS TABLE:

<table>
<thead>
<tr>
<th>REF DES</th>
<th>DESCRIPTION</th>
<th>7 BIT ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPROM1</td>
<td>1MBit I2C EEPROM</td>
<td>0x50</td>
</tr>
<tr>
<td>SODIMM</td>
<td>SODIMM EEPROM</td>
<td>0x53</td>
</tr>
<tr>
<td>U4</td>
<td>UCD9090</td>
<td>0x68</td>
</tr>
</tbody>
</table>

PCB MECHANICAL DETAILS:

1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. NUMBER OF LAYERS: 12
3. IMPEDANCE CONTROL: YES

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.
SCHEMATIC PAGE DESCRIPTION:

01: COVER PAGE
02: TABLE OF CONTENTS
03: SYSTEM BLOCK DIAGRAM
04: PLACEMENT
05: POWER CONSUMPTION
06: POWER SEQUENCE
07: POWER DISTRIBUTION
08: CLOCK DIAGRAM
09: BMC BLOCK DIAGRAM
10: AMC CONNECTOR
11: SPI TO GPIO Connector
12: SOC SGMII PCIE_MCM
13: SOC XFI USB
14: SOC DDR3
15: EMU & JTAG
16: PCIe to SATA
17: SOC EMIF NAND
18: MISC
19: SOC CLOCK & Smart-Reflex
20: SOC POWERA
21: SOC POWERB
22: SOC GND
23: CLOCK SOURCE--1
24: CLOCK SOURCE--2
25: DDR3 SODIMM AND BMC LCD
26: SGMII Ethernet PHY
27: BMC LM3S2D93
28: BMC MISC
29: mTCA ZD3/120-pin Exp.
30: POWER SUPPLY--1
31: POWER SUPPLY-2
32: XDS200_1
33: XDS200_2
34: XDS200_3
35: XDS200_POWER
36: XDS200_EMULATION
37: REVISION HISTORY
## POWER CONSUMPTION

### Approx Power Consumption for TI_EVM - EDISON

<table>
<thead>
<tr>
<th>Components Part No.</th>
<th>Description</th>
<th>Quantity Per Board</th>
<th>Current Consumed by corresponding device on power supply (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.75</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VTT</td>
</tr>
<tr>
<td>65AK2E15</td>
<td>Processor</td>
<td>1</td>
<td>800</td>
</tr>
<tr>
<td>M128F4C08A8BNR6HCD</td>
<td>NAND Flash</td>
<td>1</td>
<td>100</td>
</tr>
<tr>
<td>MT18KSF51272-2T-1G4</td>
<td>DDR1 SODIMM Module</td>
<td>1</td>
<td>600</td>
</tr>
<tr>
<td>LCD</td>
<td>LCD display</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>LM35Q353</td>
<td>Microcontroller</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>BSE9182</td>
<td>Gigabit ethernet phy</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>5EP210S</td>
<td>PCIe to SATA controller</td>
<td>1</td>
<td>663</td>
</tr>
<tr>
<td>K2SO12BA16SSF-0F</td>
<td>SPI EEPROM</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>MD252X77T6SS</td>
<td>Memory chip</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>DC20R208</td>
<td>Reference Clock generator</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>USB</td>
<td>USB 3.0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>SATA</td>
<td>SATA 3.0 HDD</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>FAN</td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Misc</td>
<td></td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

| Total Current on individual power supply (mA) | 600 | 800 | 1800 | 16000 | 2988 | 1286 | 9 | 45 | 554 | 831 | 2528 | 100 |
| 10% margin added over design (mA)            | 660 | 880 | 1980 | 17600 | 3286.8 | 1414.6 | 8.8 | 49.5 | 609.4 | 914.1 | 2791.8 | 110 |

### Power Consumption in mW

| TPS510905.1V  | 9.75W | 660.86mA |
| LMM3430.1V  | 7.57W | 77.57mA |
| LMX3430.1V  | 9.59W | 195.94mA |
| TPS4402S2.1V  | 1.63W | 1725.48mA |
| TPS3402S2.1V  | 1.63W | 573.66mA |
| LMX3402S2.1V | 1.63W | 241.31mA |
| LMX3430.1V  | 3.65W | 52.94mA |
| TPS73701S.3V  | 2.29W | 7.84mA |
| TLV911.3VOCY  | 2.29W | 689.89mA |
| LMX3402S2.1V | 3.65W | 269.66mA |
| TPS4402S2.1V  | 5.09W | 1264.85mA |

| Total Current @ 3.3V | 9.27A |
| Total Current @ 5V | 2.74A |
| Total Current @ 12V | 5.06A |
| Total Power | 61.64W |

**Note:**

1) Power consumption for 65AK2E15 is taken as TDP @ 90C & 1.4GHz (worst case)
K2E_EVM (EDISON) -- POWER SEQUENCE

Notes:
1. Project is a copy of "Power Sequencing -- Core Logic AVD 1.4", with power states removed except for Reset.
LAYOUT NOTE: Place R629 and R630 close to SoC

LAYOUT NOTE: Place ALL PCIe DC-blocking caps close to the TX pins
LAYOUT NOTE:
- Place termination resistors for EMU_TCK, TDI, TMS as close to MIPI-60 header as possible.
- Place termination resistors for SOC_TDO and SOC_EMU* signals as close to the SoC as possible.

LAYOUT NOTE:
- Place U55 as close to MIPI-60 header as possible to minimize stubs on SOC_EMU_19_R and SOC_EMU_20_R.

LAYOUT NOTE:
- Place U55 as close to MIPI-60 header as possible to minimize stubs on SOC_EMU_19_R and SOC_EMU_20_R.
PCle TO SATA CONTROLLER

Place these capacitor near to U75
Note: NAND FLASH Device size is 4Gb.
SoC UART0 TO USB

128Mb SPI NOR Flash

I2C EEPROM

Debug LEDs

I2C–0 1V8 to 3V3 CONVERTER

I2C–1 1V8 to 3V3 CONVERTER

I2C–1 PMBus Connection

I2C–2 1V8 to 3V3 CONVERTER

3V3 I2C ISOLATOR

NOTE:
- VCC1V8 mode (Default): Pull downs are installed and Pull-ups are NO
- PMBus Mode: Install Pull-ups and de-populate Pull-downs

Designed for TI by eInfochips

DU/NC1
DU/NC2
DU/NC3
DU/NC4
DU/NC5
DU/NC6
DU/NC7
DU/NC8

Project

Title

MISC

Document Number

16_00175_02

Size C

Doc. No.

Rev

2.01

Date: Wednesday, May 14, 2014

Sheet 18 of 37
These caps are added for provision only. Values can be changed based on PI analysis result.
CLOCK SOURCE-- 1

From MCU connect to this signal

Serial Interface Mode or Pin Mode Selection

<table>
<thead>
<tr>
<th>MCU_SI_MODE[1:0]</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>SPI MODE (Default)</td>
</tr>
<tr>
<td>01</td>
<td>I2C MODE</td>
</tr>
<tr>
<td>10</td>
<td>PIN MODE (NO SERIAL PROGRAMMING)</td>
</tr>
<tr>
<td>11</td>
<td>RESERVED</td>
</tr>
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</table>
CLOCK SOURCE --2

Serial Interface Mode or Pin Mode Selection

<table>
<thead>
<tr>
<th>MCU_SI_MODE[1:0]</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>SPI MODE (Default)</td>
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<tr>
<td>01</td>
<td>I2C MODE</td>
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<td>10</td>
<td>PIN MODE (NO SERIAL PROGRAMMING)</td>
</tr>
<tr>
<td>11</td>
<td>RESERVED</td>
</tr>
</tbody>
</table>
BMC INTERFACE

Power for BMC

Budget 150mA

Note: LED Color is RED

Note: LED Color is GREEN

Note: LED Color is BLUE

Note: PUSH Buttons Color is BLACK
Note: PUSH Buttons Color is RED
Note: PUSH Buttons Color is BLACK

Project: K2E EVM
Title: BMC

Designed for TI by einfochips

Document Number: 16_00175_02
Rev: 2.01

Size: C

Date: Wednesday, May 14, 2014
Sheet: 27 of 37
Power Sequencing (UCD9090)

PMBus Address Pins

<table>
<thead>
<tr>
<th>PMBus Address</th>
<th>PMBus RESISTANCE (K ohms)</th>
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<tbody>
<tr>
<td>OPEN</td>
<td>--</td>
</tr>
<tr>
<td>11</td>
<td>200</td>
</tr>
<tr>
<td>19</td>
<td>154</td>
</tr>
<tr>
<td>9, 10</td>
<td>118</td>
</tr>
<tr>
<td>3, 7, 8</td>
<td>90.9</td>
</tr>
<tr>
<td>5, 6</td>
<td>53.6</td>
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<tr>
<td>11, 13</td>
<td>41.2</td>
</tr>
<tr>
<td>4</td>
<td>31.6</td>
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<tr>
<td>SMOOTH</td>
<td>--</td>
</tr>
</tbody>
</table>

Slave I2C Address = 0x68
{Internal ADDR[7:5] = 0b110}
the interfaces on the 120-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS

LAYOUT NOTE: Place R623, R653, C874, C896 close to J2 connector
12V to CVDD Generation(TPS544C24)

LAYOUT NOTE:
C842 (4.7nF) must connect very close to VIN pins of TPS544C24

NOTE: R593 must be unpopulated in PMBus mode and VCNTL mode.

LAYOUT NOTE:
R267 must connect to VIN pins very close to VIN pins of TPS544C24

LAYOUT NOTE:
Currently, AGND and PGND are NOT shorted in schematic, to keep 2 separate grounds in layout design file. However, they should be shorted in layout design file ONLY at SINGLE point, i.e.: Pin 38 can be directly
connected to Thermal Pad with thicker trace

NOTE: R569 will be 51.1K in PMBus mode

LM26430(Quad Switcher)

LAYOUT NOTE:
Follow Layout Instruction guidelines

Slave I2C Address = 0x49

CVDD(1V) @ 18A

LM26430

CVDD1 (0.95V) @ 2.5A

VCC3V3_AUX @ 2A

0.85V @ 1.85A

VCC1V8 @ 2A

Project
K2E EVM

Designed for TI by einfochips

Title
POWER SUPPLY--2

Size
C

Document Number
16_00175_02

Rev
2.01

Date: Wednesday, May 14, 2014

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K2E EVM - REVISION HISTORY

<table>
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<th>PCB REV</th>
<th>SCH. REV</th>
<th>CHANGE DESCRIPTION</th>
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<td>1.0</td>
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<td>15-NOV-2013</td>
<td>eInfochips</td>
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</table>
| 1.01    | 1.0      | 1) LM26430: Pin#39 and #44 swapped
2) CDCM6208BV1: CLK_RST connection near to U17 is corrected
3) R601/R602 added on U17,Sec input
4) SGMIICLK#N shifted to V5 from Y1
5) AMC: DSP_PMBUS_EN changed to PFO from PE2
6) XDS200: Added a SDRAM & related circuitry
7) U20 part# changed to TPS650006, fixed version of TPS65000, Changed R185, R194, R202 to 0E and Marked R180, R196, R199, C100 as NU | 03-JAN-2014 | eInfochips |
| 2.0     | 2.0      | 1) Power: R611, R612 (NU) added on LM10011 Mode pin
2) TA: IC part# changed to TPS544C24 in place of TPS544B24
3) R628 changed to 127K, R590 changed to 215K, R587 changed to 6.81K
4) TP added near to R547 on VSSCMON signal
5) RC Snubber package size changed
6) U79 added for PMBUS_ALERT signal connection to SoC
7) SoC RSVxxx pin net names changed | 21-JAN-2014 | eInfochips |
| 1.03    | 1.03     | 1) Power: R611, R612 (NU) added on LM10011 Mode pin
2) TA: IC part# changed to TPS544C24 in place of TPS544B24
3) R628 changed to 127K, R590 changed to 215K, R587 changed to 6.81K
4) TP added near to R547 on VSSCMON signal
5) RC Snubber package size changed
6) U79 added for PMBUS_ALERT signal connection to SoC | 25-FEB-2014 | eInfochips |
| 1.04    | 1.04     | - Released for Fabrication | 05-MAR-2014 | eInfochips |
| 2.01    | 2.01     | - Released for Fabrication | 10-MAR-2014 | eInfochips |
| 2.01    | 2.01     | - Block Diagram, aesthetical changes made | 24-APR-2014 | eInfochips |

**Dummy Components**

- DM1-DM14
- CN9(1-2)1 STC02SYAN
- DM9-DM12
- DM13-DM17
- DM18

**Mounting Holes**

- H3 H35-NPTH
- H4 H107x17-NPTH
- H5 H35-NPTH
- H6 H27P35-MTH
- H7 H35-NPTH
- H8 H27P35-MTH
- H9 H35-NPTH
- H10 H27P35-MTH
- H11 H35-NPTH
- H12 H27P35-MTH
- H13 H35-NPTH
- H14 H27P35-MTH
- H15 H35-NPTH
- H16 H27P35-MTH

**On Board Fiducials**

- FM1-FM5
- FM6-FM7
- FM8-FM10

**AMC Hole**

- AMC-ESD-B

**Front panel and ESD Strip**

- ESD1 AMC-ESD-B
- ESD2 AMC-ESD-B

**Design Information**

- Designed for TI by eInfochips