C6657 Lite EVM Known Issues

1. **SGMII at AMC edge and MDIO between DSP and Eth PHY are not working in Alpha boards i.e. PCB REV : 17-00132-01.**

   In Alpha boards (PCB REV: 17-00132-01) SGMII at AMC edge and DSP to Eth PHY MDIO interface is not stable due to noise coupling to these signals. Please locate silk label at bottom side of the PCB to check if your EVM is Alpha version i.e. PCB REV : 17-00132-01.

   This issue is resolved from PCB REV: 17-00132-02 (Beta) and onwards.

2. **EMAC Boot issue**

   In Alpha & Beta version of EVMs, there are chances that the EMAC boot may not work on power-on reset. The root cause of this problem is Ethernet PHY could not initialize before DSP reset.

   Workaround: Please update the FPGA using C6657 Gauss EVM_FPGA_v02.bit file. After updating FPGA keep switch settings for EMAC boot and power cycle the EVM.

3. Communication glitch in MDIO interface between DSP and Ethernet PHY

In **all versions** of EVMs, there are chances that the DSP could not read/write Ethernet PHY registers at few random occasions. This problem is more pre-dominant when MDC operated at 1 MHz or higher rate.

Workaround: Please Un-mount resistors R85 and R957 (highlighted below in yellow color). Change resistors R82 and R83 to 10K (highlighted below in green color).

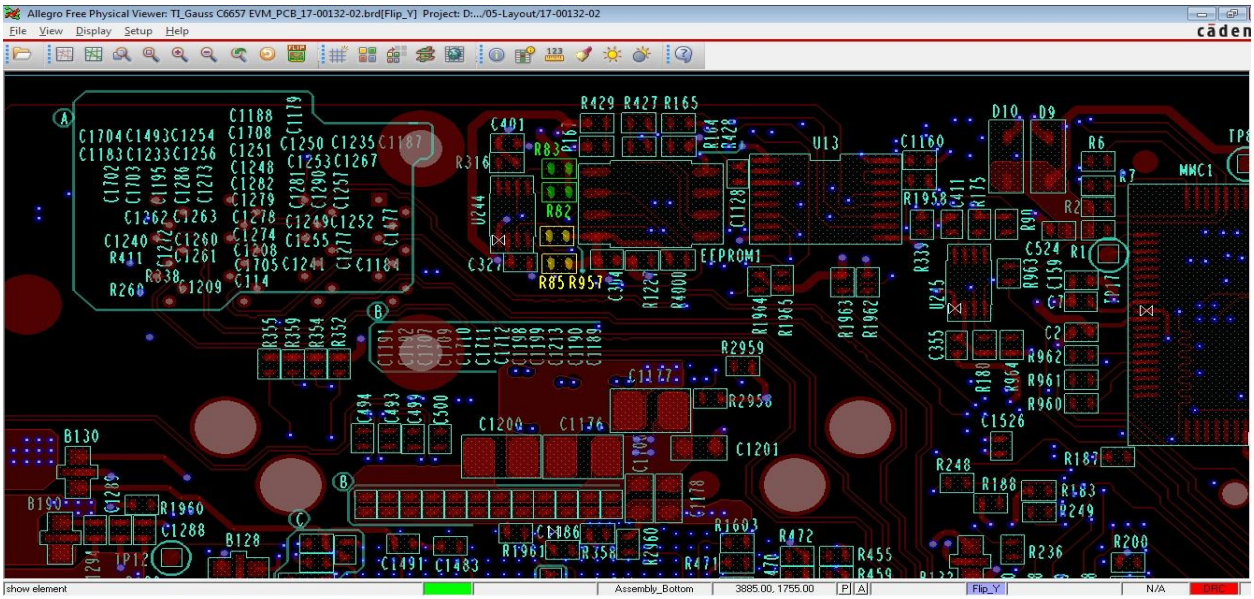

Figure 1: Bottom Pads and Bottom Assembly Layer

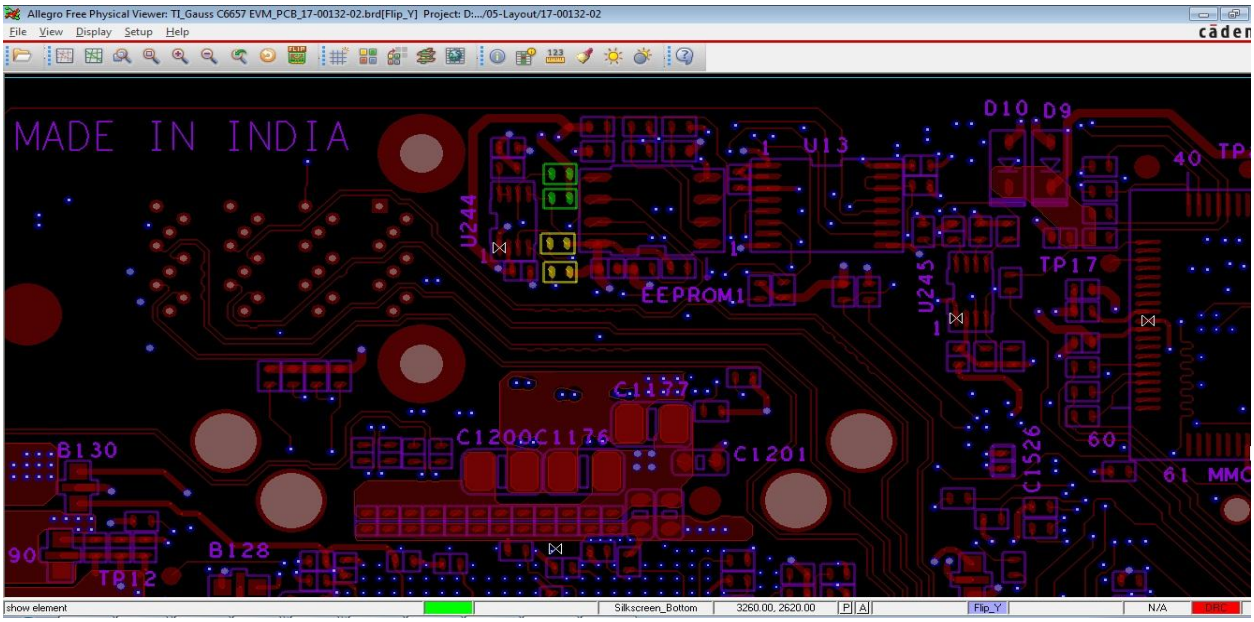

Figure 2: Bottom Pads and Bottom Silk Layer

4. **Redundant pull-up and terminations on EMU_TCK**

   The resistors R896, R67 and capacitor C555 are redundant components and can be removed from design. Also pull-up resistor R1119 should change from 10K to 4.7K.

5. **Failure to operate PCIe in an ATX chassis when using the TMDXEVMPCI adapter**

   All **production** version EVMs are not detected when inserted in ATX chassis using TMDXEVMPCI adapter.

   Workaround: The standard IBL (created for the C6678 workaround) contains PCIe configuration writes that are needed to enable robust operation in an ATX computer chassis. The FPGA version v02 redirects the C6657 to boot from the IBL even when the DIP switches are programmed for PCIe end-point boot. These PCIe configuration writes will be needed in the customer application to enable C6657 operation in an ATX computer.

   FPGA bit file of version v02 is available at below link:
   http://www.einfochips.com/texas-instruments/texas-instruments-tms320c6657-lite-evm-support.php

6. **GEL file and MCSDK code delivered with the EVM operates the DDR3 at half speed**

   GEL file and MCSDK code delivered with **all versions** of EVM, operates the DDR3 at half speed.

   Workaround: To run the DDR3 at full speed user need to request latest GEL file through e2e forum until the new EMU pack is ready.