TMDSEVM6457L Schematic

SCHEMATIC PAGE DESCRIPTION :

01 : COVER SHEET
02 : SYSTEM BLOCK DIAGRAM
03 : DSP - CLOCK, CONFIGURATION, I2C-UART BRIDGE
04 : JTAG EMULATION (ON BOARD / EXTERNAL HEADER)
05 : DDR2 INTERFACE
06 : ETHERNET INTERFACE
07 : SRIO INTERFACE, MMC, AMC CONNECTOR
08 : HPI, EMIF INTERFACE
09 : DSP POWER
10 : FPGA - NAND FLASH INTERFACE
11 : BOARD POWER SUPPLY & RESET CIRCUITRY
12 : REVISION HISTORY & DUMMY PARTS

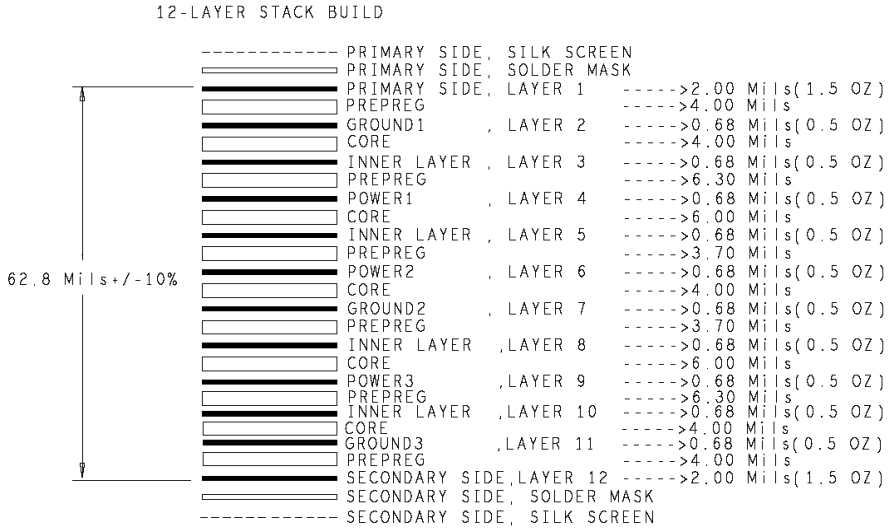
MAJOR REVISION HISTORY :

PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	1.0	Proto Build	28-JULY-2010
	1.1	Pilot Batch	17-SEP-2010
2.0	2.0	Production Batch	11-OCT-2010

I2C ADDRESS TABLE :

REF DES	DESCRIPTION	7 BIT ADDRESS
U22	I2C EEPROM	0x50, 0X51
U23	I2C - UART BRIDGE	0x4D

PCB LAYER STACK-UP DETAILS :



PCB Mechanical Details :

1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. PCB MATERIAL: FR4
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.

Project: TMDSEVM6457L	Designed for TI by eInfochips	
Title: COVER SHEET	Texas Instruments / eInfochips The Solutions People	
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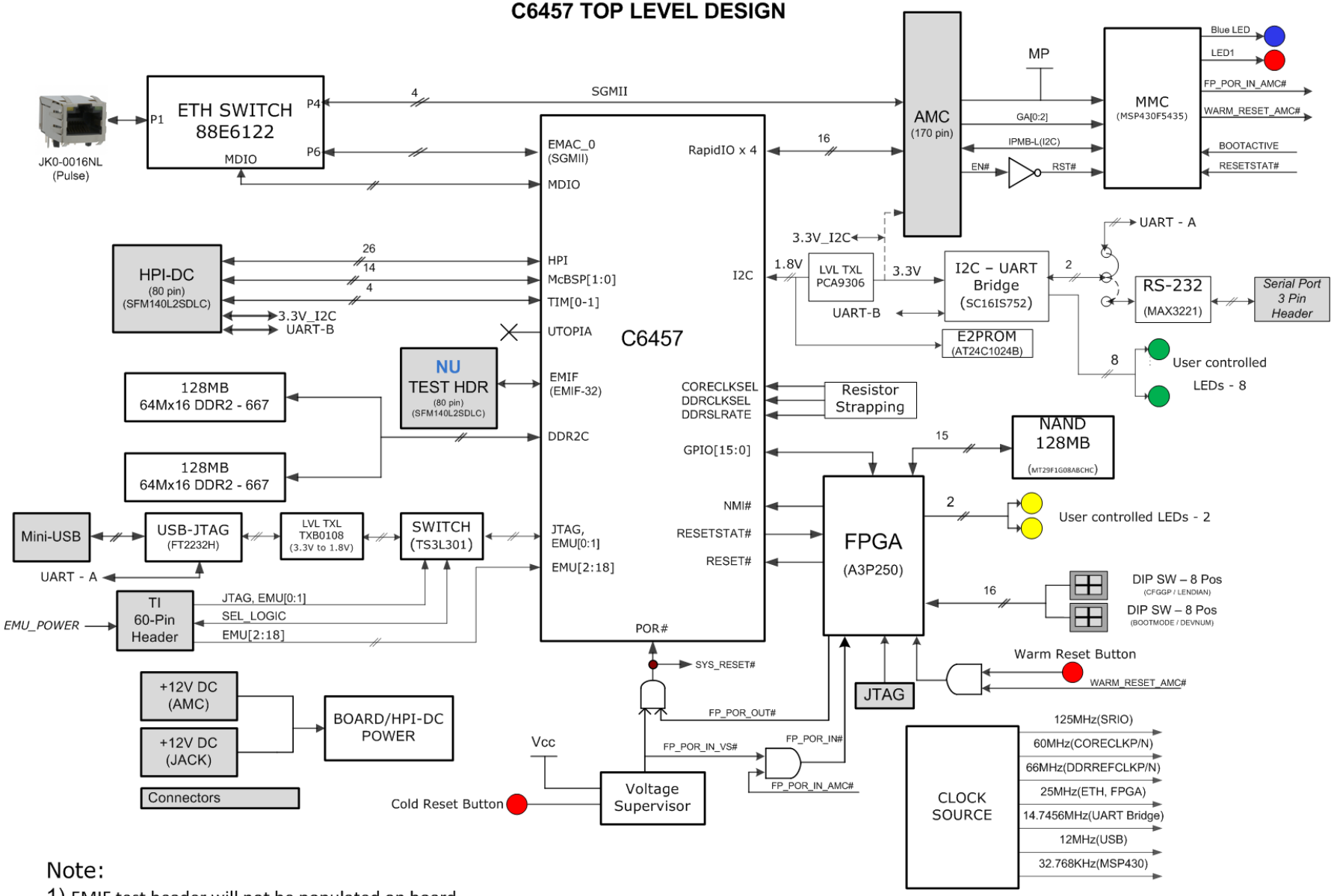
C6457 TOP LEVEL DESIGN



Note:

1) EMIF test header will not be populated on board.

Project: TMDSEVM6457L		Designed for TI by eInfochips
Title: System Block Diagram		
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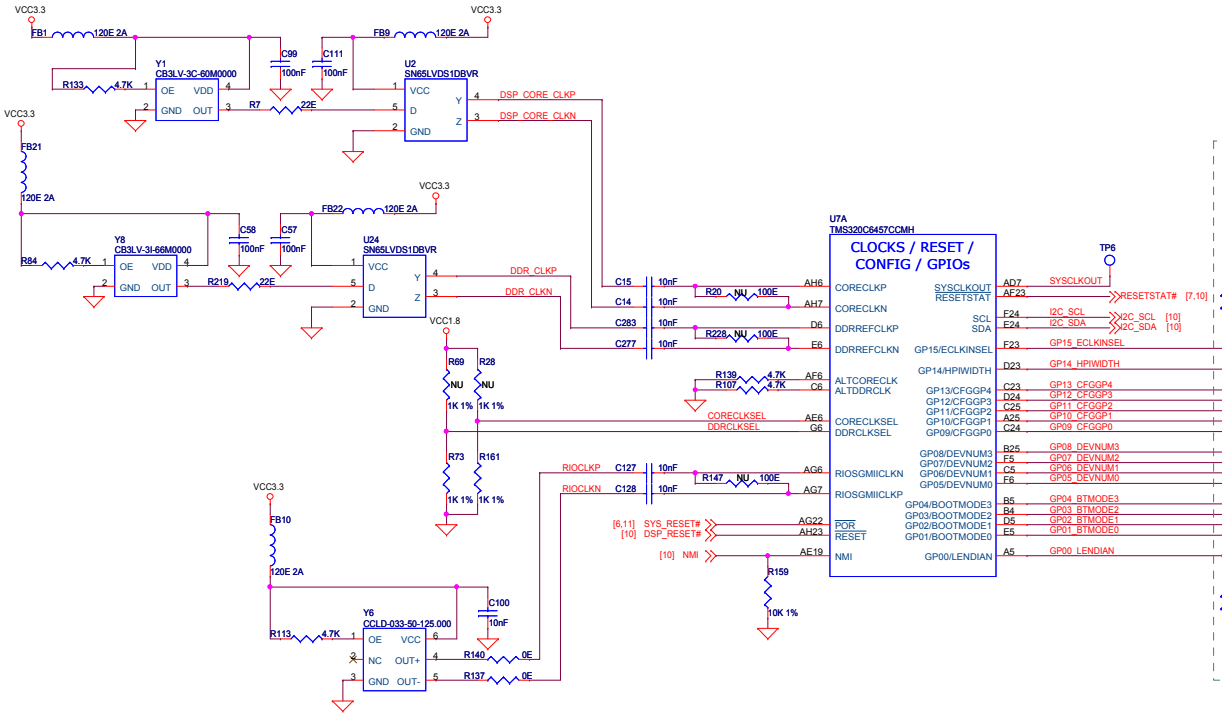
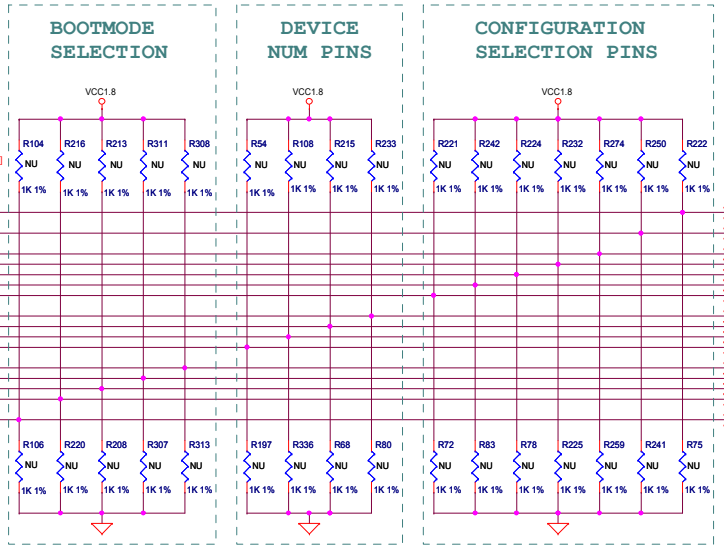
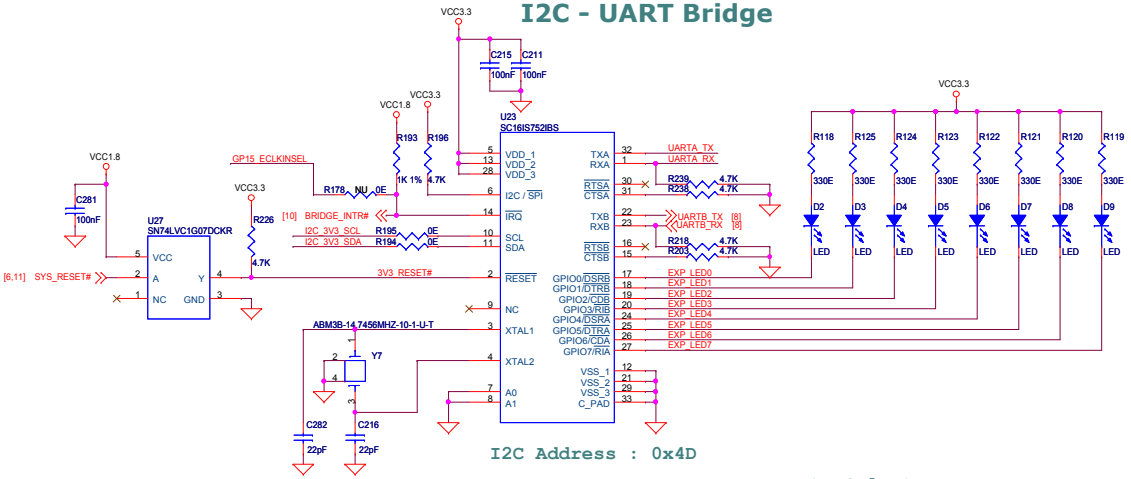


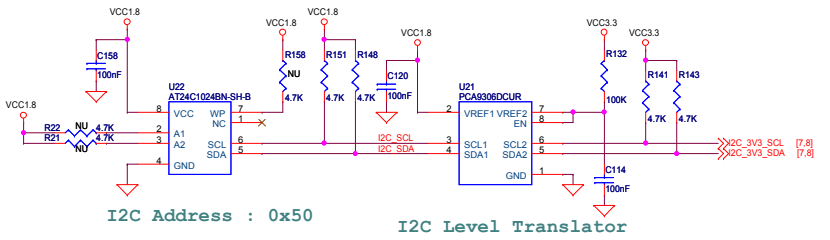
FPGA to drive GP[15:00] signals at reset



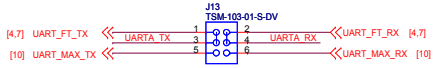
BOOTMODE[3:0]	DESCRIPTION
0000 (0)	No boot
0001 (1)	I2C Master boot (address : 50H) -- Default
0010 (2)	I2C Master boot (address : 51H)
0011 (3)	I2C Slave boot
0100 (4)	Host (HPI) boot
0101 (5)	EMIFA boot
0110 (6) - 1000 (8)	EMAC boot
1001 (9)	Reserved
1010 (10) - 1101 (13)	RIO (Config[0:3]) boot

I2C - UART Bridge





UART Route Select Jumpers



J13.3 to J13.1 & J13.4 to J13.2: UART over USB Connector (Default)
J13.3 to J13.5 & J13.4 to J13.6: UART over 3-Pin Header J12

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Title: DSP Configuration, UART Bridge		
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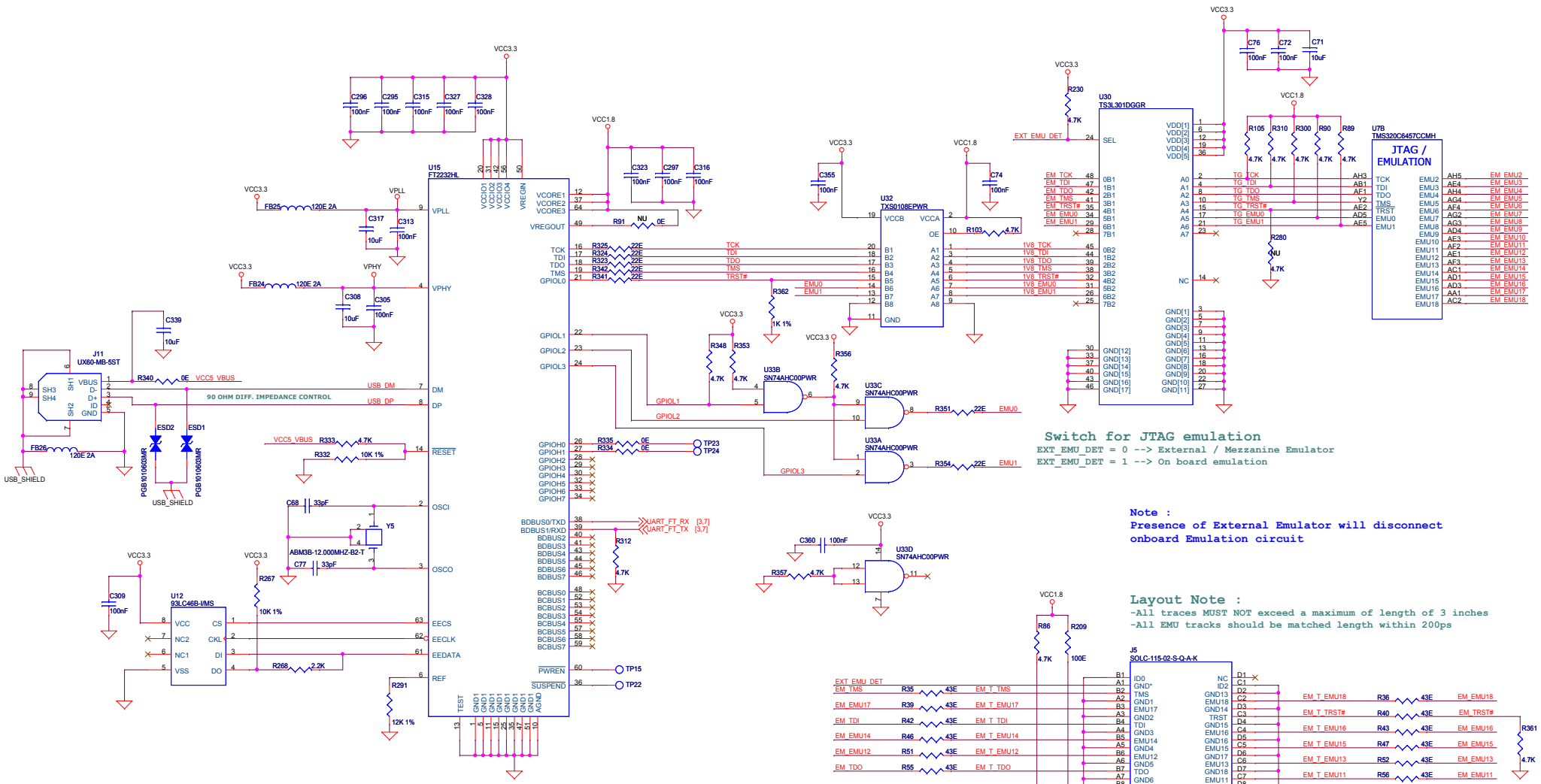

Project: TMDSEVM6457L	Designed for TI by eInfochips	
Title: JTAG Emulation		
Size: C	Document Number: 16-00079-02	Rev: 2.0
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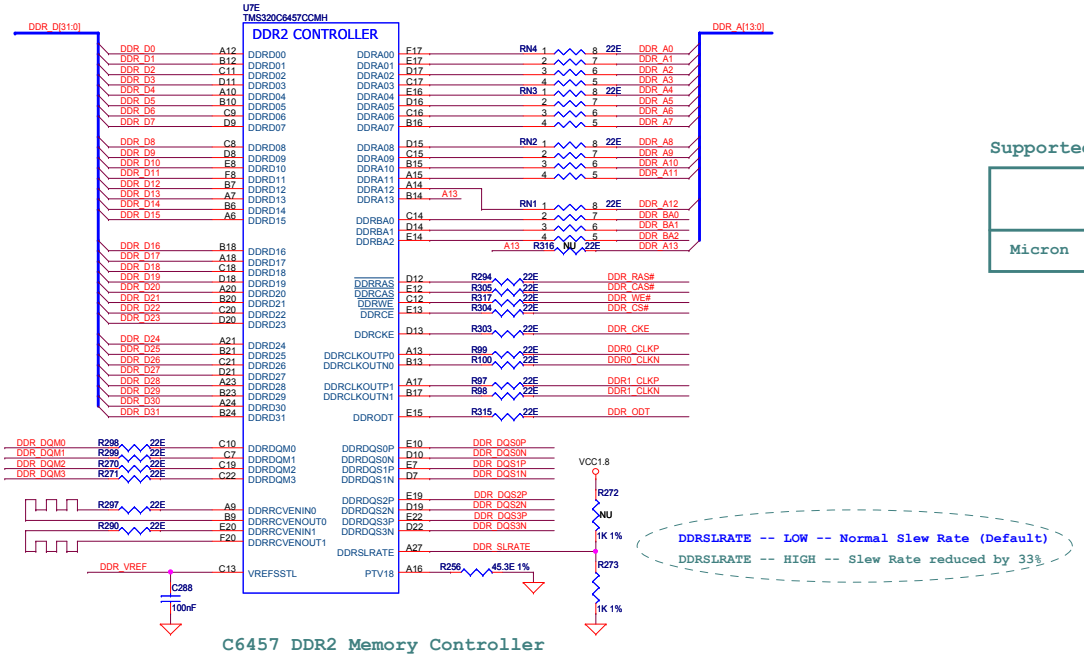
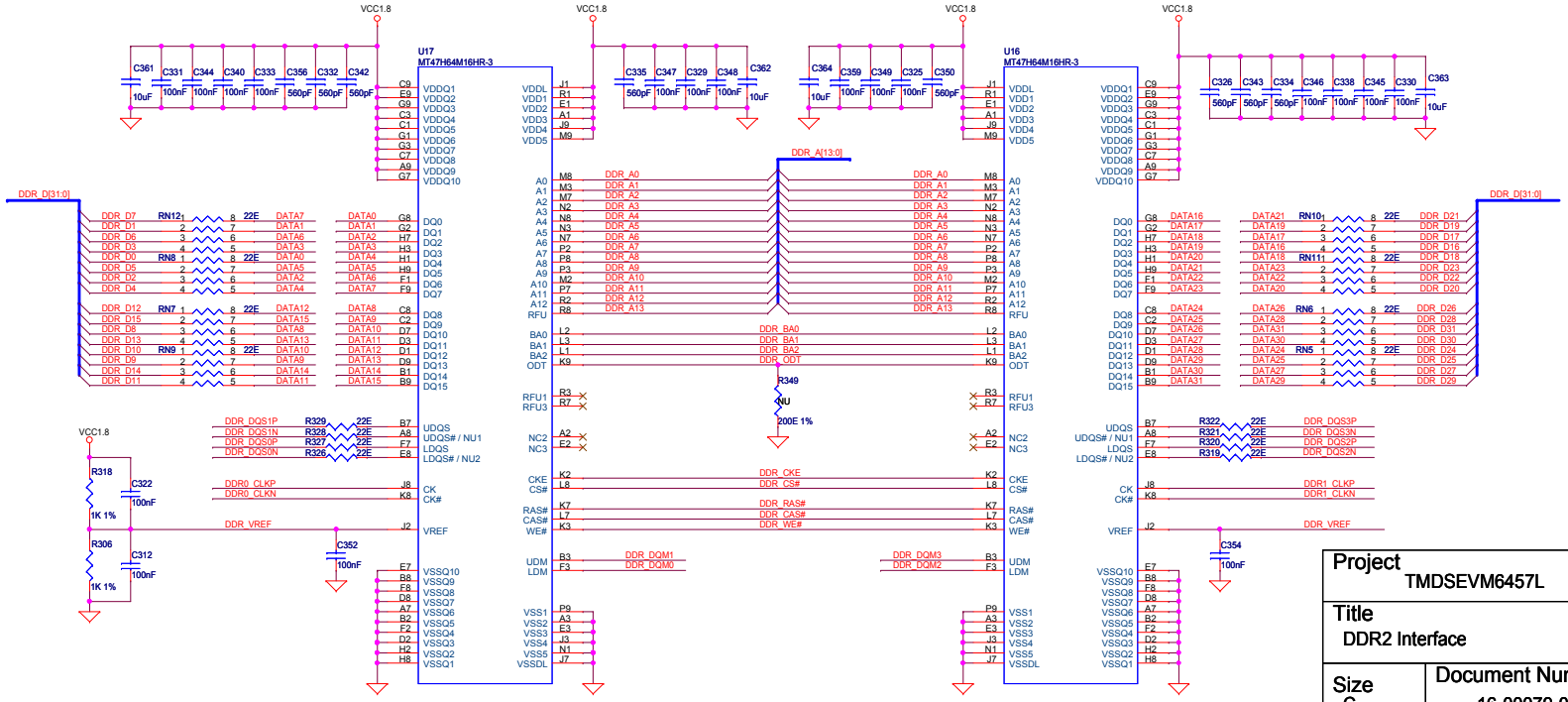


C6457 DDR2 Memory Controller

Supported Memories (84 FBGA) :

	256MB (128MB x 2)	512MB (256MB x 2)
Micron	MT47H64M16HR-3	MT47H128M16HG-3



128MB DDR2 Memory

128MB DDR2 Memory

256MB DDR2 Memory Interface

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Title: DDR2 Interface		
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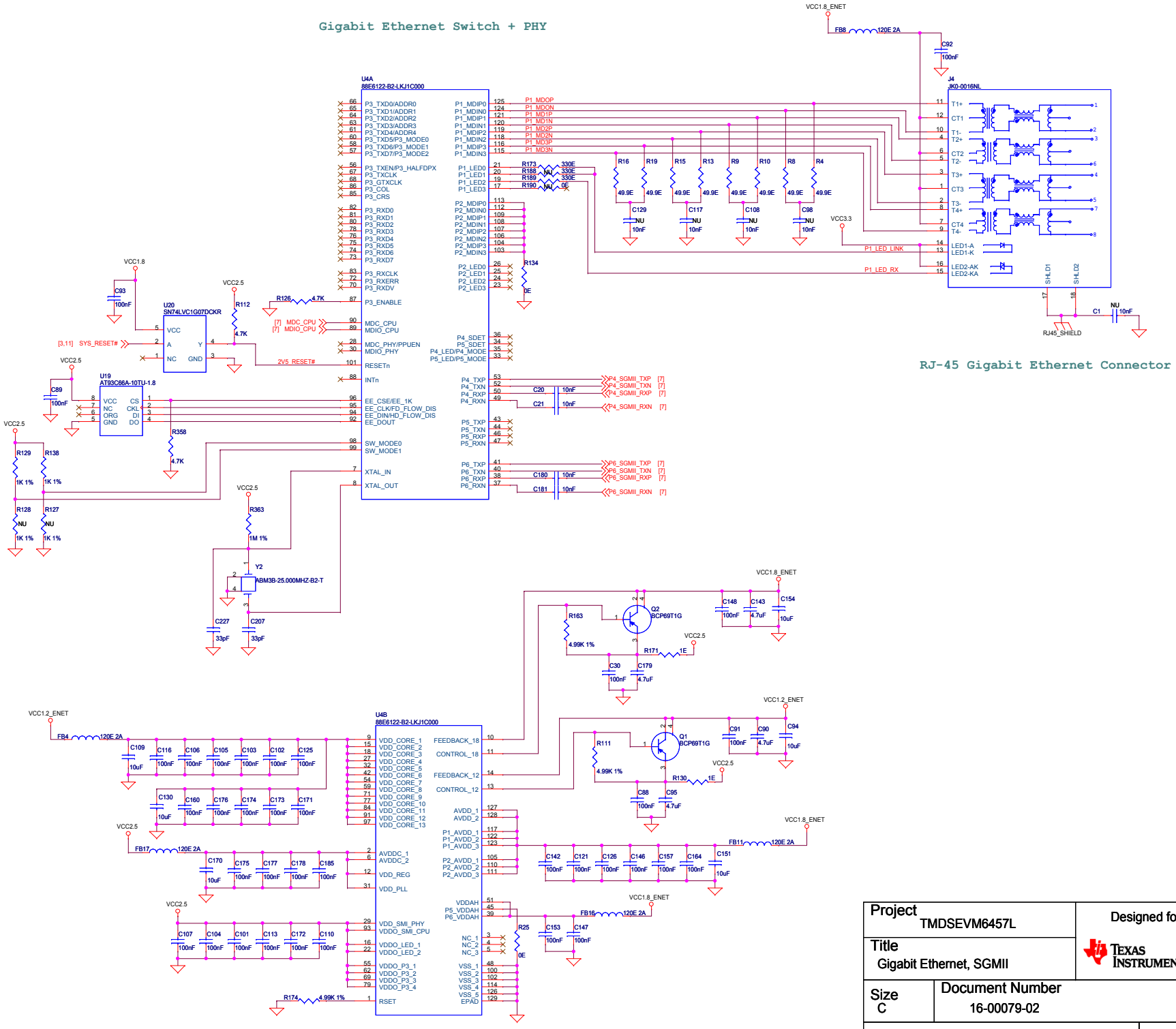
Gigabit Ethernet Switch + PHY



Project: TMDSEVM6457L	Designed for TI by eInfochips	
Title: Gigabit Ethernet, SGMII		
Size: C	Document Number: 16-00079-02	Rev: 2.0
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Power for MSP430

J8.2 to J8.1: MP3.3_AMC Power (Default)

J8.2 to J8.3: VCC3.3 Board Power (Factory Use)

J6 Open : Default

J6 Short: Factory Use

MMC for IPMI

JTAG for MSP430

C6457 SGMII / SRIO Interface

AMC Connector

Project: TMDSEVM6457L	Designed for TI by eInfochips	
Title: MMC, AMC Connector Interface		
Size: C	Document Number: 16-00079-02	Rev: 2.0
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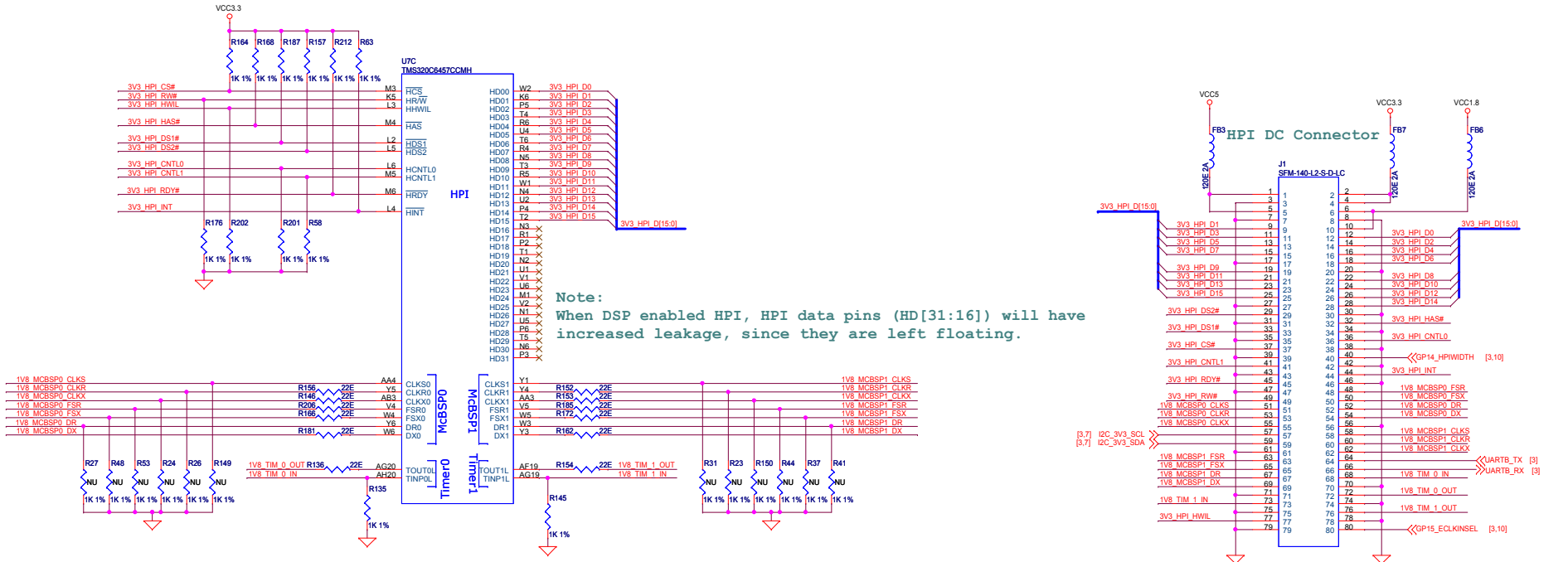

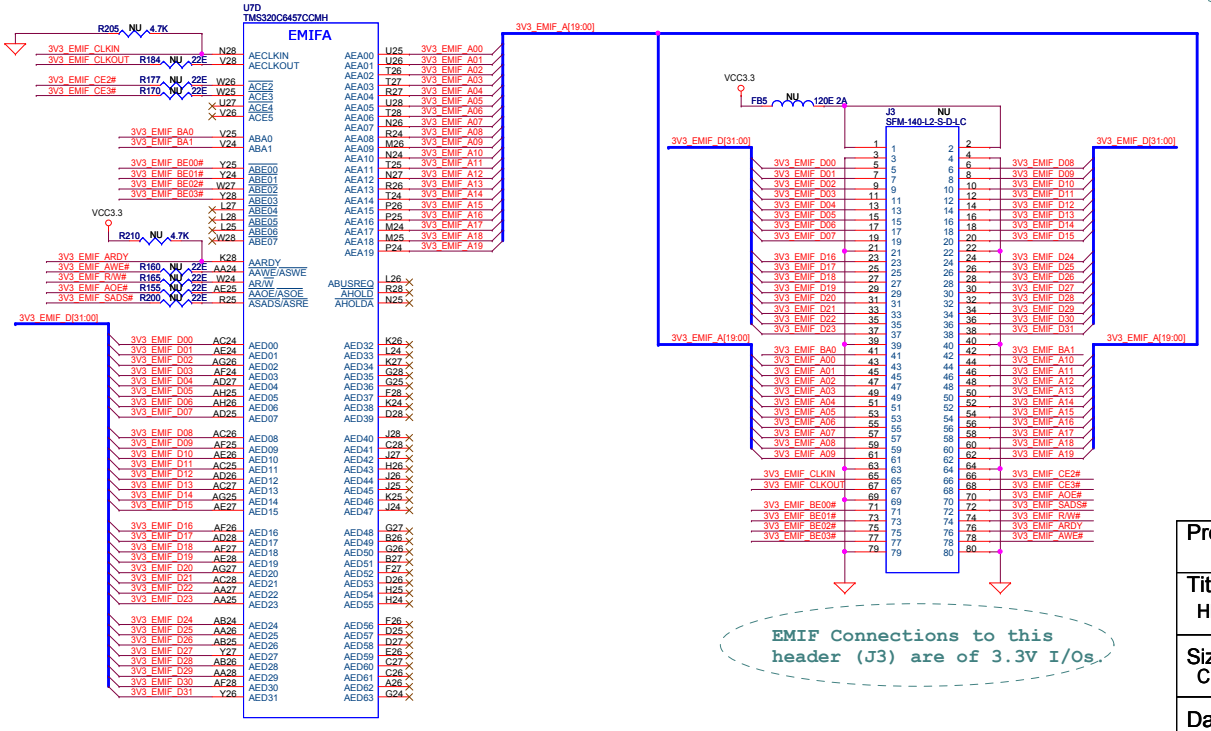

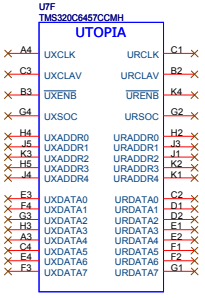

Project: TMDSEVM6457L	Designed for TI by eInfochips	
Title: HPI DC, EMIF Header		
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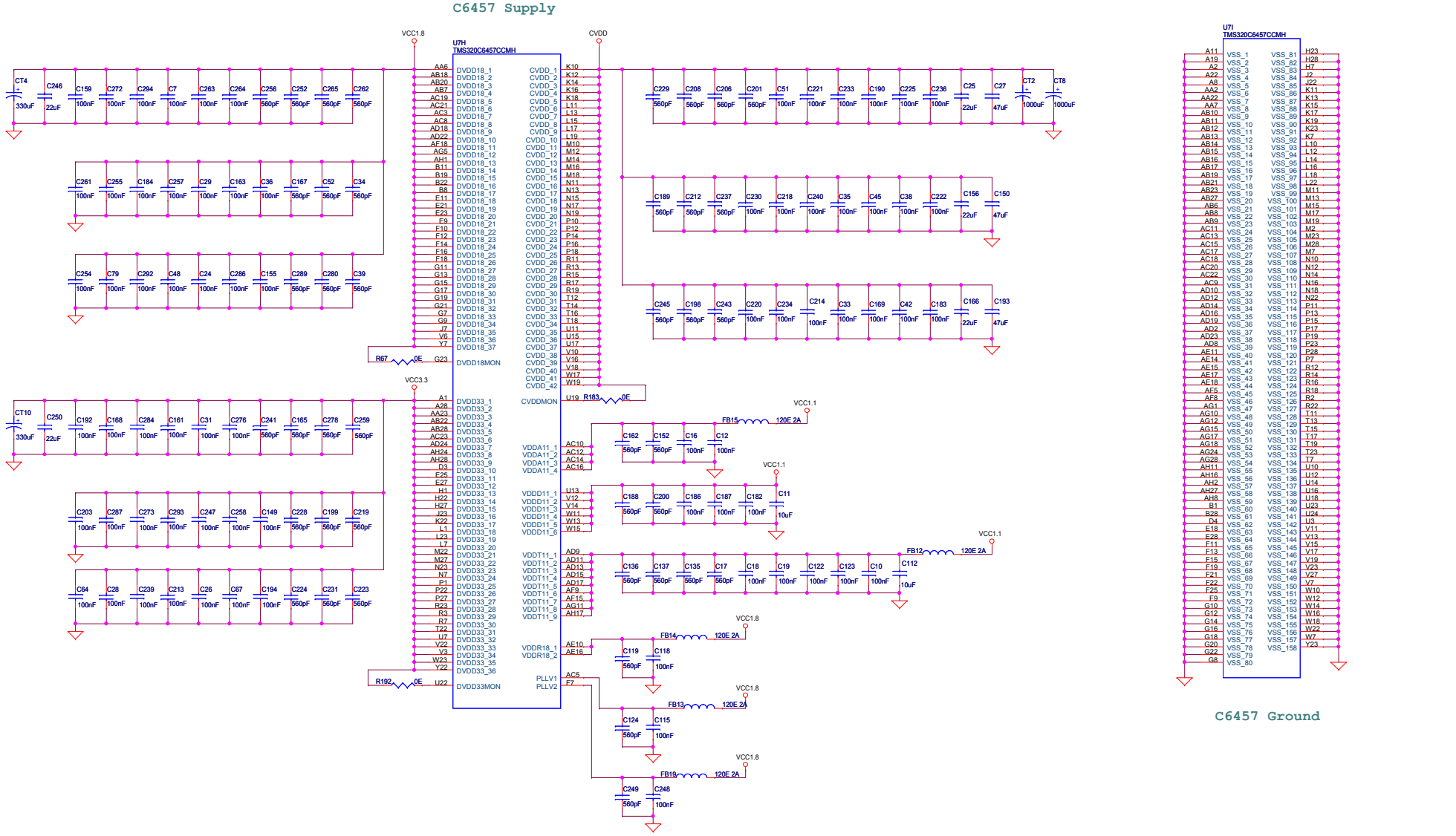

Project: TMDSEVM6457L	Designed for TI by eInfochips	
Title: DSP Power Supply		
Size: C	Document Number: 16-00079-02	Rev: 2.0
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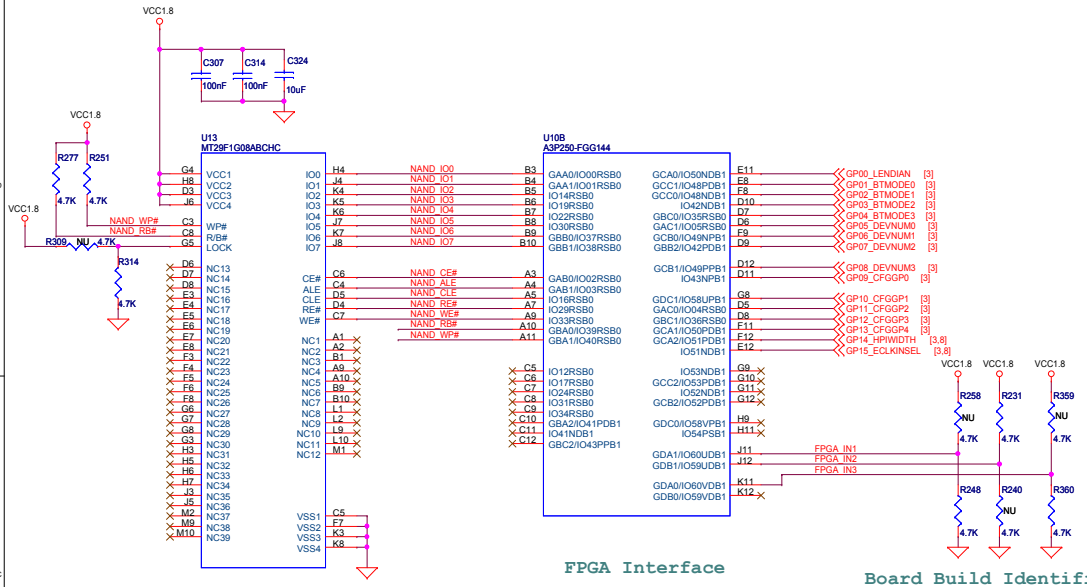
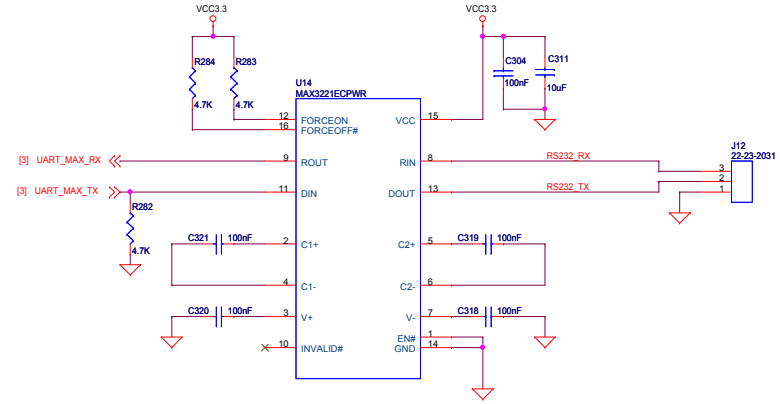


NAND Interface

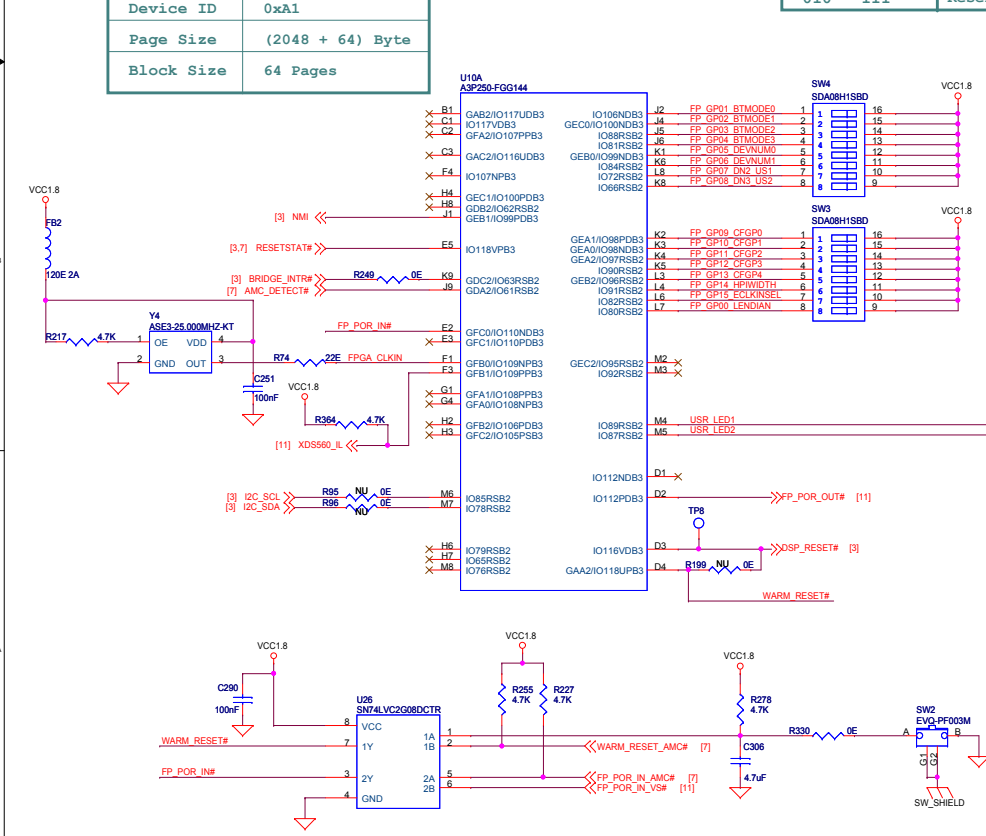
Size	128MB
Mfg ID	0x2C
Device ID	0xA1
Page Size	(2048 + 64) Byte
Block Size	64 Pages

FPGA Interface

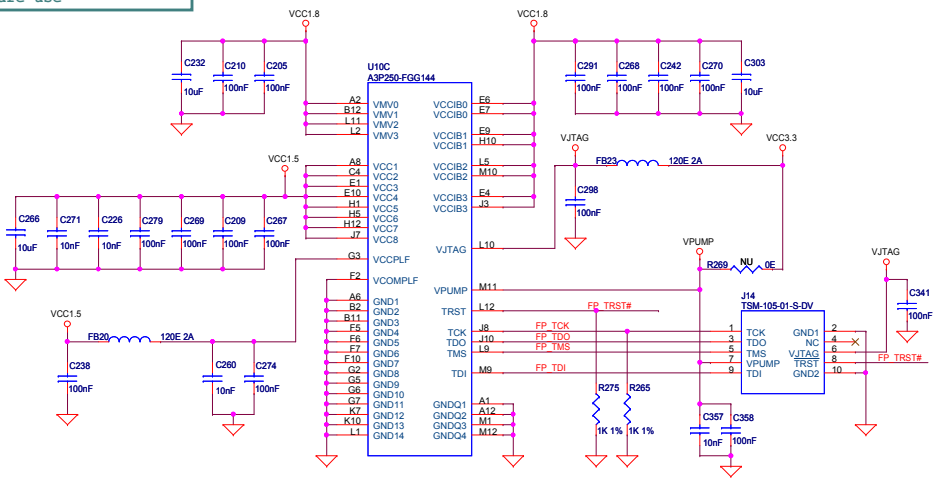


Board Build Identification

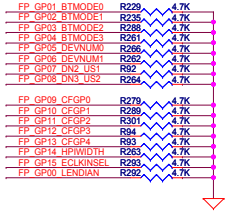
[K11:J12:J11]	Description
000	Proto Batch, PCB Rev 01
001	Pilot Batch, PCB Rev 01
010	Production Batch, PCB Rev 02
010 - 111	Reserved for future use



FPGA Power



FPGA JTAG Connector



Project TMDSEVM6457L		Designed for TI by eInfochips
Title FPGA - NAND Flash Interface		
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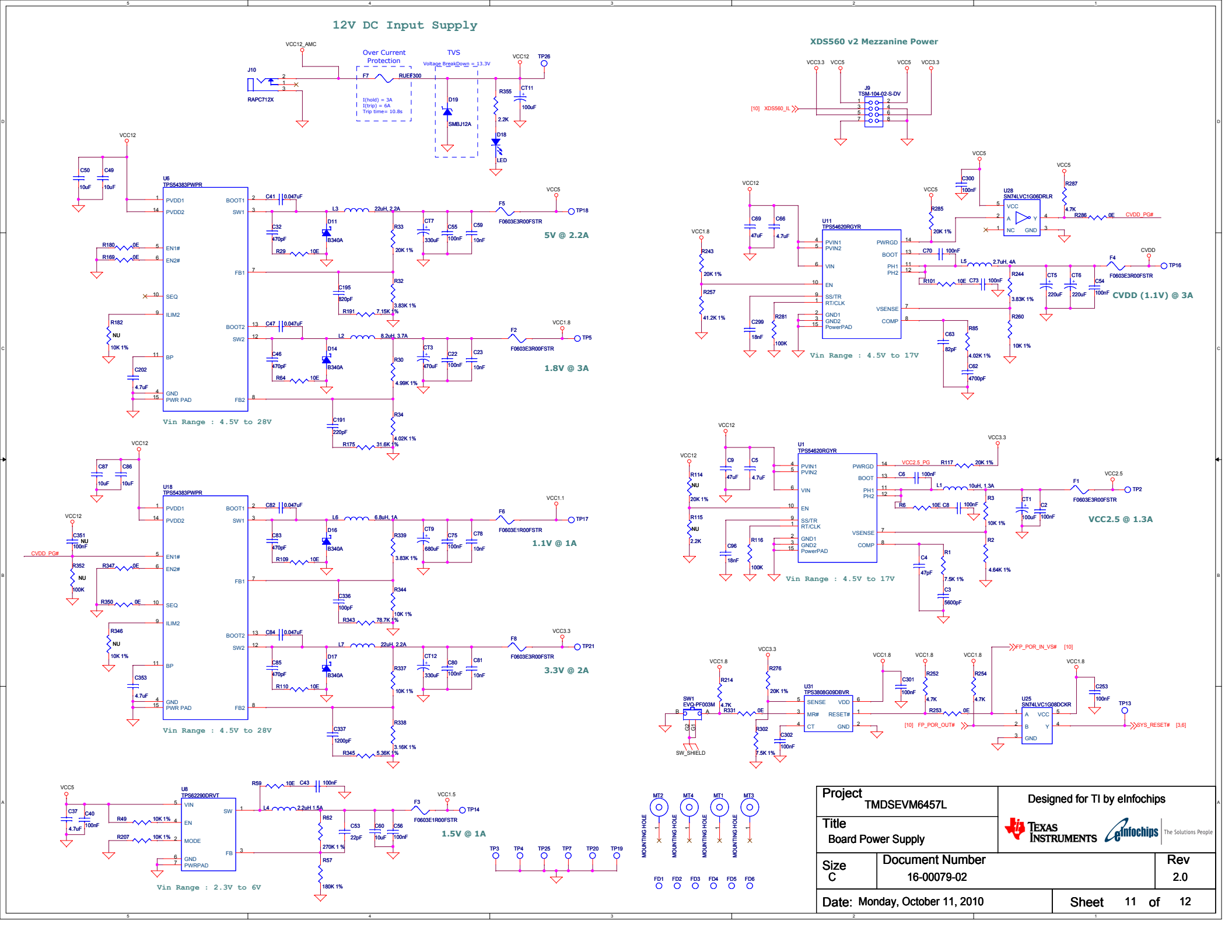

Project: TMDSEVM6457L	Designed for TI by eInfochips	
Title: Board Power Supply		
Size: C	Document Number: 16-00079-02	Rev: 2.0
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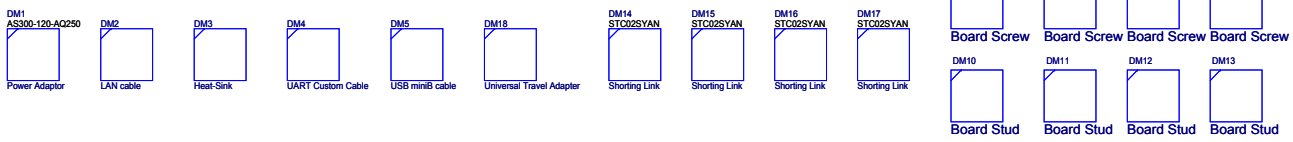
TMDSEVM6457L - REVISION HISTORY

PCB REV.	SCH. REV.	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	Issue 1.0	- Released for PCB fabrication -- Proto Boards	28JULY2010	eInfochips
	Issue 1.1	Pilot Batch Release - U32 part number changed to TXS0108EPWR - Board Identification # changed to 001 from 000 - R280 (4.7K) made NU, 4.7K PD added on EM_TRST#, 1K PD added on TRST# net - 1M bias resistor added on Y2.1 pin	17SEP2010	eInfochips
2.0	Issue 2.0	Production Batch Release - Pull up added on XDS560_IL net - AMC_DETECT# signal to FPGA taken from Level Translator chip U29 - CT11 part # changed - Board Identification # changed to 010	11OCT2010	eInfochips

Dummy Components



Project: TMDSEVM6457L		Designed for TI by eInfochips
Title: Revision History & Dummy Parts		
Size: C	Document Number: 16-00079-02	Rev: 2.0
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