

TMDSEVM6457L Schematic

SCHEMATIC PAGE DESCRIPTION :

- 01 : COVER SHEET
- 02 : SYSTEM BLOCK DIAGRAM
- 03 : DSP - CLOCK, CONFIGURATION, I2C-UART BRIDGE
- 04 : JTAG EMULATION (ON BOARD / EXTERNAL HEADER)
- 05 : DDR2 INTERFACE
- 06 : ETHERNET INTERFACE
- 07 : SRIO INTERFACE, MMC, AMC CONNECTOR
- 08 : HPI, EMIF INTERFACE
- 09 : DSP POWER
- 10 : FPGA - NAND FLASH INTERFACE
- 11 : BOARD POWER SUPPLY & RESET CIRCUITRY
- 12 : REVISION HISTORY & DUMMY PARTS

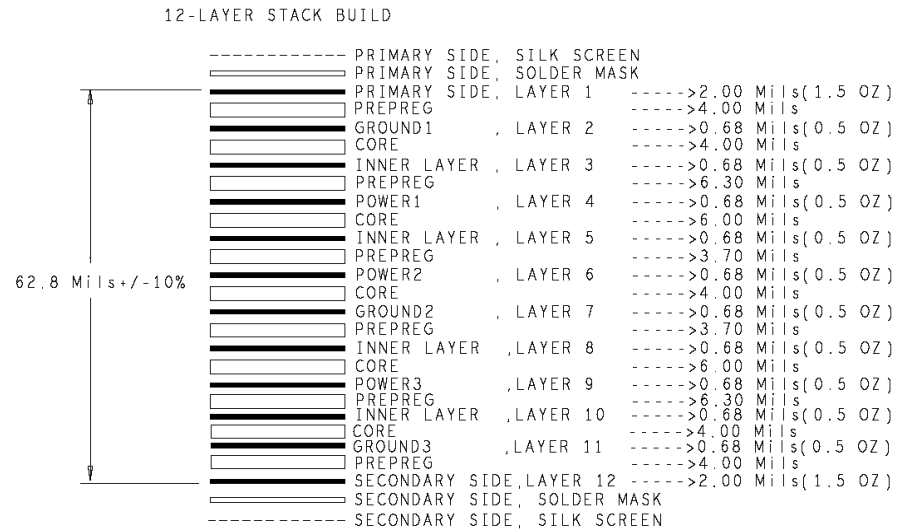
MAJOR REVISION HISTORY :

| PCB REV. | SCH. REV. | DESCRIPTION | DATE |
|----------|-----------|------------------|--------------|
| 1.0 | 1.0 | Proto Build | 28-JULY-2010 |
| | 1.1 | Pilot Batch | 17-SEP-2010 |
| 2.0 | 2.0 | Production Batch | 11-OCT-2010 |

I2C ADDRESS TABLE :

| REF DES | DESCRIPTION | 7 BIT ADDRESS |
|---------|-------------------|---------------|
| U22 | I2C EEPROM | 0x50, 0x51 |
| U23 | I2C - UART BRIDGE | 0x4D |
| | | |
| | | |

PCB LAYER STACK-UP DETAILS :



PCB Mechanical Details :

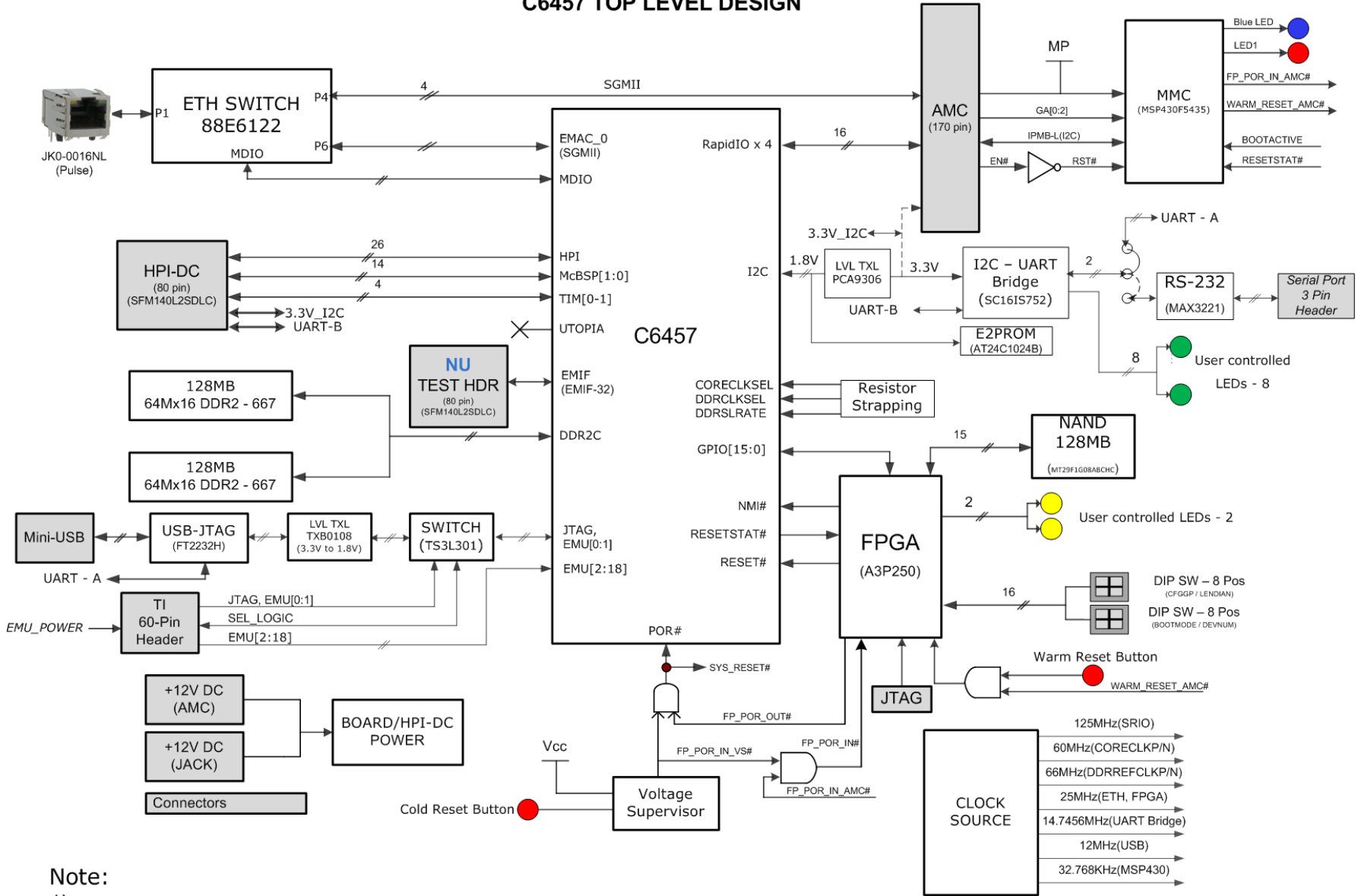
1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. PCB MATERIAL: FR4
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.

| | | | |
|--------------------------------|--------------------------------|-------------------------------|--|
| Project TMDSEVM6457L | | Designed for TI by eInfochips | |
| Title COVER SHEET | | | |
| Size C | Document Number 16-00079-02 | Rev 2.0 | |
| Date: Monday, October 11, 2010 | | Sheet 1 of 12 | |

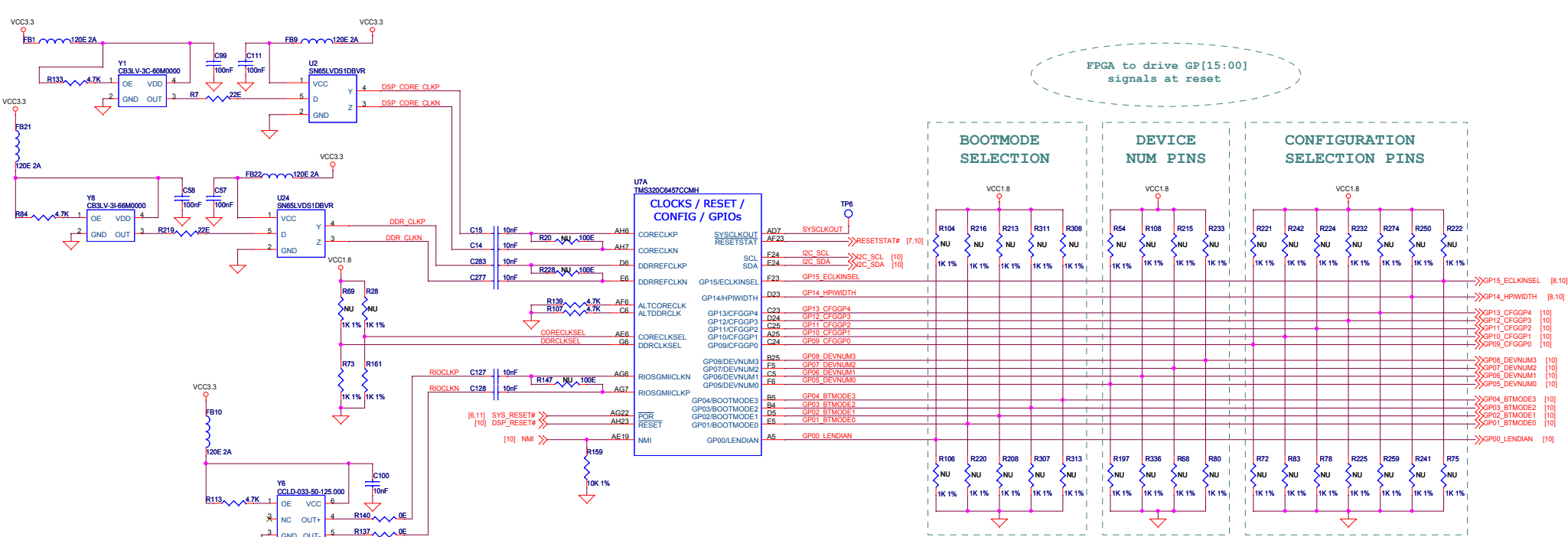
C6457 TOP LEVEL DESIGN



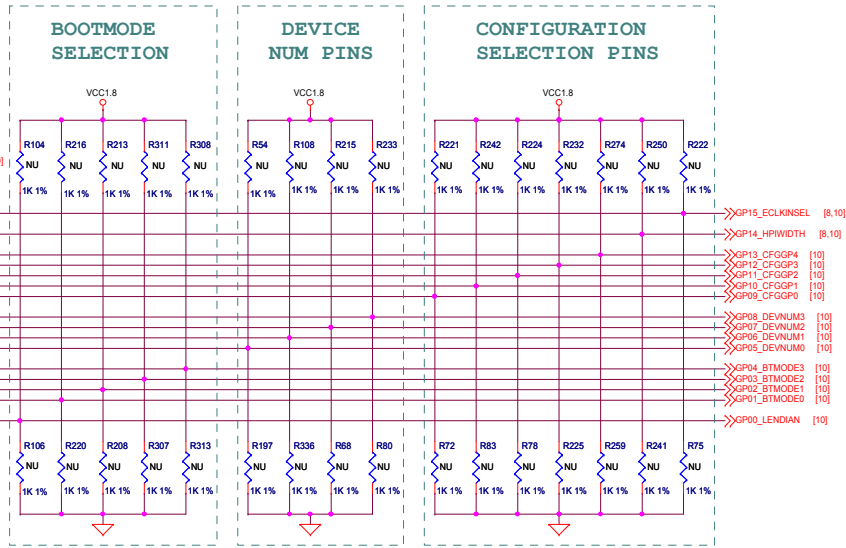
Note:

1) EMIF test header will not be populated on board.

| | | | |
|--------------------------------|--------------------------------|-------------------------------|--|
| Project TMDSEVM6457L | | Designed for TI by eInfochips | |
| Title System Block Diagram | | | |
| Size C | Document Number 16-00079-02 | Rev 2.0 | |
| Date: Monday, October 11, 2010 | | Sheet 2 of 12 | |

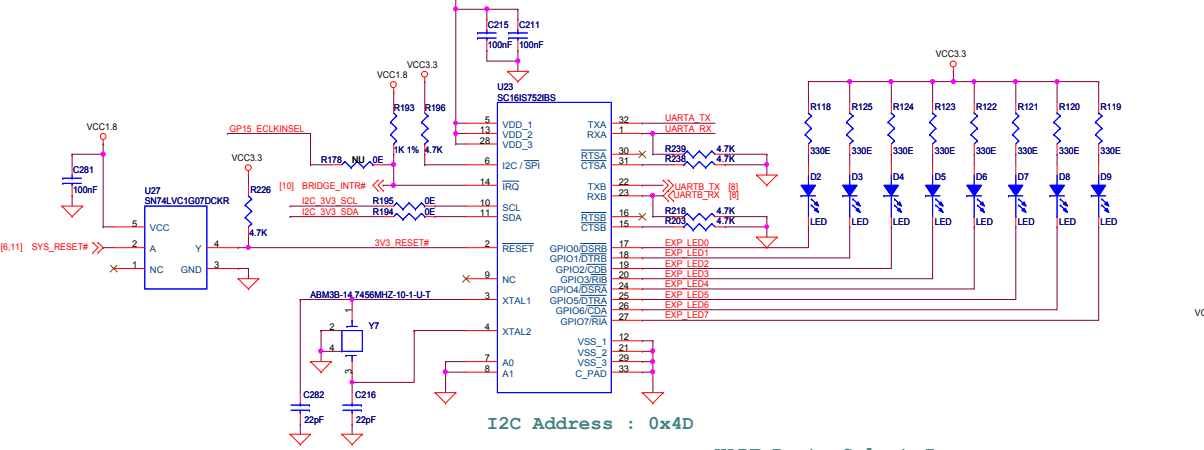


FPGA to drive GP[15:00] signals at reset

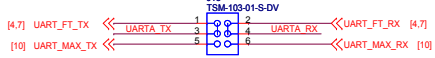


| BOOTMODE [3:0] | DESCRIPTION |
|-----------------------|--|
| 0000 (0) | No boot |
| 0001 (1) | I2C Master boot (address : 50H) -- Default |
| 0010 (2) | I2C Master boot (address : 51H) |
| 0011 (3) | I2C Slave boot |
| 0100 (4) | Host (HPI) boot |
| 0101 (5) | EMIFA boot |
| 0110 (6) - 1000 (8) | EMAC boot |
| 1001 (9) | Reserved |
| 1010 (10) - 1101 (13) | RIO (Config[0:3]) boot |

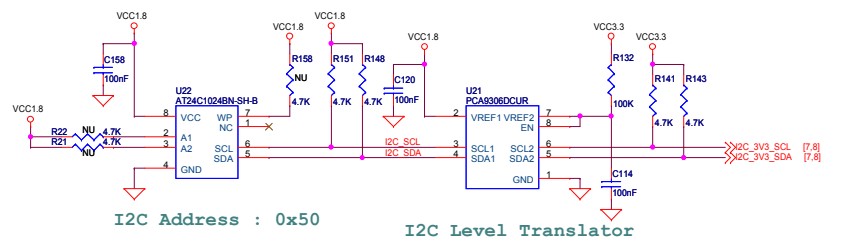
I2C - UART Bridge



I2C Address : 0x4D
UART Route Select Jumpers

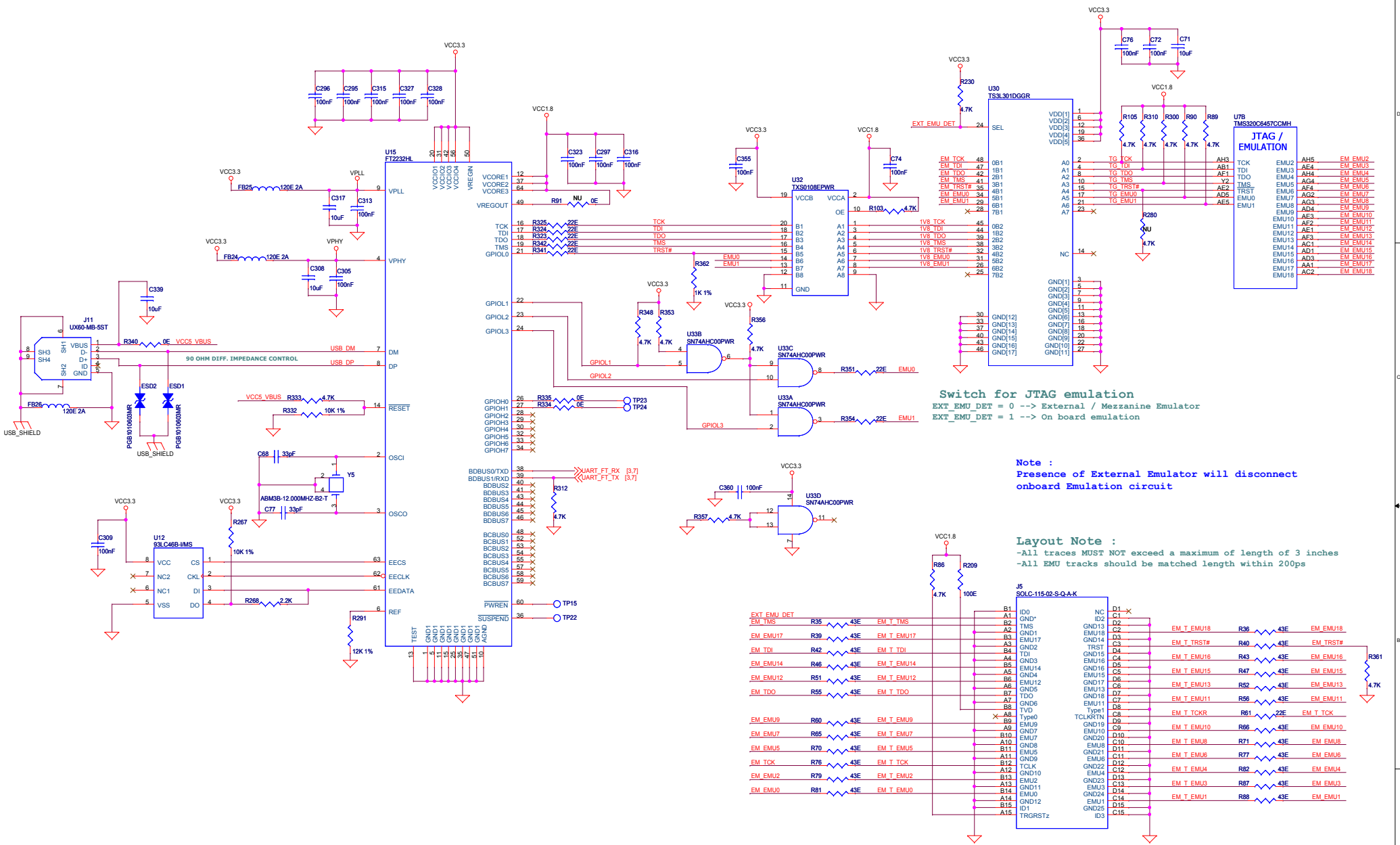


J13.3 to J13.1 & J13.4 to J13.2: UART over USB Connector (Default)
J13.3 to J13.5 & J13.4 to J13.6: UART over 3-Pin Header J12



I2C Address : 0x50
I2C Level Translator

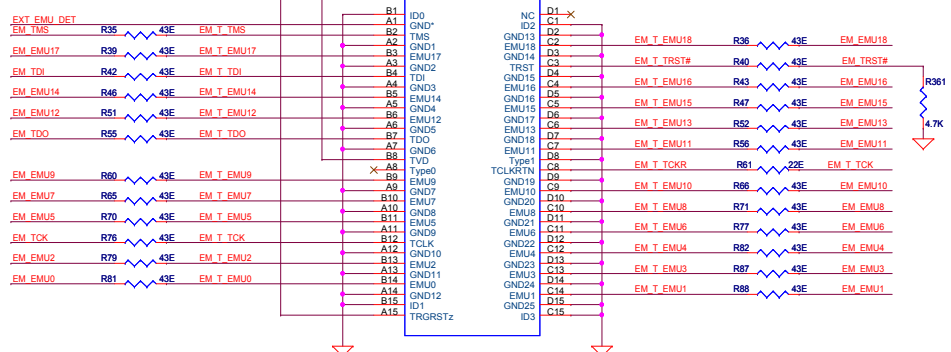
| | | | |
|---|--------------------------------|-------------------------------|--|
| Project TMDSEVM6457L | | Designed for TI by elnfochips | |
| Title DSP Configuration, UART Bridge | | | |
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Switch for JTAG emulation
 EXT_EMU_DET = 0 --> External / Mezzanine Emulator
 EXT_EMU_DET = 1 --> On board emulation

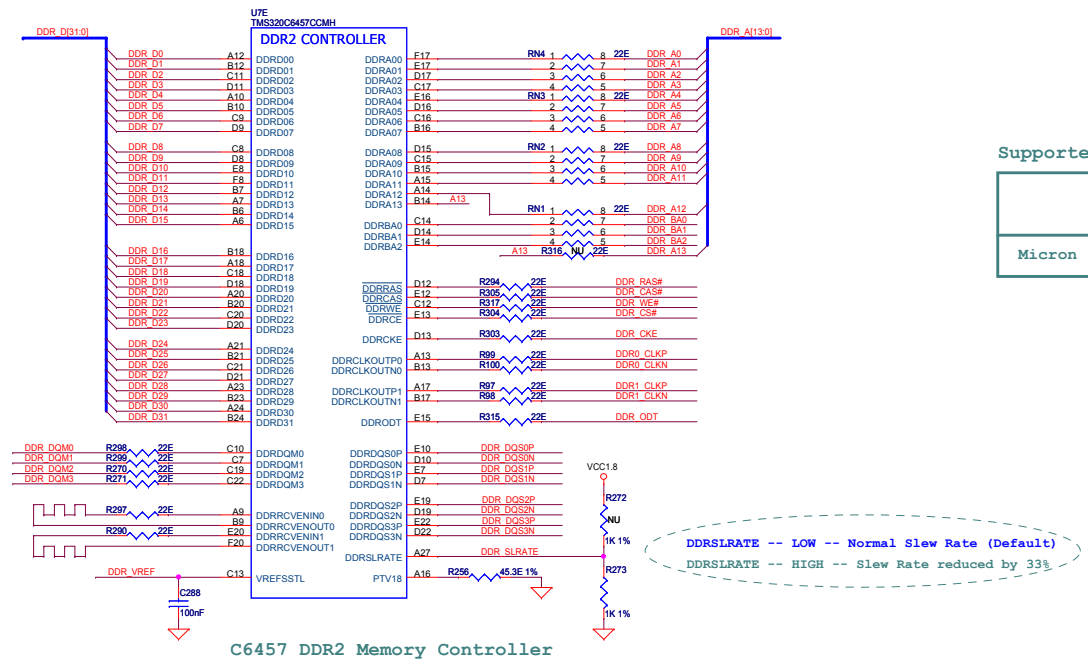
Note :
 Presence of External Emulator will disconnect onboard Emulation circuit

Layout Note :
 -All traces MUST NOT exceed a maximum of length of 3 inches
 -All EMU tracks should be matched length within 200ps

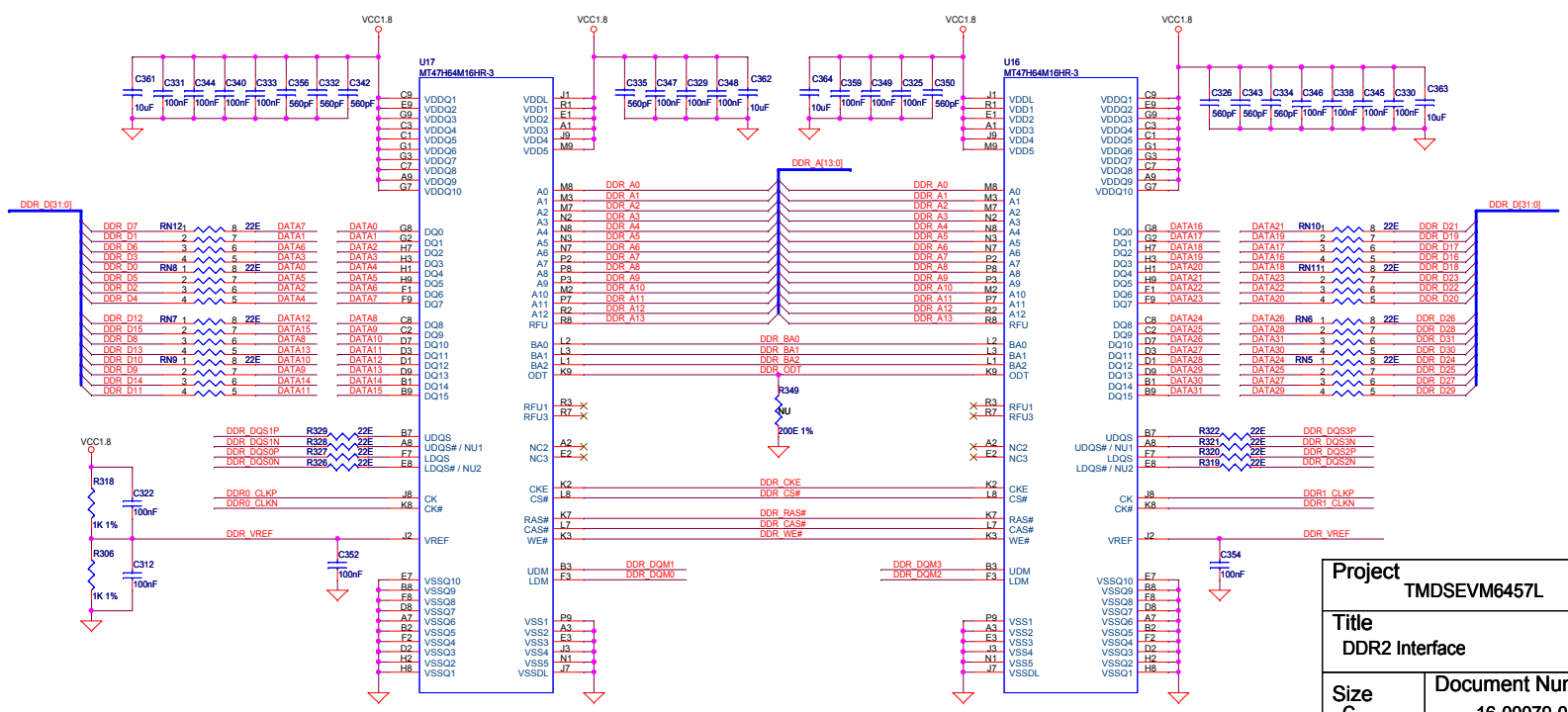


TI-60 Pin JTAG Connector for External/Mezzanine Emulator

| | | | |
|--------------------------------|--------------------------------|------------------------------|--|
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| Title JTAG Emulation | | | |
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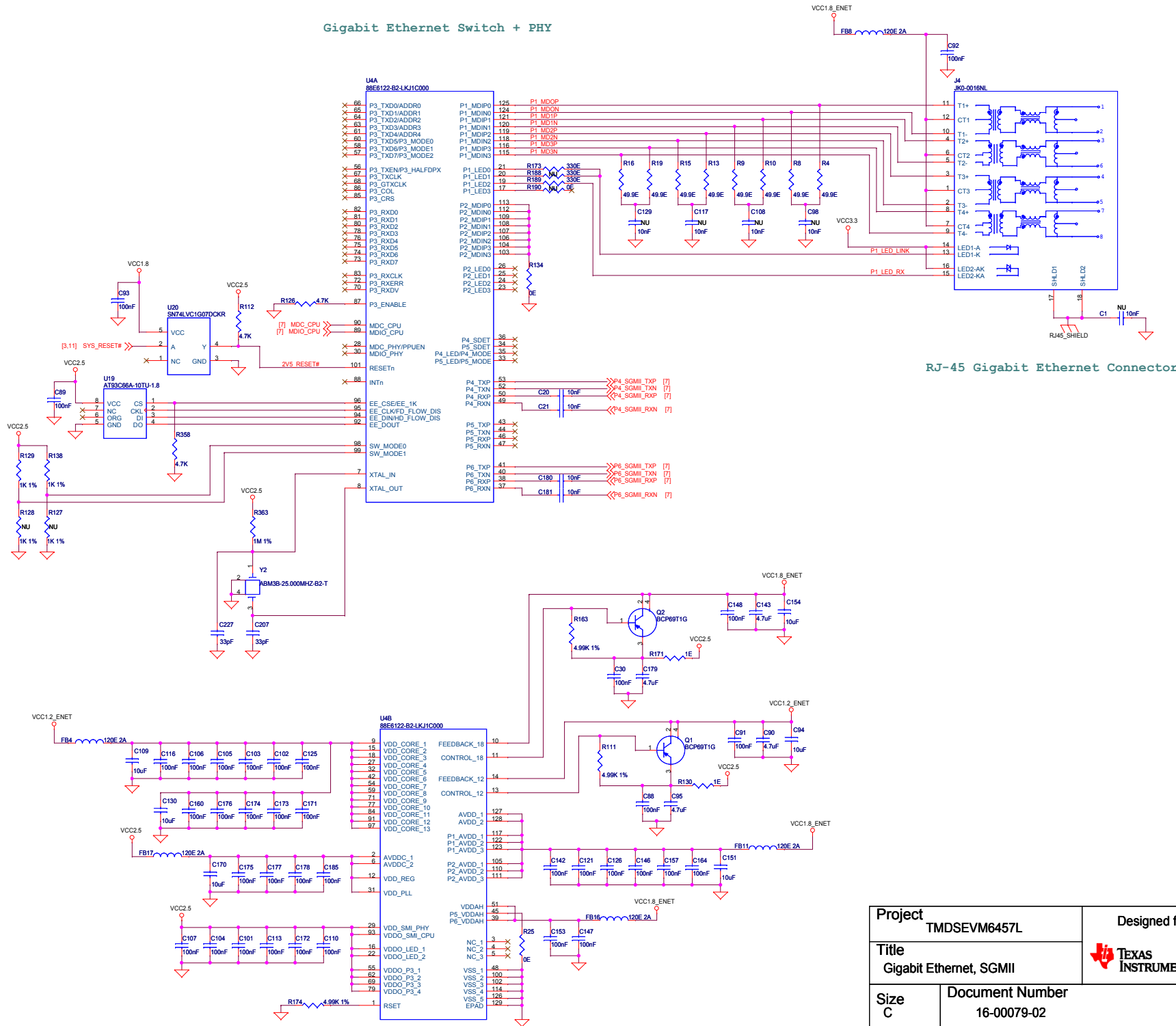


C6457 DDR2 Memory Controller



| | | | |
|--------------------------------|---------------------------------------|-------------------------------|--|
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| Title DDR2 Interface | | | |
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| Date: Monday, October 11, 2010 | | Sheet 5 of 12 | |

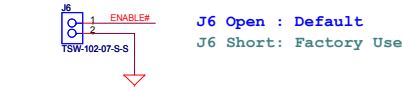
Gigabit Ethernet Switch + PHY



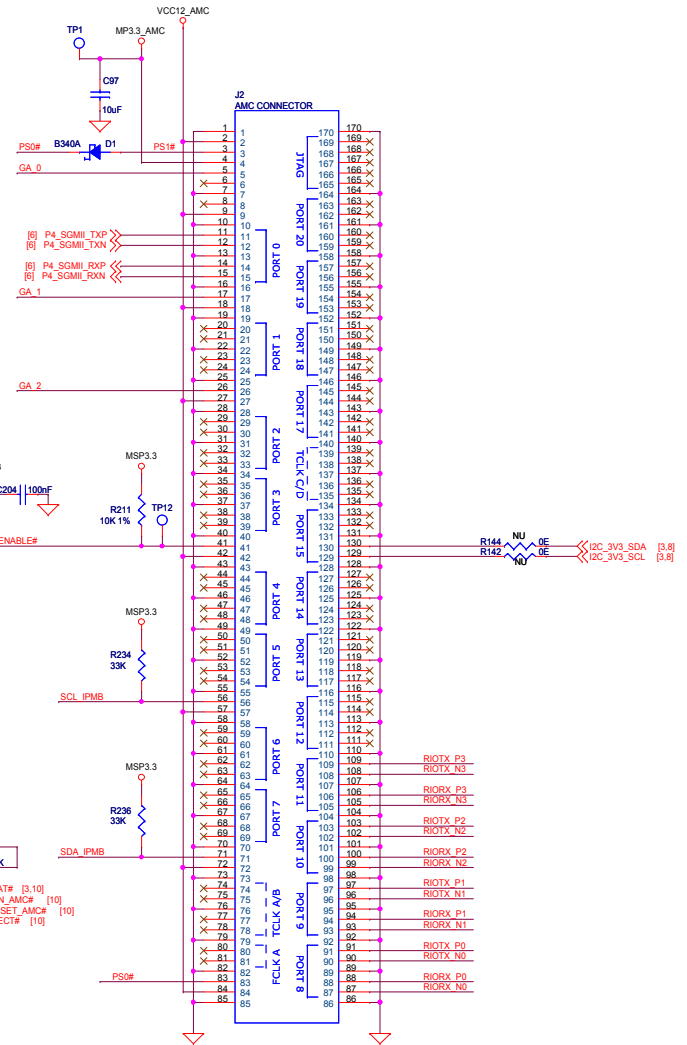
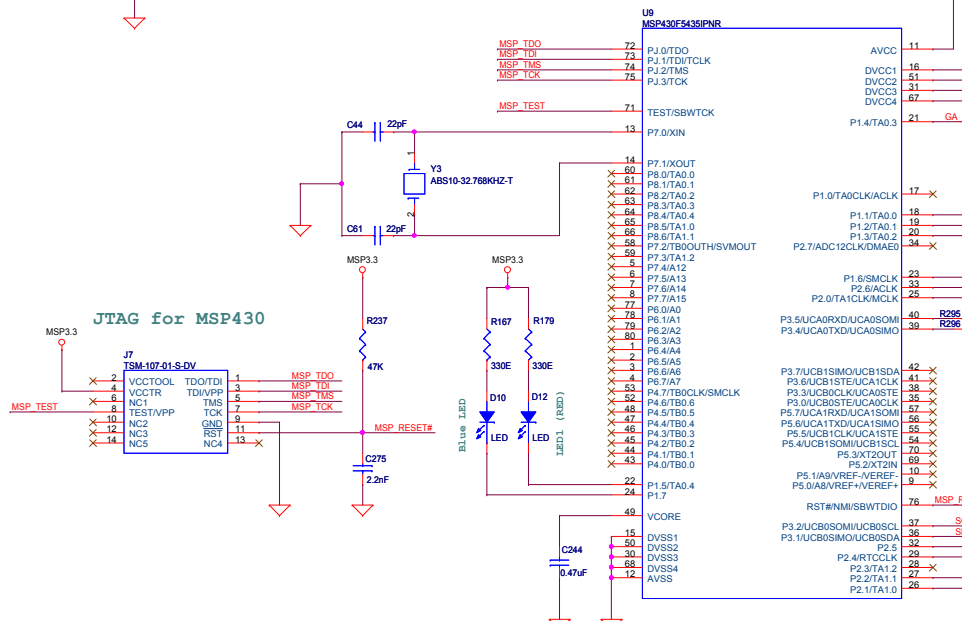
RJ-45 Gigabit Ethernet Connector

| | | | |
|----------------------------------|--------------------------------|-------------------------------|--|
| Project TMDSEVM6457L | | Designed for TI by eInfochips | |
| Title Gigabit Ethernet, SGMII | | | |
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| Date: Monday, October 11, 2010 | | Sheet 6 of 12 | |

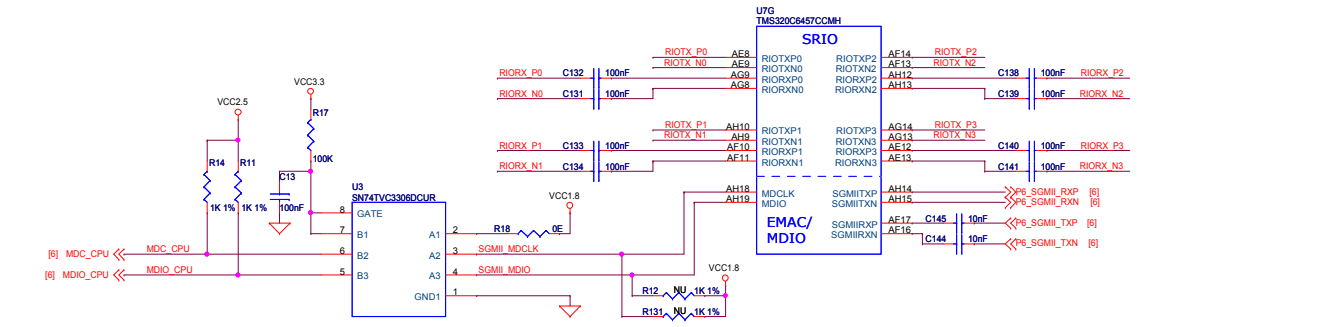
Power for MSP430
J8.2 to J8.1: MP3.3 AMC Power (Default)
J8.2 to J8.3: VCC3.3 Board Power (Factory Use)



MMC for IPMI

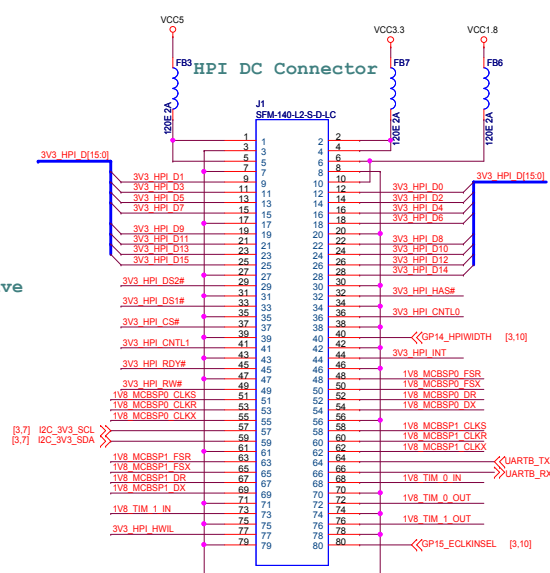
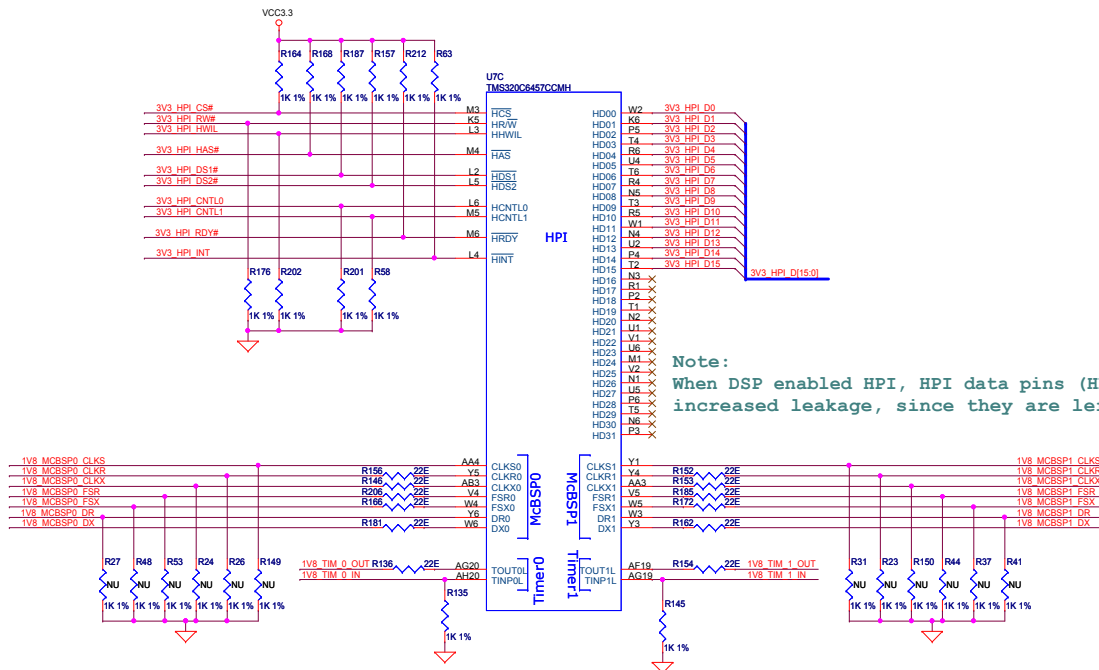


C6457 SGMII / SRIIO Interface

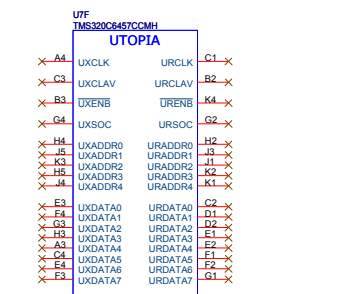
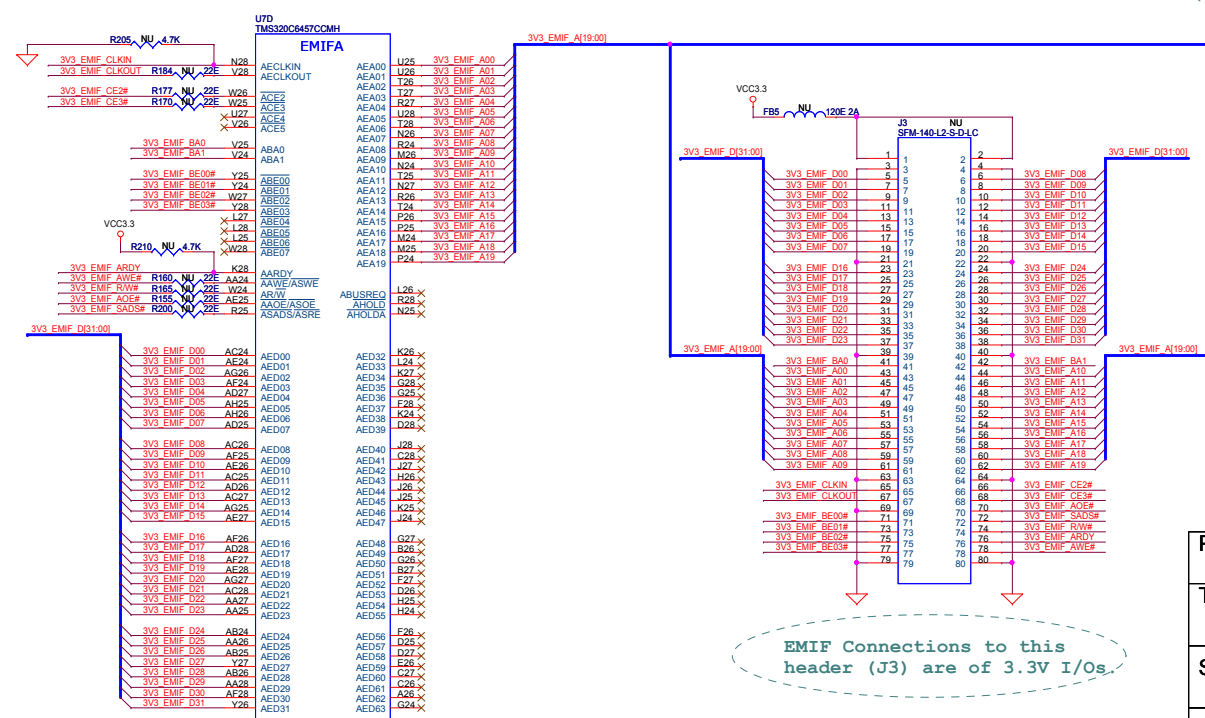


AMC Connector

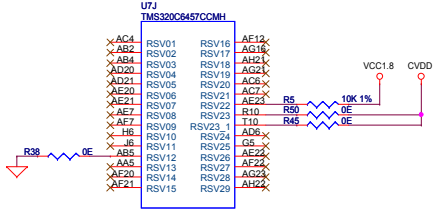
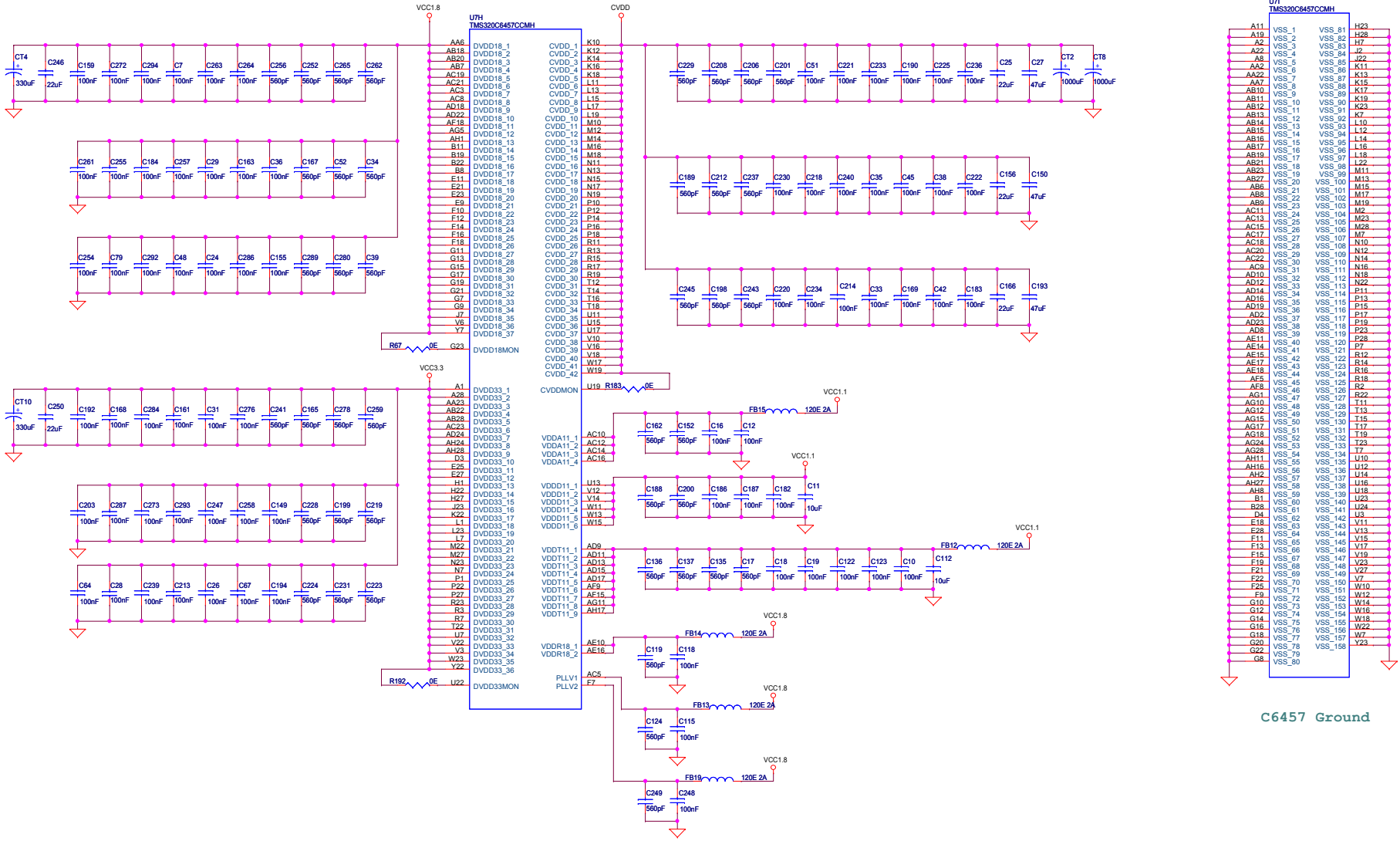
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| Project TMDSEVM6457L | | Designed for TI by elnfochips | |
| Title MMC, AMC Connector Interface | | <small>The Solutions People</small> | |
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| Date: Monday, October 11, 2010 | | Sheet 7 of 12 | |



- HPI, I2C and UART Connections to this header (J1) are of 3.3V I/Os.
- McBSP, Timers and GPIO connections to this header (J1) are of 1.8V I/Os.



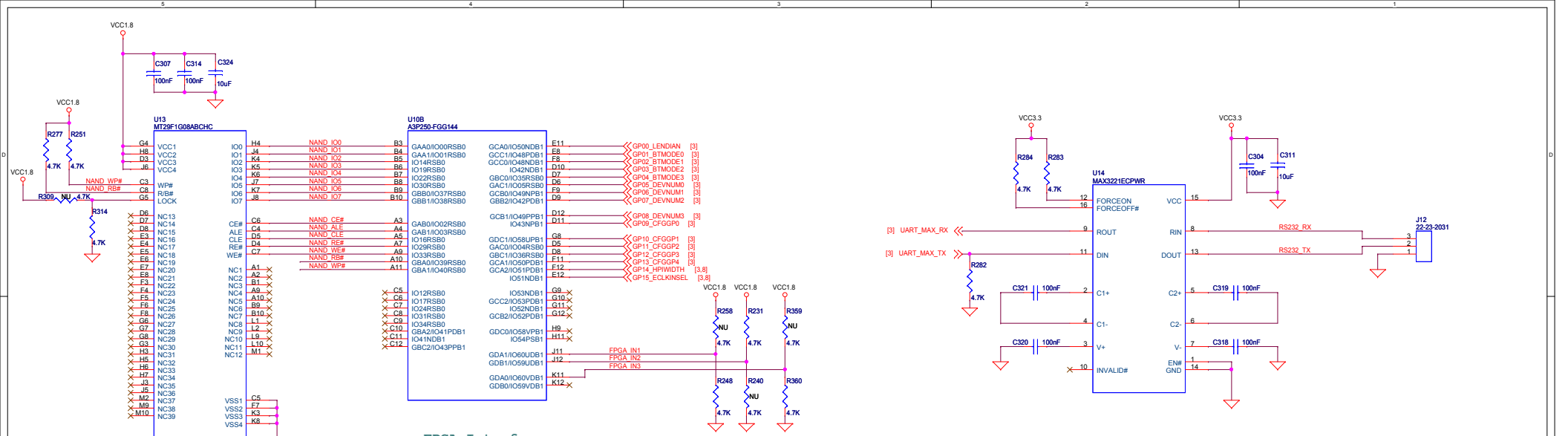
C6457 Supply



| U7J | | TMS320C6457CCMH | |
|------|--------|-----------------|-----|
| A11 | VSS_1 | VSS_81 | H23 |
| A19 | VSS_2 | VSS_82 | H28 |
| A2 | VSS_3 | VSS_83 | H7 |
| A22 | VSS_4 | VSS_84 | J22 |
| AA6 | VSS_5 | VSS_85 | K17 |
| AA2 | VSS_6 | VSS_86 | K11 |
| AA22 | VSS_7 | VSS_87 | K15 |
| AA7 | VSS_8 | VSS_88 | K17 |
| AA10 | VSS_9 | VSS_89 | K17 |
| AB11 | VSS_10 | VSS_90 | K17 |
| AB12 | VSS_11 | VSS_91 | K23 |
| AB13 | VSS_12 | VSS_92 | K7 |
| AB14 | VSS_13 | VSS_93 | L10 |
| AB15 | VSS_14 | VSS_94 | L12 |
| AB16 | VSS_15 | VSS_95 | L14 |
| AB17 | VSS_16 | VSS_96 | L16 |
| AB18 | VSS_17 | VSS_97 | L22 |
| AB19 | VSS_18 | VSS_98 | L18 |
| AB20 | VSS_19 | VSS_99 | M11 |
| AB21 | VSS_20 | VSS_100 | M11 |
| AB22 | VSS_21 | VSS_101 | M13 |
| AB23 | VSS_22 | VSS_102 | M15 |
| AB24 | VSS_23 | VSS_103 | M17 |
| AB25 | VSS_24 | VSS_104 | M19 |
| AB26 | VSS_25 | VSS_105 | M23 |
| AB27 | VSS_26 | VSS_106 | M28 |
| AB28 | VSS_27 | VSS_107 | M10 |
| AB29 | VSS_28 | VSS_108 | N12 |
| AB30 | VSS_29 | VSS_109 | N12 |
| AB31 | VSS_30 | VSS_110 | N14 |
| AB32 | VSS_31 | VSS_111 | N16 |
| AB33 | VSS_32 | VSS_112 | N18 |
| AB34 | VSS_33 | VSS_113 | N22 |
| AB35 | VSS_34 | VSS_114 | P11 |
| AB36 | VSS_35 | VSS_115 | P13 |
| AB37 | VSS_36 | VSS_116 | P15 |
| AB38 | VSS_37 | VSS_117 | P17 |
| AB39 | VSS_38 | VSS_118 | P23 |
| AB40 | VSS_39 | VSS_119 | P28 |
| AB41 | VSS_40 | VSS_120 | P28 |
| AB42 | VSS_41 | VSS_121 | P7 |
| AB43 | VSS_42 | VSS_122 | R12 |
| AB44 | VSS_43 | VSS_123 | R14 |
| AB45 | VSS_44 | VSS_124 | R18 |
| AB46 | VSS_45 | VSS_125 | R2 |
| AB47 | VSS_46 | VSS_126 | R2 |
| AB48 | VSS_47 | VSS_127 | R22 |
| AB49 | VSS_48 | VSS_128 | R22 |
| AB50 | VSS_49 | VSS_129 | R22 |
| AB51 | VSS_50 | VSS_130 | R22 |
| AB52 | VSS_51 | VSS_131 | R22 |
| AB53 | VSS_52 | VSS_132 | R22 |
| AB54 | VSS_53 | VSS_133 | R22 |
| AB55 | VSS_54 | VSS_134 | R22 |
| AB56 | VSS_55 | VSS_135 | R22 |
| AB57 | VSS_56 | VSS_136 | R22 |
| AB58 | VSS_57 | VSS_137 | R22 |
| AB59 | VSS_58 | VSS_138 | R22 |
| AB60 | VSS_59 | VSS_139 | R22 |
| AB61 | VSS_60 | VSS_140 | R22 |
| AB62 | VSS_61 | VSS_141 | R22 |
| AB63 | VSS_62 | VSS_142 | R22 |
| AB64 | VSS_63 | VSS_143 | R22 |
| AB65 | VSS_64 | VSS_144 | R22 |
| AB66 | VSS_65 | VSS_145 | R22 |
| AB67 | VSS_66 | VSS_146 | R22 |
| AB68 | VSS_67 | VSS_147 | R22 |
| AB69 | VSS_68 | VSS_148 | R22 |
| AB70 | VSS_69 | VSS_149 | R22 |
| AB71 | VSS_70 | VSS_150 | R22 |
| AB72 | VSS_71 | VSS_151 | R22 |
| AB73 | VSS_72 | VSS_152 | R22 |
| AB74 | VSS_73 | VSS_153 | R22 |
| AB75 | VSS_74 | VSS_154 | R22 |
| AB76 | VSS_75 | VSS_155 | R22 |
| AB77 | VSS_76 | VSS_156 | R22 |
| AB78 | VSS_77 | VSS_157 | R22 |
| AB79 | VSS_78 | VSS_158 | R22 |
| AB80 | VSS_79 | VSS_159 | R22 |
| AB81 | VSS_80 | VSS_160 | R22 |

C6457 Ground

| | | | |
|--------------------------------|--------------------------------|------------------------------|--|
| Project TMDSEVM6457L | | Designed for TI by elfnchips | |
| Title DSP Power Supply | | | |
| Size C | Document Number 16-00079-02 | Rev 2.0 | |
| Date: Monday, October 11, 2010 | | Sheet 9 of 12 | |



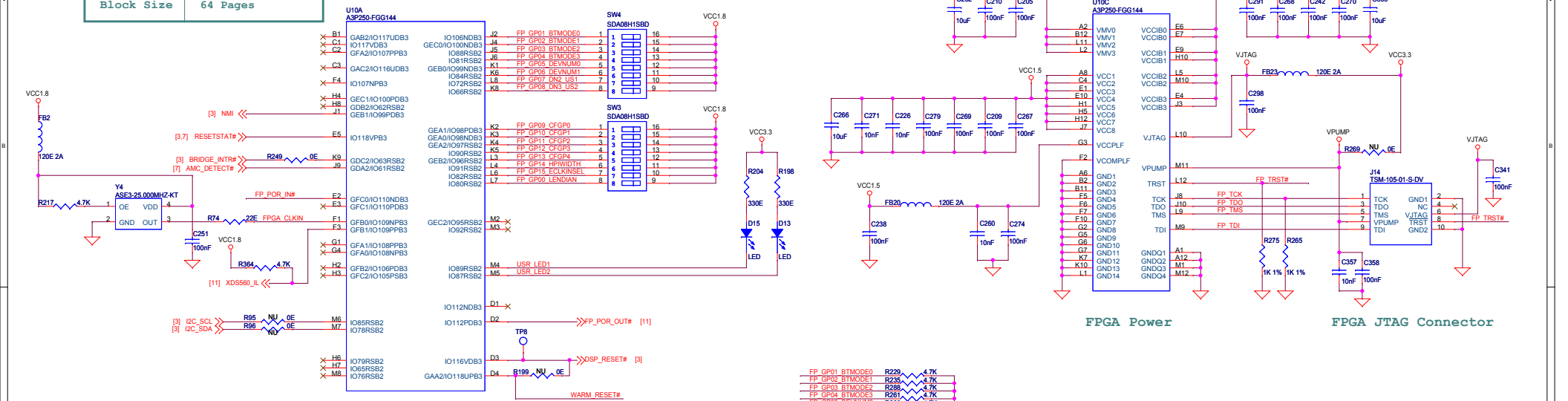
FPGA Interface

Board Build Identification

NAND Interface

| | |
|------------|------------------|
| Size | 128MB |
| Mfg ID | 0x2C |
| Device ID | 0xA1 |
| Page Size | (2048 + 64) Byte |
| Block Size | 64 Pages |

| [K11:J12:J11] | Description |
|---------------|------------------------------|
| 000 | Proto Batch, PCB Rev 01 |
| 001 | Pilot Batch, PCB Rev 01 |
| 010 | Production Batch, PCB Rev 02 |
| 010 - 111 | Reserved for future use |



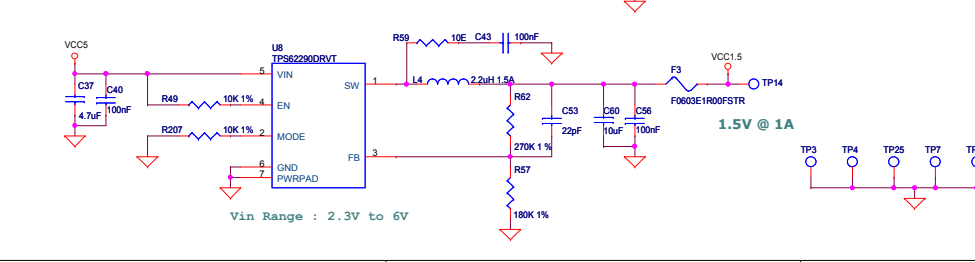
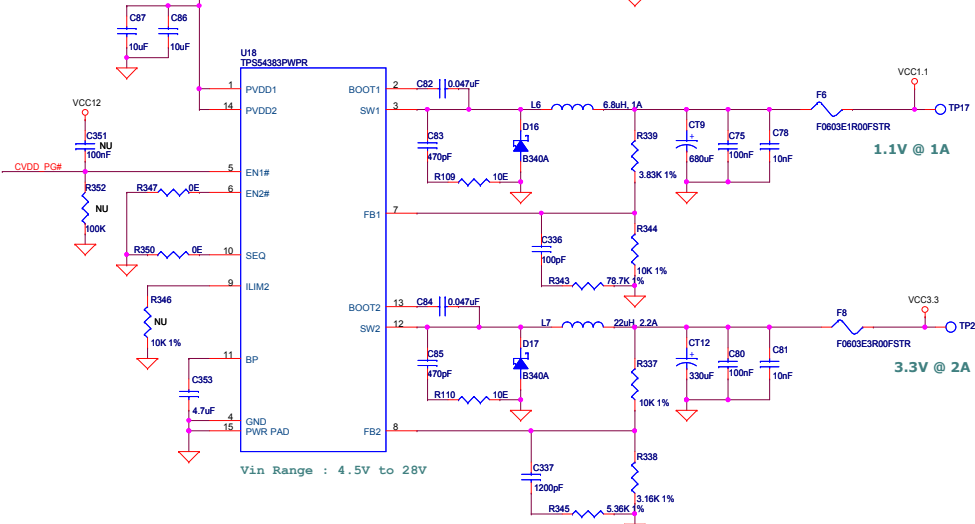
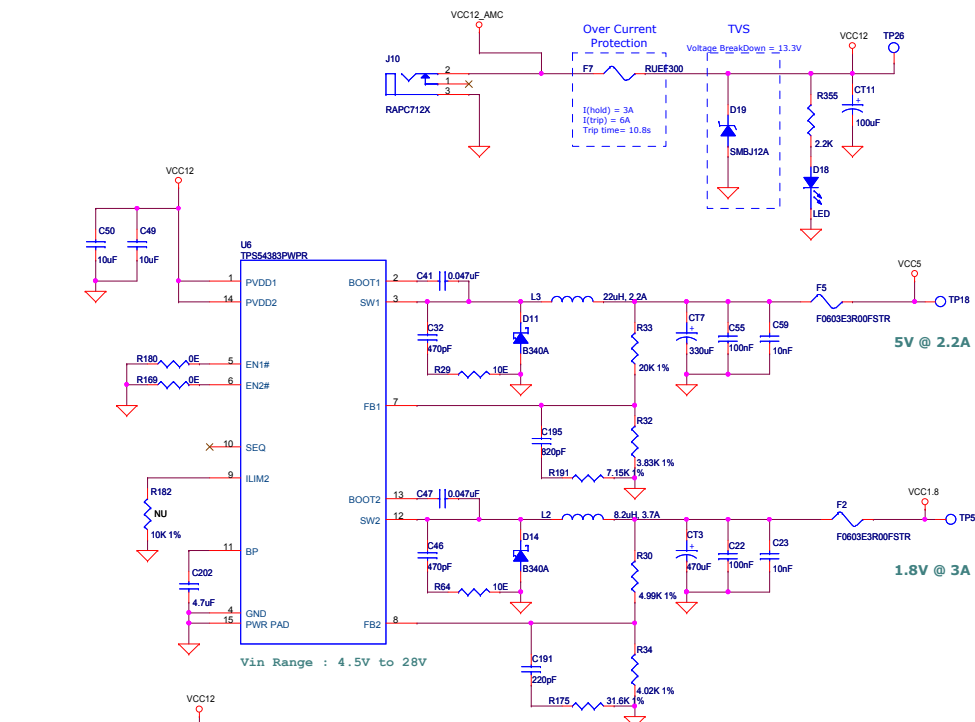
FPGA Power

FPGA JTAG Connector

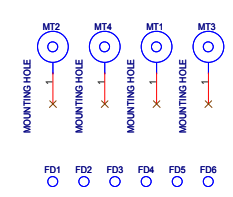
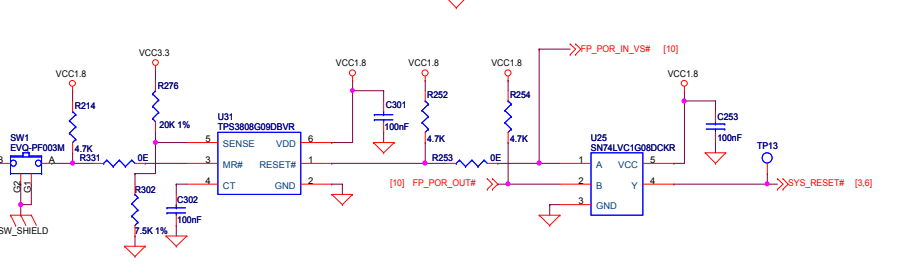
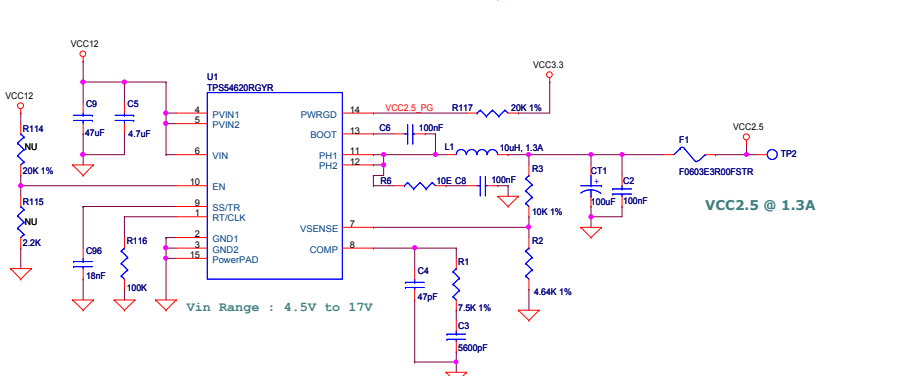
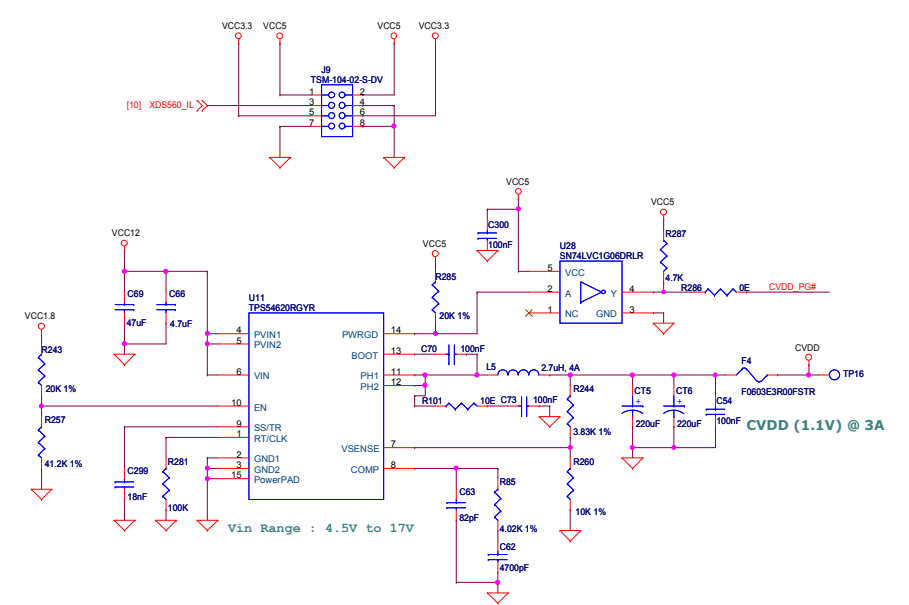
- FP GP01 BTMODE0 R229 4.7K
- FP GP02 BTMODE1 R235 4.7K
- FP GP03 BTMODE2 R389 4.7K
- FP GP04 BTMODE3 R261 4.7K
- FP GP05 DEVLNUM0 R266 4.7K
- FP GP06 DEVLNUM1 R265 4.7K
- FP GP07 DN2_US1 R92 4.7K
- FP GP08 DN3_US2 R264 4.7K
- FP GP09 CFGP0 R279 4.7K
- FP GP10 CFGP1 R289 4.7K
- FP GP11 CFGP2 R301 4.7K
- FP GP12 CFGP3 R84 4.7K
- FP GP13 CFGP4 R303 4.7K
- FP GP14 HPWIDTH R265 4.7K
- FP GP15 ECLKINSEL R293 4.7K
- FP GP00 LENDIAN R292 4.7K

| | | | |
|---|---------------------------------------|-------------------------------|--|
| Project TMDSEVM6457L | | Designed for TI by einfochips | |
| Title FPGA - NAND Flash Interface | | | |
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12V DC Input Supply



XDS560 v2 Mezzanine Power

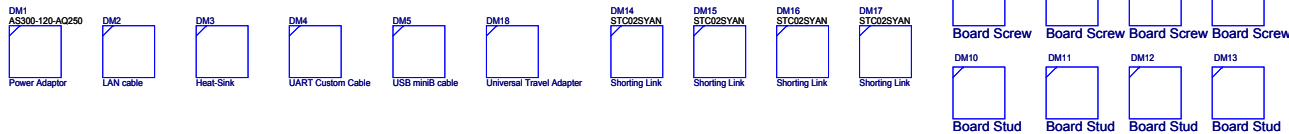


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| Title Board Power Supply | | | |
| Size C | Document Number 16-00079-02 | Rev 2.0 | |
| Date: Monday, October 11, 2010 | | Sheet 11 of 12 | |

TMDSEVM6457L - REVISION HISTORY

| PCB REV. | SCH. REV. | CHANGE DESCRIPTION | DATE | AUTHOR |
|----------|-----------|---|------------|------------|
| 1.0 | Issue 1.0 | - Released for PCB fabrication -- Proto Boards | 28JULY2010 | eInfochips |
| | Issue 1.1 | Pilot Batch Release - U32 part number changed to TXS0108EPWR - Board Identification # changed to 001 from 000 - R280 (4.7K) made NU, 4.7K PD added on EM_TRST#, 1K PD added on TRST# net - 1M bias resistor added on Y2.1 pin | 17SEP2010 | eInfochips |
| 2.0 | Issue 2.0 | Production Batch Release - Pull up added on XDS560_IL net - AMC_DETECT# signal to FPGA taken from Level Translator chip U29 - CT11 part # changed - Board Identification # changed to 010 | 11OCT2010 | eInfochips |

Dummy Components



| | | | |
|--|---------------------------------------|---|-------------------|
| Project TMDSEVM6457L | | Designed for TI by eInfochips | |
| Title Revision History & Dummy Parts | | The Solutions People | |
| Size C | Document Number 16-00079-02 | | Rev 2.0 |
| Date: Monday, October 11, 2010 | | Sheet 12 of 12 | |