**Advanced fault models in small-scale CMOS technology nodes**


With small-scale CMOS technology nodes, the probability of physical defects occurring in the device increases. Various defects occur which cannot be detected with the help of conventional Single Stuck-at and Transition Fault models. Due to this barrier, use of advanced fault model for detection of physical defects becomes necessary.

The ATPG tool supports the following advanced fault models which can target various classes of faults within the design. Ideally, this tool can apply various test pattern sets that can cover possible faults within the design. This test strategy can help one to increase the high defect coverage leading to drastic test quality improvement. As given below, Path delay, Hold Time, Small delay and Iddq are diverse fault models supported by ATPG tools other than conventional Single Stuck-at and Transition fault models.

**Path Delay Test:** The path delay test targets faults in the critical path design. During the Static Timing Analysis, the information regarding critical timing paths can be extracted. This information is applied to the ATPG tool for targeting those critical paths. As per the following diagram, the clock period of the circuit is 7ns. The total propagation delay for path P3 B-e-f-g-Z is 6ns, so the path P3 has a small timing slack to meet the requirement. Such information on Critical Timing paths need to be extracted from design analysis. The paths can be targeted through the ATPG tool to generate patterns. One can get signoff that the IC can withstand on such critical timing paths, after successfully executing the path delay test. We observed in our analysis that 73 dies passed through the conventional transition, but 2 dies failed the path delay test. Path delay tests can detect defects those might escape transition tests with higher test coverage.
Hold Time Test: The hold time test targets the shortest paths which have maximum timing slack in the design. The shortest paths may result in hold time violation. The ATPG tool will target those paths to cover possible occurrences of fast-to-rise and fast-to-fall faults in the design. As hold time violation is independent of clock period, it can also be detected with stuck-at test. There is still the possibility that the path having hold time violation can escape with stuck-at patterns as these patterns might not create conditions or transitions that is necessary to detect hold time violations. The adoption of this new fault model enables us to detect all possible hold time violations effectively and also makes diagnosis quickly and easily. The following figure is a representation of hold time ATPG pattern.

Small Delay Defect test: Conventional transition delay tests target the easiest sensitizable path between two flipflops. As displayed in the figure below, there are three possible paths (Path1, Path2 and Path3) to detect the slow-to-rise or slow-to-fall faults at the mentioned location by cross mark. In the conventional Transition fault model, the ATPG tool will target the easiest sensitizable path which is Path3. This Path3 has maximum timing slack compared to others, while Path1 has minimum
timing slack. So any possible physical defect on Path1 can create failure, which will not be detected by conventional Transition fault model. This results in possible test escape at small-scale CMOS technology nodes, where smaller delays can result in timing failure. The small delay defect test, targets the path of each nodes between the two flipflops having smallest timing slack. In the figure given below, one will note that the small delay defect will target Path1 having smallest timing slack. This method can help avoid possible test escapes due to timing failure. A study says that more than 60% of delay defects would be occurred due to smaller delay defect as the technology shrinks.

**Iddq test:** Iddq tests help to measure the quiescent current. Sometimes the physical defects like gate-oxide short can result in very high leakage current. Such types of physical defects cannot be modeled properly with the help of Single Stuck-at fault model. Apart from that, the logic inside the design is intentionally kept as a non-scannable. Due to this, the conventional ATPG test cannot target those faults. Iddq can detect defects with high coverage in fewer patterns compared to Stuck-at test. It can even detect faults that remain undetected after stuck-at tests.

One can achieve high defect coverage with the help of various fault models, that in turn reduce possible testability escapes. This approach also results in lower DPPM (Defective Part Per Million) after field tests. The Williams and Brown equation for the DPPM can be given as below,

\[ D = (1 - Y^{(1-C)}) \]

where
D = Defect rate, DPPM = D \times 10^6

Y = Yield, 0 < Y < 1

C = Defect coverage, 0 < C < 1

- Based on the above equation, DPPM would be '0' for 100% coverage on any yield.
- DPPM = 10^6 for 0% coverage on zero yield.
- DPPM = > 200 for 99% coverage on 70% yield.

**CONCLUSION:** Achieving high defect coverage becomes necessary with the small-scale CMOS technology nodes. With the reduction in the size of the CMOS device, various physical defects can occur which remain undetected with the help of conventional tests. Any possible test escape in the test strategy can result in failures in the field or during system level testing, thus contributing to high DPPM. Such types of test escapes can prove to be extremely costly and unfavorable to chip manufacturers and the service industry. To avoid such situations, better test strategies need to be developed to target various faults. Applying various test vectors of various fault models can be a better solution for test quality improvement. One can take advantages of all fault models and achieve high defect coverage in the process too.

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**Also see:**

- Guidelines improve test quality in advanced CMOS nodes