ATPG Challenges at Lower Technology Nodes

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Abstract:

With regards to the ongoing trend of diminishing transistor geometries, we are witnessing a sharp increase in defect density along with significant on-chip process variations that affect transistor size, threshold voltage, and wire resistance. Due to these factors, new fault models and scan techniques have to be introduced to ensure high quality testing. Due to continuous reduction in transistor geometries, the available pin count for test keeps on reducing which places a serious burden on semiconductor companies wishing to perform Design for Testability (DFT). Power dissipation during the test affects yield and introduces failures that can only occur during the test procedure. So, DFT has to be redesigned considering the power consumption by test vectors being used.

With lesser pins available and greater need for logic check, the failure diagnosis after the chip is implemented has become trickier than before and needs major attention during test architecture design. In this blog, we have covered our experience at **eInfochips** in addressing ATPG challenges at lower technology nodes. We speak from our direct experience being counted as one of the very few engineering services companies in the world capable of delivering 16nm chip designs which reduce a chip's power consumption by half, while improving performance by one-third over 28nm technology.

Keywords: DFT (Design For Testability), MBIST (Memory Built-In Self-Test), ATPG (Automatic test pattern generation), UDFM (User defined fault models), LPC (Low pin count), SDD (small delay defect), FinFET (Fin Field Effect Transistor), SoC (System On Chip), DPPM (Defective Parts Per Million), .

1. Added defects at lower technology node.

The major factors which cause delayed defects in the design due to decreased geometries are: Process Variation, Cross Talk and Power Supply Noise effects. Also, the new faults related to FinFETs needs to be taken into account. To ensure high quality testing, the following mentioned techniques have to be involved for the purpose of testing.

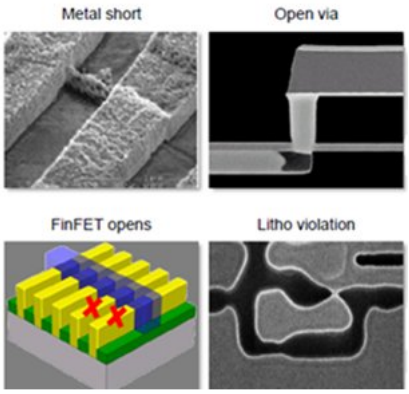


Figure 1: Examples of Physical Defects

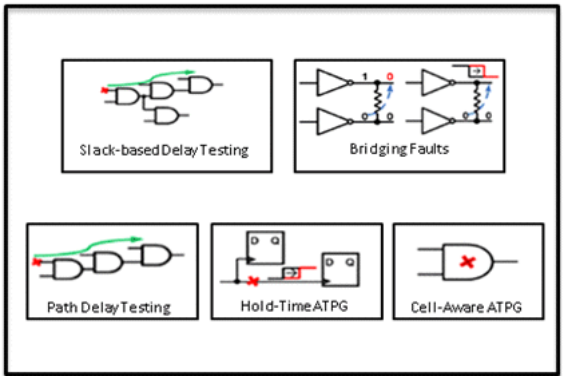


Figure 2: Advanced Fault Models

1.1- Path Delay Test: Path Delay test targets the critical paths in design which assume that there is a cumulative delay defect along a given combinational path causing the path to exceed some specified duration and making sure critical paths are actually getting tested.

1.2- Slack-based delay testing: Regular transition fault testing cannot detect SDDs as it targets faults on shorter or easily sensitizable paths. In case of slack-based delay testing, the faults are targeted in such a way that they get sensitized on the minimum slack path. The slack information can be given from SDF.

1.3- Hold Time ATPG: Hold time test patterns are conceptually similar to path delays with the difference being that they are targeted for hold violations instead of setup violations. So paths with largest slack (fastest path) have to be taken into account for hold time check. To test hold violation, only one clock pulse is needed during capture as opposed to two clock pulses for path delay test.

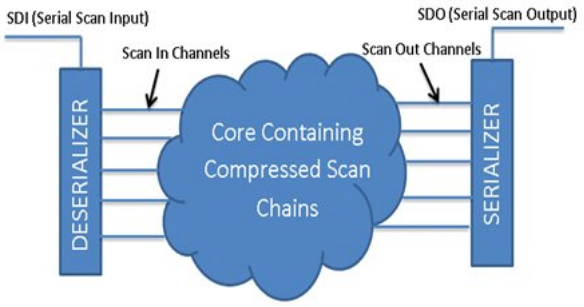
1.4- N-detect ATPG: The n-detect ATPG can be an effective method for detecting SDD and Bridging Faults, even without having timing information of the design. For each targeted fault, n-detect ATPG will generate patterns trying to detect it n times, through different paths. By that, the tool will have a good chance of detecting faults via their possible long paths.

1.5- Bridging faults: Bridging faults are more prominent in shrinking technology because smaller distances between metal interconnect results in a short between groups of signals. The bridging faults are targeted separately as they require layout information for making the fault list.

1.6- Faster-than-at-speed testing: This technique increases the test frequency to reduce the positive slack of the path to detect SDDs on target paths. Drawbacks of this method are Overdesigned clock generation which can be expensive and false identification of good chips due to the reduced cycle time as well as increased IR-drop which can lead to unnecessary yield loss.

1.7- Cell Aware ATPG: A cell-aware ATPG method performs a characterization of the library cell's physical design to produce a set of UDFMs. The actual cell-internal physical characteristics are used to define and target faults.. The cell-aware test methodology is well suited for addressing defect mechanisms specific to FinFETs. The defects in FinFET can be captured by proper cell library characterization. Once that is completed, the result is a UDFM model that can be used with the ATPG tool.

2. Low Pin Count and test time reduction:



There are various factors that make low pin count testing important in lower technology nodes.

- Reduced number of digital pins available because of small package size.
- The increasing use of very-low-cost testers that have memory and pin limitation.
- Multi-site testing technique, where multiple dies are attached to tester and all the dies are tested in parallel, so lower the test pin count per die, more number of dies can be tested simultaneously.

Scan compression techniques have become necessary to reduce the tester time, test pins and tester data volume. The lesser pin count causes data-correlation at input end and aliasing at output end which makes the compression ineffective. To avoid this, one of the solution is to add Deserializer/Serializer structure before the scan chains. Deserializer/Serializer can works at higher frequency so the internal shift frequency is not changed. So test time remains same with less number of test pins.

3. Reducing Power Consumption:

Power consumption is one of the major issues to be factored in during functional testing as well as other tests. For reducing the test time, there is a tendency to test maximum things in the least possible amount of time. Thus the switching during test is generally more than that during function. Increase in test power can lead to good dies detected as faulty dies which affects the yield due to increase in IR drop above the limit that is functionally acceptable.

Or worse, the excessive heat dissipation during test can burn the chip. The effect due to power is prominent in lower technology nodes. We need to incorporate low power ATPG techniques like *X-fill, clock gating control*, *blocking scan cell outputs* and *test scheduling*. Hierarchical testing helps in reducing the power by selectively doing test for different hierarchies. Further Hierarchical SoC implementation helps to reduce runtime of test vectors, faster post silicon debug and core reusability. For power reduction techniques present functionally, special care has to be taken while building scan chain, to reduce the number of level shifter and isolation cells added during scan [4].

4. Diagnosis Support:

Lower technology nodes bring new design challenges that influence Design For Test strategies. At lower technology nodes, defect densities are higher. So diagnostics play an important role in accurately identify the manufacturing defects in failing devices which ramps up support for yield learning and production. The diagnosis support should help to identify the defect location and defect type on the failing devices. The DFT logic inserted such as test compression logic should provide fail data and help in intelligent failure analysis.

Conclusion:

In this blog, we have discussed ATPG challenges at lower technology nodes based on my direct experience with eInfochips clients. The new fault models SDD, Hold Time ATPG, n-detect, Bridging Faults, Cell Aware ATPG are a must at low technology nodes. By taking care of these ATPG challenges discussed, we can detect new faults, achieve low DPPM and low cost of testing even at lower technology nodes. Further DFT challenges related to advanced MBIST fault models & diagnostics at lower nodes will be discussed in the coming blogs.

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