

Overview:

AXI 4.0 VIP is reusable, highly configurable, pre-verified, plug-and-play verification component developed in System Verilog solution for SoC incorporating AXI 4.0 component at Module, Chip and System level.

Key Features:

- Supports File size and Incremental burst
- Support for aligned and multiple transfer
- User and Response Signalling support

Deliverables:

SystemVerilog Source Code

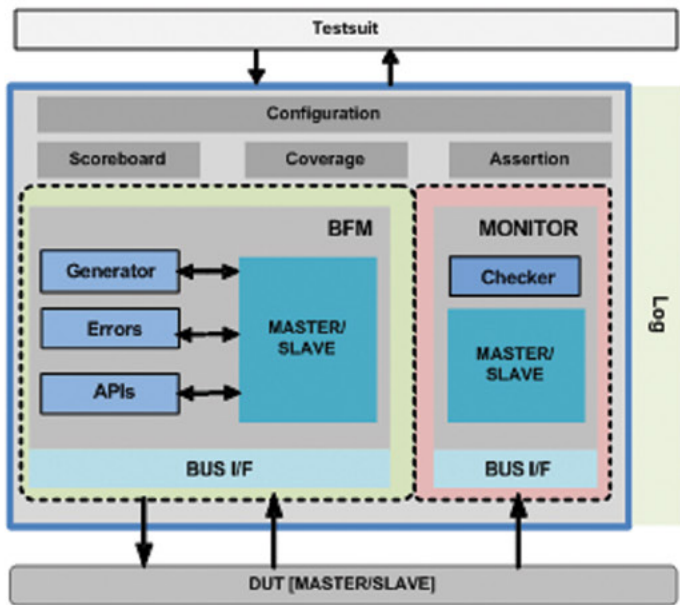
Sanity Testcases

Examples of Topological Usage

Sample Verification Environment

User Guide and Release Notes

Test Plan + Coverage Plan [Upon Request]



- Fully compliant to Methodology : UVM, OVM and VMM
- Separate module for AXI 4.0 and AXI 4.0-LITE assertions
- Hook-ups for end-to-end score boarding
- Supports variety of Error Injection via generators / callbacks in data transactions
- Fully configurable data transactions

AXI 4.0 VIP can be used as MASTER, SLAVE or MONITOR component to verify AXI DUT. AXI 4.0 MASTER can issue READ or WRITE request with FIX or INCREMENT burst type and AXI4.0 slave can accept them and respond accordingly. Master, Slave and Monitor can also be turned into AXI4.0-LITE component.

Custom VIP Development and Verification Services

eInfochips has developed dozens of complex VIPs for top global EDA companies and end-customers. Our experience includes VIPs for the latest high-speed and low-power protocol standards, like MIPI, SERDES, USB 3.0, DDR3, HDMI and eMMC. Today, eInfochips has contributed to VIPs that are deployed by hundreds of customers to bring confidence to their ASIC, SOC and FPGA designs.

eInfochips is a Product and Semiconductor Engineering Solutions company recognized for technology leadership by Gartner, Frost & Sullivan, NASSCOM and Zinnov. eInfochips has contributed to 500+ products for top global companies, with more than 10 million deployments across the world. The company is debt-free and profitable since inception in 1994.

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