Squeeze the Power of Specman Elite™

Taking care of 'x' and 'z' signals during e code development

While checking for signals from the verilog or vhdl variables, allow the necessary conditions for checking x and z states of the signals. For e.g., consider the following code. This code exemplifies the effect of 'z' on the rise events.

```
extend sys {
simu : simu is instance;
};

unit simu {
keep hdl_path() == "test_sim";
sig_a : string;
keep sig_a == "a";
// signal test_sim.a can assume any of the values from 0,1,x,z

event a_rise is rise('(sig_a)') @sim;
// 1. from '0' to 'z'
// 2. from '0' to '1'
// 3. from 'x' to '1'
// 4. from 'x' to 'z'
on a_rise {
out (">>>>","sig_a rise at ",sys.time, " time");
};
};
```

The above code will execute and give the rise events as mentioned in points 1 to 4 in the comments.
Changing the code as below will limit the rise event to changing from 'x' to '1' and from '0' to '1'.

```
event a_r is rise('(sig_a)') @sim;
event a_rise is true('(sig_a)' !== 1'bz) @a_r;
```

The same can be done for fall events by checking for 'x' values.