

How to improve speed and minimize the peak power requirement in physical design?

Negative setup libraries can be used for better optimization & to achieve improved timing. This concept sounds good in building the useful skew inside the library itself, and if you can account some clock path delay during synthesis, it would definitely increase the speed as well as reduces the peak power requirement. The advantage of using negative setup cells is right from the synthesis level as it provides an edge over the tool, that utilizes the concept of useful skew later, by utilizing these timings before proceeding for the physical design.

The advantages are:

1. Optimum drive cells for implementation in data path is chosen at the Synthesis Level which may not be so efficient during the Physical implementation stage.
2. The overall speed of the design may improve.
3. Peak Currents near the clock edges may get reduced.
4. We may see area/power reduction overall in the design.

An additional advantage with the back end tools is achieving timing closure using this type of cells, because of the fact that all the finer tuning cells have the same footprints of the other cells. So, while doing timing analysis, even if some paths having these skewed FF are not meeting timing constraints we can simply replace them with higher or lower skew cells of same drive.

