

An unconventional way to program the Flash in DSP & FPGA based systems

In a slave parallel mode configuration for Spartan II FPGA (for example), the FLASH is used for loading the FPGA **application code** at power ON. This **application code** in the FLASH can be changed by using another 'read-only' **Utility code** within the FLASH itself, which can be loaded onto the FPGA using a switch for selection. This read-only FPGA **utility code** when loaded onto the FPGA has the sole function of taking the changed **application code** data from the DSP interface to the FPGA and write to the **application code** region of the FLASH. The figure given below illustrates the functionality. The CPLD provides the address sequence to the FLASH.

