

INDIA: RIDING HIGH ON THE CHIP TIDE

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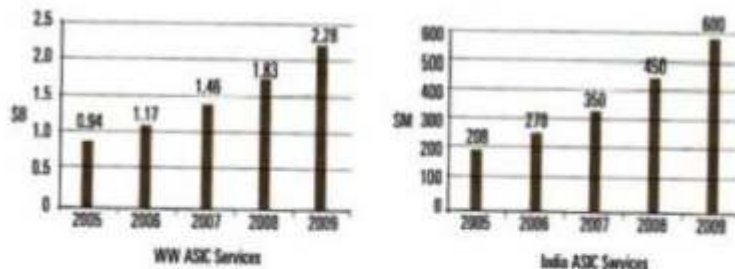
Success in chip design has always been about being the first one to produce low-cost, feature-rich and performance-enhanced products. The intensifying pressure to reduce cost and time-to-market while keeping up with the growing complexity of chips, led to radical changes in chip design methodology. The conventional integrated forms of design organizations where entire chips were designed within a single firm, gave way to vertical specializations where stages of chip design were outsourced to other firms. In addition to this fragmentation of the design cycle, the global semiconductor industry witnessed two other major discontinuities: (1) the emergence of the fabless semiconductor model marking the separation of the "capital intensive" fabrication phase from the "people intensive" design phase; and (2) the rapidly growing "design gap."* These transformations fragmented the market and enabled countries, such as India to enter the chip design industry by offering services at different points in the design process.

While these key global trends served as push factors in helping India enter the electronics product design services arena, India's intrinsic strength in software worked as a strong pull factor. With chip design requirements being implemented in software languages that describe digital circuits at register-transfer level (RTL), India was the obvious destination for all types of software development, chip design and system design. Additionally, India offered a vast pool of qualified engineers who could meet the resource requirements of the fabless companies at much lower rates than their counterparts in the United States.

Outsourcing design services to India is becoming more accepted. The trend, which started with small offshore projects, has now moved on to multi-year and multi-project deals. An increasing number of companies are also setting up dedicated design centers that work as extensions of their design centers in the United States. Today, India is one of the top three outsourcing destinations in the world and home to approximately 25% of the consulting firms to which the U.S. companies outsource their designs. In spite of this, the Indian semiconductor industry's market share is a small fraction of the world market. The global semiconductor market is estimated to be over \$200 billion, with the Gartner Group predicting a compound annual growth rate (CAGR) of 10.6%. According to

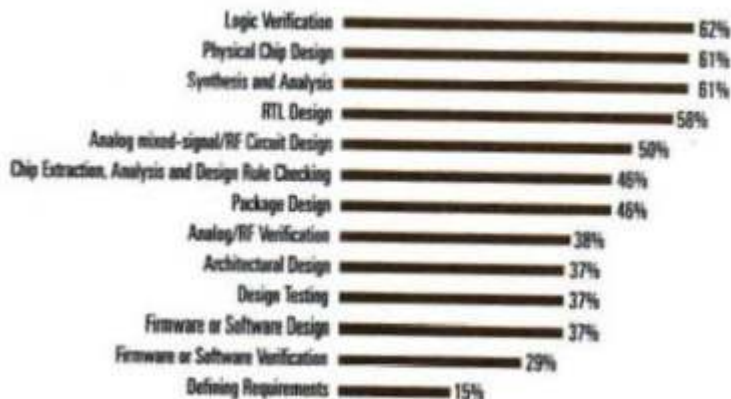
eInfochips's internal estimates, by 2009, the worldwide application-specific IC (ASIC) services market is estimated to touch \$2 billion with India's design services market share rising to \$600 million (Figure 1).

Figure 1. eInfochips' Internal Estimates of ASIC Design Services Market



A recent study conducted by *EE times* and *Electronics Supply and Manufacturing*, directed towards managers who currently outsource chip design activities to third-party IP, showed that logic verification is the most frequently outsourced chip design activity (Figure 2). This is not surprising because though verification is an essential phase in the chip design cycle, it is a complex, multi-stage, time-consuming process with huge associated development costs. With chip development requiring large investments, it is important to get the design right at the first attempt. One error can decide the success or failure of a product.

Figure 2. Design Outsourcing Survey for Chip Design Activities



Source: *EE Times* & *Electronic Supply and Manufacturing*

* Design gap refers to the gap between the available capacity of gates on a chip and the design capacity or the resources available to design those gates.

Outsourcing of verification also means a clear separation between design and verification teams. This becomes critical as independent operation of design and verification teams with minimized interaction helps in determining all the possibilities of misconceptions at the designers' end.

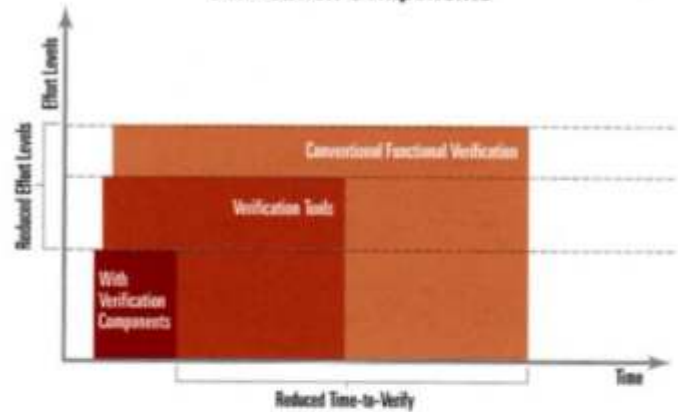
Focus on design services has proved to be highly lucrative for Indian companies, but they must venture into other market segments. Take for example the silicon intellectual property (SIP) market. The SIP market, which is also a byproduct of the "design-gap" phenomenon, is still in its formative years but offers great potential. With the increasing gate count, it will soon be impractical to design chips without effective reuse of design blocks. SIP firms provide IP blocks, which after minor modifications can be reused for other designs, enabling faster project ramp-up, thereby decreasing time-to-market. Moreover, IP development is not a well-accepted business model for U.S. companies because it is not scalable to the volumes required for financial, but is definitely a good business model for the Indian companies.

The concept of using third-party IP to design systems-on-chip (SOCs) looks simple, but often times SOC designers do not completely understand what drives the design operations of the blocks they work with and face difficulties in integrating the IP in their SOC. This provides an opportunity for IP providers to offer value-added system integration services to their customers. The other advantage is that chip companies prefer design services companies that offer IP in addition to their regular suite of services because clients are more confident in companies that have showcased their design capability expertise by way of IP development. IP development serves as a showcase of design expertise for the services companies.

Effective reuse of verification environments is just as essential as reuse of design environment. IP/design reuse provides only 30% to 40% effort savings, but the big return on investment (ROI) lies in verification reuse. Conventional functional verification consumes up to 70% of the time and resources of the total chip design cycle. Use of sophisticated verification tools significantly reduces time and effort, but use of verification IP (VIP) offers remarkable value to teams trying to integrate an IP core into their device. Until recently, VIP only consisted of a bus-functional model (BFM) and possibly included a monitor for protocol checking. For a VIP to be effective in enabling reuse of complex design IP, it needs to provide many more features and functions. The main advantages of using verification IP are: reduced time-to-verify, reduced costs, a scalable verification environment that enables bottom-up verification of complex SOC and fast ramp-up to functional testing stage (Figure 3).

A testament to the fact that Indian companies can work on the latest cutting-edge technology is the steady increase in the number of companies venturing into research and development. Today, India is a home to more than 150 research and development (R&D) outsourcing centers set up by companies, such as TI, GE, Intel, Cisco, Microsoft, Motorola and others. These centers are actively engaged in definition and development of next-generation processors, digital signal processors (DSPs) and communication chips. This can be attributed to the fact that semiconductor companies no longer outsource just to avail cheap labor and do away with undesirable tasks. They have recognized the enormous amount of knowledge resources available in India and are leveraging it to develop new

Figure 3. Improved Verification Productivity Using Verification Components



products faster. This demonstrates that the Indian technology industry is well poised to make its mark as an innovator and not just an implementer.

The current business environment in India is also highly conducive to jumpstart the innovation movement. A large number of Indian origin engineers are moving back to India, bringing with them years of experience in leading-edge technologies. The technological industries have also recognized the benefits of academia and industry interaction by actively participating in activities, such as curriculum development, funding student research projects and offering career guidelines to the students. And most importantly, the middle class of India has finally arrived. The buying power of India's population has considerably increased, enabling them to avail the new products and facilities available. This has opened a large market, forcing the global technology giants to define and develop products specifically addressing the needs of this market. It also presents the Indian design services providers an opportunity to move up the food chain to develop complete products.

The semiconductor industry promises a bright future for India, but the same can beset-back if a few basic problems are not addressed. First, there is a lack of linkage between the Indian semiconductor firms and the foundries in Korea and Taiwan. Second, is the lack of analog and mixed-signal domain expertise. For fast growth, the indigenous design service providers need to build tight relationships with foundries and testing/packaging houses. They also need to stifle their opportunistic mindset and concentrate on investing time, effort and resources with long-term goals in mind. ■

About the Author

Niyati Naik holds a BSEE from Michigan Tech University and works as a marketing manager for the ASIC solutions and services division at elfnfochips. She is responsible for defining and promoting elfnfochips' ASIC portfolios of IP leveraged services like ChipMaestro and VeriSuite. In her role, she spearheads partnership programs with EDA tool companies to enable elfnfochips provide effective services to its customers. She also contributes towards developing new strategies for winning in the ASIC market. elfnfochips is a leading provider of cutting-edge ASIC design and verification services, embedded systems solutions and IP cores. Their capabilities extend from specification to system, with knowledge on ASIC design & verification, physical design, board design and embedded firmware development. The company's India and U.S. design centers have delivered SOC and embedded solutions to a variety of customers, thus increasing their cost-effectiveness, reducing their time-to-market and growing their market strength. A partial list of customers includes GateInx, TI, IDEO, Northrup Grumman and Cisco.