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eInfochips rolls four VMM-enabled VIP products

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Indian design services company eInfochips Ltd announced the availability of Verification Methodology Manual (VMM)-enabled MIPI Camera Serial Interface (CSI-2), Display Serial Interface (DSI), High Speed Synchronous Interface (HSI) & SDIO verification IP (VIP).

The eInfochips VIP has also been added to the Synopsys DesignWare Verification IP Alliance Program. The Alliance program gives designers access to a broader range of VMM-enabledverification IP, which complements the DesignWare verification IP portfolio.

"eInfochips has been developing verification IP for many years and has seen an increasing demand for VMM-enabled verification IP for MIPI standards," said Sribash Dey, VP of Sales at eInfochips. "By working closely with Synopsys to develop VIP that is in accordance with Synopsys' guidelines and VMM rating tool, our mutual customers can have access to a wider range of VMM-enabled verification IP that helps accelerate their verification process."

eInfochips' VMM-enabled MIPI CSI-2, DSI & HSI, and SDIO VIP products are based on the layered architecture of object oriented programming that allows

coverage-driven verification suitable for verifying transmitter and receiver with either of them as the design-under-test (DUT).

MIPI CSI-2 VMM-enabled verification IP

The VMM-enabled MIPI CSI-2 VIP is compliant to the CSI-2 MIPI Specification version 1.0 and draft MIPI Alliance Standard for D-PHY Version 0.85.00.

MIPI CSI-2 is an interface between a digital imaging module such as a host processor and image sensor peripheral such as a camera. The VIP for the MIPI CSI-2 interface can be configured as a transmitter, receiver or monitor. The 4 channel VMM-enabled MIPI CSI-2 VIP has fully configurable short and long packets and supports RGB, YUV and RAW long packet data types and short pack synchronisation. The VIP supports directed/constrained/fully random testing mode, monitors and checkers for protocol violations, coverage report generation while allowing configurable transaction generation for each device model.

MIPI DSI VMM-enabled verification IP

The VMM-enabled MIPI DSI VIP is compliant to the DSI MIPI Specification for Version 1.00 and draft MIPI Alliance Standard for D-PHY Version 0.85.00.

MIPI DSI is an interface between a digital imaging module such as a host processor and display peripheral such as an LCD. The MIPI DSI VIP can be configured as a transmitter, receiver or monitor and allows system level verification. It is a highly configurable, SystemVerilog verification IP that supports 4 virtual channels, RGB colour format for 16bit, 18bit & 24bit, DCS read/write commands & generic write commands, interleaved and normal frames, bidirectional data transfer and PPI control interface. The VIP supports fully

configurable fields of short and long packets, directed, constrained and fully random testing, coverage report generation and command mode of operation.