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eInfochips Announces VMM-Enabled MIPI CSI-2, DSI & HSI and SDIO Verification IP for the Synopsys DesignWare Verification IP Alliance Program

Reduce schedule risk through improved quality, scalability and predictability

Ahmedabad, India -- June 30, 2009 - eInfochips Ltd., a leading design services company today announced the availability of Verification Methodology Manual (VMM)-enabled MIPI® CSI-2 (Camera Serial Interface), DSI (Display Serial Interface), HSI (High Speed Synchronous Interface) & SDIO Verification IP (VIP). The eInfochips VIP has also been added to the Synopsys DesignWare® Verification IP Alliance Program. The Alliance program gives designers access to a broader range of VMM-enabled verification IP, which complements DesignWare Verification IP portfolio. Synopsys selected and qualified eInfochips for the Alliance program because of its extensive experience in verification, VMM methodology and verification IP development.

“eInfochips has been developing verification IP for many years and has seen an increasing demand for VMM-enabled verification IP for MIPI standards,” said Sribash Dey, VP of Sales at eInfochips. “By working closely with Synopsys to develop VIP that is in accordance with Synopsys’ guidelines and VMM rating tool, our mutual customers can have access to a wider range of VMM-enabled verification IP that helps accelerate their verification process.”

“The addition of eInfoChips’ MIPI and SDIO VIP to the DesignWare VIP Alliance Program further expands the broad range of VMM-enabled verification IP that is complementary to the DesignWare portfolio” said John Koeter, vice president of marketing for the Solutions Group at Synopsys. “With eInfochip’s extensive experience in VMM-enabled verification IP, designers can have confidence that the verification IP can be easily integrated into System-Verilog verification environments, helping to speed testbench development efforts.”

eInfochips' VMM-enabled MIPI CSI-2, DSI & HSI, and SDIO VIP products are based on the layered architecture of object oriented programming that allows coverage-driven verification suitable for verifying transmitter and receiver with either of them as the design-under-test (DUT).

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MIPI CSI-2 VMM-Enabled Verification IP

eInfochips' VMM-enabled MIPI CSI-2 VIP is compliant to the CSI-2 MIPI Specification version 1.0 and draft MIPI Alliance Standard for D-PHY Version 0.85.00. MIPI CSI-2 is an interface between a digital imaging module such as a host processor and image sensor peripheral such as a camera. The VIP for the MIPI CSI-2 interface can be configured as a Transmitter, Receiver or Monitor. The 4 channel VMM-enabled MIPI CSI-2 VIP has fully configurable short and long packets and supports RGB, YUV and RAW long packet data types and short pack synchronization. The VIP supports directed/constrained/fully random testing mode, monitors and checkers for protocol violations, coverage report generation while allowing configurable transaction generation for each device model.

More information available at <http://www.einfochips.com/services/asic/IP/mipi-csi2-vmm-ip.php>

MIPI DSI VMM-Enabled Verification IP

eInfochips' VMM-enabled MIPI DSI VIP is compliant to the DSI MIPI Specification for Version 1.00 and draft MIPI Alliance Standard for D-PHY Version 0.85.00. MIPI DSI is an interface between a digital imaging module such as a host processor and display peripheral such as an LCD. The MIPI DSI VIP can be configured as a Transmitter, Receiver or Monitor and allows system level verification. It is a highly configurable, SystemVerilog verification IP that supports 4 virtual channels, RGB color format for 16bit, 18bit & 24 bit, DCS read/write commands & generic write commands, interleaved and normal frames, bidirectional data transfer and PPI control interface. The VIP supports fully configurable fields of short and long packets, directed, constrained and fully random testing, coverage report generation and command mode of operation.

More information is available at <http://www.einfochips.com/services/asic/IP/mipi-dsi-vmm-ip.php>

MIPI HSI VMM-Enabled Verification IP

eInfochips' MIPI HSI VMM-enabled VIP is compliant with the version 1.01.00 specification. MIPI HSI is an interface between an applications processor and cellular modem. The MIPI HSI VIP can be used for system level verification of DUT MIPI HSI transmitter and/or receiver and for functional coverage generation. The highly configurable, VMM-enabled SystemVerilog verification component supports synchronized/pipelined/receiver data flows and stream/frame transmission modes. Other features of MIPI HSI VIP are error injection, functional coverage, random as well as user-defined configuration and run-time configurability. More information is available at <http://www.einfochips.com/services/asic/IP/mipi-hsi-vmm-ip.php>

SDIO VMM-Enabled Verification IP

eInfochips' VMM-enabled SDIO HOST VIP allows coverage-driven verification and can be configured as IO-aware or non IO-aware to verify SDIO card, SD memory card, SD Combo card and SD Multimedia Card (MMC). The VIP is compliant to the SD Host

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Specification 1.0, SD Specification 1.10 and 2.00 and to the SDIO Specification 1.2. It offers support for single slot operation, card detection, re-initialization of combo card, 1/4/8 bit SD bus mode and SPI bus mode, low/full/high speed, stream transfer and direct command during data transfer. The VIP also facilitates functional coverage, card suspend/resume/lock/unlock operations, protocol and transaction level checking and plug-and-play operations.

More information is available at <http://www.einfochips.com/services/asic/IP/sdio-vmm-ip.php>

Deliverables

Deliverables include verification IP encrypted code, sample test bench and test cases, user guide and release notes.

Support & Availability:

eInfochips provides regular product updates and technical support. MIPI CSI-2, HSI, DSI & SDIO VMM-enabled VIP products are now available. For pricing details, please contact us at sales@einfochips.com.

About the DesignWare Verification IP Alliance Program

The DesignWare Verification IP (VIP) Alliance Program connects engineers to a broader range of VMM-enabled verification IP, complementing the DesignWare VIP portfolio. Members of the Alliance have extensive experience in verification methodology, VMM, and verification IP development. The Verification IP included in the Alliance program is developed using common guidelines to help ensure that a consistent use model is delivered to engineers. For more information on DesignWare IP and the Alliance Program, please visit: <http://www.synopsys.com/designware>

About eInfochips

eInfochips is a leading IP driven design services company with the range of services and solutions in ASIC/Chip/SoC, Embedded System and Software. eInfochips' Chip/ASIC group has capabilities spanning from ASIC/Chip design, verification, physical design, FPGA design & prototyping and IP Cores development and integration. For more information, visit www.einfochips.com.