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elfinichips announces DDR2 SDRAM verification IP and Reed Solomon Encoder design IP

- *DDR2 SDRAM (Double-Data-Rate-Two Synchronous Dynamic Random Access Memory) verification IP is fully compatible to JEDEC standard (JESD79-2D)*
- *Reed Solomon Encoder IP is compatible to European DVB standard, IEEE 802.16, IntelSat Earth Station (IESS), ETS 300 421 and ETS 300 429 standards*

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Ahmedabad -- November 6, 2008 -- elfinichips, Inc., a leading IP leveraged design and verification services company today announced the availability of JEDEC (JESD79-2D) compliant DDR2 SDRAM (Double-Data-Rate-Two Synchronous Dynamic Random Access Memory) verification IP and European DVB, IEEE 802.16, IntelSat Earth Station (IESS), ETS 300 421 and ETS 300 429 standards compliant Reed Solomon encoder design IP.

elfinichips' DDR2 SDRAM verification IP (VIP) can be used to verify JEDEC standard (JESD79-2D) based DDR2 SDRAM memory model(s). The Reed Solomon design IP is designed for efficient implementation on FPGA and ASIC and can be used for communication systems like satellite communication, telecommunication, video and audio broadcast or data storage systems (ex: CD-ROM, Hard Disks etc.).

"Our high performance, fully programmable, standards compliant Reed Solomon Encoder IP Core is intended for use in a wide range of applications requiring forward error correction and can be targeted in any ASIC or FPGA technologies," said Nirav Shah, Director of Marketing at elfinichips. "Also, our DDR2 SDRAM Verification IP is a thoroughly verified, highly scalable plug and play core equipped with a user interface and would enable our customers to greatly reduce their discrete memory subsystem chip development time and costs."

DDR2 SDRAM VIP:

The DDR2 SDRAM verification IP supports normal mode command operations, multiple bank operations, data transfer with sequential/interleaved burst, extended mode registers, variable additive latency (0 – 5 clocks), differential signaling for DQS (or LDQS and UDQS) and RDQS signals and auto configuration of timing parameters.

The command operations supported by DDR2 SDRAM VIP are truncated read/write, data masking, read/write with auto-precharge, posted column address strobe (CAS) read/write and seamless read/write command operations for bandwidth conservation. User configurable features of DDR2 SDRAM VIP are clock frequency model (400, 533, 667, 800), data port interface (x4, x8, x16), memory size (256 Mb, 512 Mb, 1 Gb, 2 Gb, 4 Gb), speed bins (3-3-3, 4-4-4, 5-5-5, 6-6-6).

The verification features available are functional coverage for coverage driven verification, protocol checks (assertions), active/passive VIP configuration operation and error injection mechanism.

Deliverables:

DDR2 SDRAM VIP deliverables include documentation of verification environment plan, verification plan, test plan, assertion plan and coverage plan. Also delivered is a sample verification environment illustrating DDR2 SDRAM VIP instance and its active operations, verification environment supporting responder (DDR2 DUT emulator) and data integrity checking scoreboard modules, comprehensive coverage driven verification test suite, scripts and other utilities.

For more information on this IP please visit: <http://www.elfinichips.com/ips/DDR2-SDRAM-VIP.html>

Reed Solomon Design IP

The Reed Solomon Encoder (RS Encoder) accepts k blocks of symbols and generates n blocks of code words. n-k symbols are the parity. The number of errors that can be corrected for the parity generated by the RS encoder with defined n and k is given by t, where 2t = n - k. The core has been verified through extensive simulations, direct testing and code coverage measurements.

The RS Encoder accepts data serially and in bursts. It supports any primitive polynomial; user defined generated polynomial, shortened RS codes and has low latency output

The symbol width range of the core is 3-31 bits while the code symbol range is 4-231 symbols with parity up to 999 symbols. Its simple interface allows easy integration into larger systems.

Deliverables:



Deliverables include completely verified RTL code (Verilog), synthesis scripts, timing constraints, design specs and user guide.

For more information on this IP please visit: <http://www.elfochips.com/ips/Reed-Solomon-Encoder-DIP.html>

Support & Availability:

elfochips provides regular product updates and expert consultation to its esteemed customers. Our verification experts are available round the clock to meet all customer requirements related to integrating verification components into their test environment and to meet all other support related issues.

DDR2 SDRAM verification IP and Reed Solomon Encoder design IP are now available from elfochips. For pricing details write to us at sales@elfochips.com

About elfochips

elfochips is a leading provider of ASIC/SoC design & verification services, product development services, IP cores and software product development solutions & services. elfochips has contributed to over 150 chip designs in automotive, consumer, semiconductor, avionics, networking and communication segments through its wide array of RTL to GDS II services and solutions. The company's design centers have delivered SoC and product design solutions to a variety of customer's thus increasing cost-effectiveness, reducing time-to-market and growing their market strength.

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