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DaVinci-HD – The answer to building High Definition Systems

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Introduction:

The eternal question while designing a DSP System has been “Which one is the best choice – ASIC, FPGA, or DSP?” The choice is not just about processing power, since the flexibility and the time to market play an important role in this decision. High quality video transmission is creating challenges to designers and this article tries to address how new generation chips address these challenges.

What DSP Systems are about:

Typical applications of any multimedia (audio-video) application are

1. Reception of multimedia data over network or input video/audio ports
2. Pre-processing of input data (if analog audio-video inputs)
3. De-multiplexing different transport containers (RTP, MPEG-2TS, 3GP, QTFF etc) to extract elementary audio-video streams for decoder application
4. Encoding/Decoding of video/audio streams (raw/compressed) with required audio-video codec
5. Post-processing of encoder/decoder output data

Each of these tasks consume high CPU cycles but need different instruction set architectures (ISA) in order to hit real time performance. For example, the data path (instruction sets) required for extracting an audio/video stream is totally different from that of a signal processing operation (convolution/filtering operation). This makes it highly desired to have different sub system/core supporting different data paths optimized for specific jobs needed in multimedia applications. New generation high performance media SoCs (System on Chip) incorporate such needs by having different sub systems for different tasks, something like having a RISC for OS/application control flow and a DSP with h/w acceleration for encode/decode/signal processing operations. These sub-systems are highly optimized in terms of data path for specific

multimedia task (an advantage equivalent to having an ASIC for a particular task) which results in effective task level pipelining and increase in overall system performance.

Why Video Encoding isn't as simple as it sounds:

Video encoding and transcoding still are video chip designers' biggest challenge due to very high computation complexity and data bandwidth requirements. This challenge gets compounded by a plethora of video standards and ever-increasing consumer demand for better quality through HD proliferation.

It is a challenge to achieve real time performance for encode/decode using single DSP having general instruction sets for complex compression standards like H.264/VC-1, more so in the case of HD video. Only highly optimized h/w accelerators which offload different modules of compression standards (like context adaptive bit stream code/decode, quantization, inverse-quantization, DCT, iDCT, motion compensation, motion estimation and inloop-filtering) which require high CPU processing power from DSP can enable the system to achieve real time processing. These h/w modules run in parallel with DSP core effectively pipelining different tasks (like parsing, DCT, ME, MC etc.) which result in very high h/w module throughput.

How things used to be done:

Due to high processing power requirements, typically HD video encoding was performed using custom ASICs or FPGAs. Custom ASICs used to offer good processing capability at lower power. However, the fixed costs were so high that the sale volumes were not enough to bring down the price. The result was designers supporting only one standard. Typically, there are lot of ASICs for MPEG2 compression which had been quite popular for DVD players and movies.

This approach became obsolete with compression standards moving to H.264, MPEG4 or VC-1. Supporting multiple codecs became necessary for survival. This is when the industry moved to FPGAs or high speed or multi-core DSPs. FPGAs offer high performance, but come with a cost, design time and power consumption penalty. Multi-core and high speed DSPs also offered the same bundle of performance at higher cost and power consumption.

Solutions	Performance	Cost	Power	Flexibility	Time to Market
Custom ASIC	High	Low	Low	Low	High
FPGA	Medium	High	High	High	High
Single Core DSP (Multiple Chips)	Low	High	High	High	High
Multi Core DSPs	High	High	High	High	Medium

Media Processor w/ HW Accelerator	High	Low	Low	High	Low
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What New Generation Chips bring in:

New generation chips are built to address three basic concerns of designers:

1. Easy programmability so as to support multiple compression standards
2. Lower cost and lower power consumption
3. Very high processing power, so as to have headroom for other DSP functions like Video Analytics apart from encoding

The new generation chips take advantage of both the DSP world and ASIC / FPGA world. They use hardware accelerators which perform parallel signal processing tasks as compared to traditional sequential software processing in DSP.

The new chips contain three major blocks:

1. Hardware accelerators
2. Control processor
3. DSP Core

With re-usable modules allowing simultaneous development, these chips provide faster time to market at lower cost.

The DaVinci-HD:

DaVinci-HD DM6467™ processor (from Texas Instruments) is a very high performance media SoC which is highly customized for HD video application. The HD performance makes the SoC very suitable in equipments handling HD H.264/VC-1 video such as HD broadcast, HD video transcode, multi channel SD video encode and decode.

Chip features:

- Single chip solution implementing multiple sub-systems tuned for real time, multi-format, HD video performance.
- Based on an ARM926EJ-S core, TMS320C64x+™ DSP core and HD video/imaging coprocessor.

- The HD-VICP is optimized for multi-format transcoding and provides 720p/1080i MPEG-2, H.264, VC-1, MPEG-4 encode/decode.

Performance:

The DM6467™ SoC is designed to address the HD transcoding challenge for commercial and consumer markets. It supports multi format HD video (720p @ 60Hz, 1080i @ 60 Hz, 1080p @ 30 Hz) decode/encode, simultaneous multi channel, multi-format SD video decode and encode. For example, it can handle simultaneous 4-channel D1 resolution H.264 Main Profile @ 30 Hz video encode, 4xCIF H.264 Baseline Profile @ 30 Hz video encode and some video analytics application.

The Best of All Worlds:

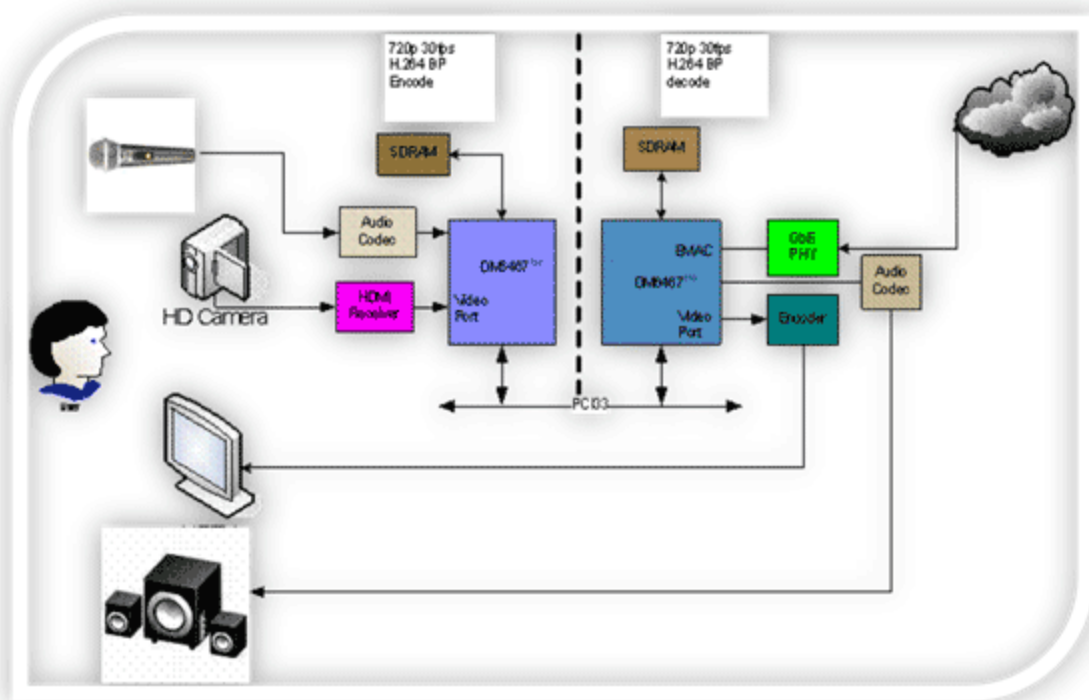


Figure: 720p video conferencing system based on two DM6467™ SoCs

Cost, power consumption and performance advantages:

The DM6467™ is available at 1/10 the cost of previous application system while addressing multiple formats HD video encode and decode. As the overall functionality is performed within single chip, overall power consumption comes down by a factor of four. Same form factor boards can accommodate more number of DSPs to support multi-channel video encode / decode and transcode applications.

About eInfochips:

eInfochips is a leading spec to silicon to system services company with expertise in ASIC/SoC design & verification, electronics product realization, IP cores and Software Product development.

eInfochips has significant experience in the field of video, audio and multimedia delivery over the IP network. The company is offering solutions around Texas Instruments' DaVinci™ technology. Texas Instrument (TI) is an industry leader in innovative DSP solutions.

As a premier Third Party Network member, eInfochips is already engaged with customers on DaVinci-HD based designs and will shortly come out with solutions around DaVinci-HD to enable faster development of products for the customers.

