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eInfochips announces MIPI System Verilog Verification IP

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By VARIndia Correspondent

eInfochips, Inc. has announced the availability of CSI-2 (Camera Serial Interface Version 1.00) & D-PHY 0.85.00 compliant MIPI SystemVerilog verification component.

eInfochips' SystemVerilog MIPI verification component is based on a layered object-oriented architecture that allows coverage driven system level verification suitable for verification of MIPI transmitter or receiver DUT (Design Under Test).

The MIPI (Mobile Industry Processor Interface) SystemVerilog VIP generates High Speed, Escape-LPDT, Escape-ULPS and Escape Trigger modes of data traffic with various formats on virtual channels for multiple data lanes. It has support for error injections and detections for ECC, Synchronization, CRC, Payload and Unrecognized ID detection with an FSM based protocol checker. MIPI Monitor uses SystemVerilog assertion to check for timing violations, if any, at the DPHY interface. Functional coverage mechanism helps determine uncovered configuration variables. MIPI VIP is highly configurable for primary images data formats, number of images (maximum 4), number of lines in the image, number of data-lanes and interleaved image transfers.

Deliverables include completely verified verification component encrypted code, user guide, release notes and sample test cases. eInfochips' IP support staff meet customer requirements related to integrating IP into test environment and other support related issues

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