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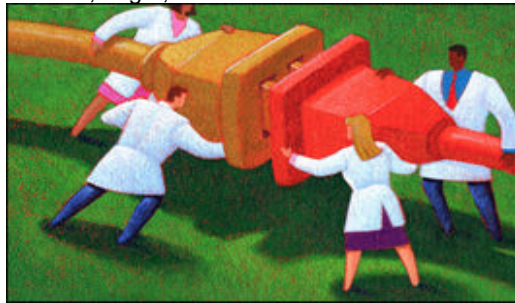
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MIPI SystemVerilog VIP from eInfochip

By [CXOtoday Staff](#)
Mumbai, Aug 4, 2008



eInfochip has announced the availability of CSI-2 (Camera Serial Interface Version 1.00) and D-PHY 0.85.00 compliant Mobile Industry Processor Interface (MIPI) SystemVerilog verification component.

This verification component is based on a layered-object oriented architecture. It allows coverage driven system level

verification. It is suitable for verification of MIPI transmitter or receiver Design Under Test (DUT).

The MIPI SystemVerilog VIP generates escape-LPDT, escape-ULPS and escape trigger modes of data traffic with various formats on virtual channels for multiple data lanes.

It also supports error injections and detections for ECC, synchronization, CRC, payload and unrecognized ID detection with an FSM based protocol checker. It can be configured for primary image data formats, number of images (maximum 4), number of lines in the image, number of data-lanes and interleaved image transfers.

Related links:

[EInfochip Unveils IPNetCam](#)

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