

[PRINT](#)

Article Title: eInfochips' SPI4.2 and CCIR656 design IPs

SUNNYVALE, USA & AHMEDABAD, INDIA: [eInfochips Inc.](#) has announced the availability of OIF (Optical Internetworking forum) compliant SPI4.2 design IP (System packet interface Level 4 Phase 2) and ITU-R BT 601 and ITU-R BT 656 compliant CCIR 656 stream generator design IP.

eInfochips' SPI4.2 Design IP is a highly configurable and efficient implementation that can be used for high speed networking interfaces where queuing, scheduling, arbitration and credit management is done outside the SPI 4.2 IP core.

eInfochips' CCIR656 design IP provides video interface for display controller ICs and supports 525 and 625 line interlaced TV display. It may be used for digital surveillance systems, digital cameras and advanced mobile phones with video capabilities.

"[eInfochips](#) SPI4.2 and CCIR 656 stream generator design IPs, are important additions to our ever increasing portfolio of high speed bus protocol and video processor core IPs," said Nirav Shah, Director of Marketing at eInfochips. "These IP cores are thoroughly verified, highly scalable, easily integrable and standards compliant and would enable our customers to greatly reduce their networking interfaces and video surveillance equipment chip development time and costs."

SPI4.2 design IP

SPI4.2 design IP has a 64-bit user logic interface and a fully configurable error reporting and interrupt generation mechanism that supports both interleaved and normal mode of data transfer. It has a bandwidth optimized design capable of scaling up the number of physical ports to 256. Other features include framing error detection, DIP-2 and DIP-4 parity generation with programmable error check.

CCIR656 design IP

CCIR656 design IP accepts YCrCb (4:2:2) color space video input and provides a parallel 8-bit BT 656 video stream output. This IP supports the NTSC system with 525 lines and 720x487i resolution and PAL system with 625 lines and 720x576i resolutions.

The core is designed for efficient implementation on FPGA and

ASIC. The device utilization of CCIR656 IP on Spartan 3E 1200 k gates is 1 percent and operating frequency is 27 MHz. This core has been verified through extensive simulations, direct testing and code coverage measurements.

Availability and deliverables

Deliverables include completely verified RTL code (Verilog), synthesis scripts, timing constraints, design specs and user guide. eInfochips' IP support staff meet customer requirements related to integrating IP into test environment and other support related issues. SPI4.2 and CCIR656 video stream generator design IPs are now available from eInfochips.

Copyright (c) 2007 [CyberMedia India Online Ltd](#) . All rights reserved. Additional reproduction in whole or in part or in any form or medium without express written permission of CIOL is prohibited.

Send your questions to webmasterciol@cybermedia.co.in

PRINT

[Close this window](#)