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India's eInfochip rolls two design IP cores

[K.C. Krishnadas](#)

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BENGALURU, India — Design services provider eInfochips Ltd. has launched two design IP cores designed to reduce networking interfaces and video surveillance chip development time and cost.

The new IP cores emerged a month after the company announced [verification cores](#). They will supplement an increasing portfolio of high-speed bus protocol and video processor cores.

The new IP cores comply with the Optical Internetworking Forum's SPI4.2 design IP (System Packet Interface Level 4, Phase 2) and other ITU specs. EInfochips (Ahmedabad, India) claimed the SPI4.2 design IP is a configurable implementation for use in high-speed networking interfaces where queuing, scheduling, arbitration and credit management are handled outside the SPI 4.2 IP core.

The CCIR656 design IP provides a video interface for display controller ICs and supports 525- and 625-line interlaced TV displays used for digital surveillance systems, digital cameras and advanced mobile phones with video capabilities. It can be implemented on an FPGA or ASIC, the company said.

The cores include verified RTL code (Verilog), synthesis scripts, timing constraints and design specs, said Nirav Shah, eInfochips' marketing director.

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