Dealing with IR drop issues in Nanometer technology

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Due to Very-Deep-Submicron (VDSM) technology evolution the semiconductor industry is facing exciting new challenges all the time. As minimum layout dimensions continue to shrink and the number of functions that can be put on a SOC continues to grow, creating signal integrity as a major issue causing chip failures. These nanometer effects void the estimations in conventional timing analysis, creating a major difference in predicted performance and silicon results.

Nanometer-design timing analysis requires a comprehensive subflow that accounts for the interactions of IR-drop and signal-integrity effects on timing, based on accurate parasitic data and detailed models. Tools such as Voltage Storm, CeltIC NDC, and Fire & Ice QX combine accurate parasitic extraction, advanced models, and simultaneous analysis of the effects of IR drop and signal integrity on timing before tape-out.

IR DROP

IR drop is a signal integrity effect caused by wire resistance and current drawn off from the power and ground grids. If the wire resistance is too high or the cell current larger than predicted, an unacceptable voltage drop may occur. Nanometer designs are extremely susceptible to IR drop because power and ground wire resistivity increases with decreasing geometries, while the overall power supply voltage decreases. This results in poor performance and increased noise susceptibility. Furthermore, gates with different voltage levels communicating with each other across the chip can propagate erroneous data, causing a malfunction.

Gate delays increase non-linearly as voltage at gates decrease. This may lead to setup or hold timing violations depending on which path these gates are residing. The increase in gate delay due to IR-drop on the data path can ultimately lead to setup timing violations. On the contrary, the voltage drop on the buffers and inverter cells of the clock path will cause the delay in arrival of clock signal, resulting in a hold violation.

Due to IR-drop and signal-integrity effects, the traditional analysis methods are proving inaccurate. For example, conventional power-analysis methods have typically relied on a single derating factor to determine IR-drop effects in a design. Engineers often derate global drain-to-drain voltage by 2 to 5% and rerun the delay calculation, but this approach applies the same supply voltage to all instances in a design and typically provides an overoptimistic view of results. In fact, the impact of IR drop on timing is nonlinear with supply voltage. As a result, the use of static- timing analysis with simple linear derated power cannot correctly identify setup- and-hold-time violations that IR drop- related delay variations cause.

Some Tips to deal with IR Drop issues

1. Proper power-planning:
Ensure uniform power distribution throughout the chip area is the key to have minimum IR drop in the design. Provide reasonable number of horizontal as well as vertical power stripes with appropriate width in the design.

2. Increase the width of the power stripes:
This will help in decreasing the resistance in the path and hence the voltage drop. But this will reduce the routing resource in the design. Apply this option only if you have enough routing resources.

3. Perform pre-layout signal integrity analysis:
In conventional IC design flows signal integrity analysis is performed as a post-layout activity. Unfortunately, this is the wrong time to be analyzing for signal integrity effects. After doing floor planning

perform IR-drop analysis to make sure that your power planning is not giving you large IR-drop in the design. If you get dissatisfying result, do power planning again and make sure that power is distributed uniformly throughout the design. You can also go for multiple VDD pins such that the chip will get power supply from each side.

4. Provide extra power stripes:
In the region that experience large IR-drop provide extra power strips.

5. Setup positive slack:
Try to achieve sensible positive slack(Setup margin) at the end of your final routing stage to make sure that final the design will not violate setup timing even if there is slight delay due to IR drop.