

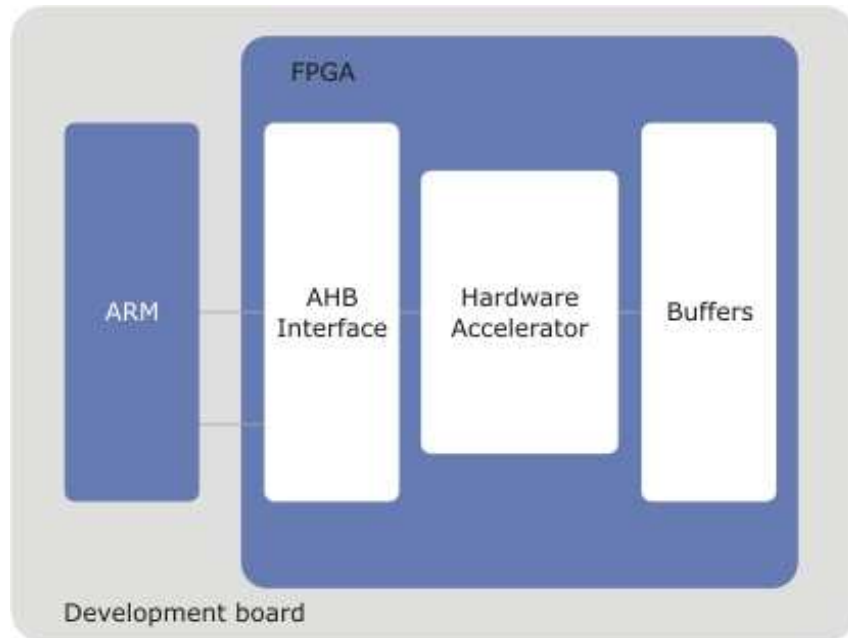
Hardware Acceleration for Video Processing applications

Overview:

Our customer is leading company offering solutions for electronic, biomedical and information technology domains. The project included implementation of H.264 protocol for video applications.

Project Overview:

Implementation of silicon IP H.264 codec was targeted for video applications on mobile devices. Few functional blocks were implemented as software algorithms. Hardware acceleration was done for most of the functional blocks for achieving the desired performance. The complete system was validated on ARM development kit. The kit included baseboard, FPGA daughter board and Core tile daughter board. The hardware accelerators were burned in the FPGA and two parallel running processors controls the operation of the hardware accelerators.



Block Diagram

eInfochips' Role:

Design:

- RTL design of glue logic for integration

Verification:

- Verification environment and test case development for De-blocking filter module.
- Verification environment and test case development for Transform Quantizer module.

- Verification environment and test case development for Motion estimation module.
 - Verification environment and test case development for Interpolation sub-module
- Combined system level verification, environment verification and test case development for all modules.

Board bring-up:

- Synthesis
- Timing Closure
- Integration of software with board

Benefits:

The project was a resounding success. The major benefits to the customer were:

- eInfochips team served as a one-stop solution for the complete design, verification and board bring-up
- Time to market