

OVM Ready I2C Verification Component Overview

The I2C (Inter-Integrated Circuit) Bus is a two-wire, low to medium speed, communication bus (a path for electronic signals) developed by Philips Semiconductors. The bus provides a communication link between integrated circuits. Its applications include volume and contrast control in radios and televisions.

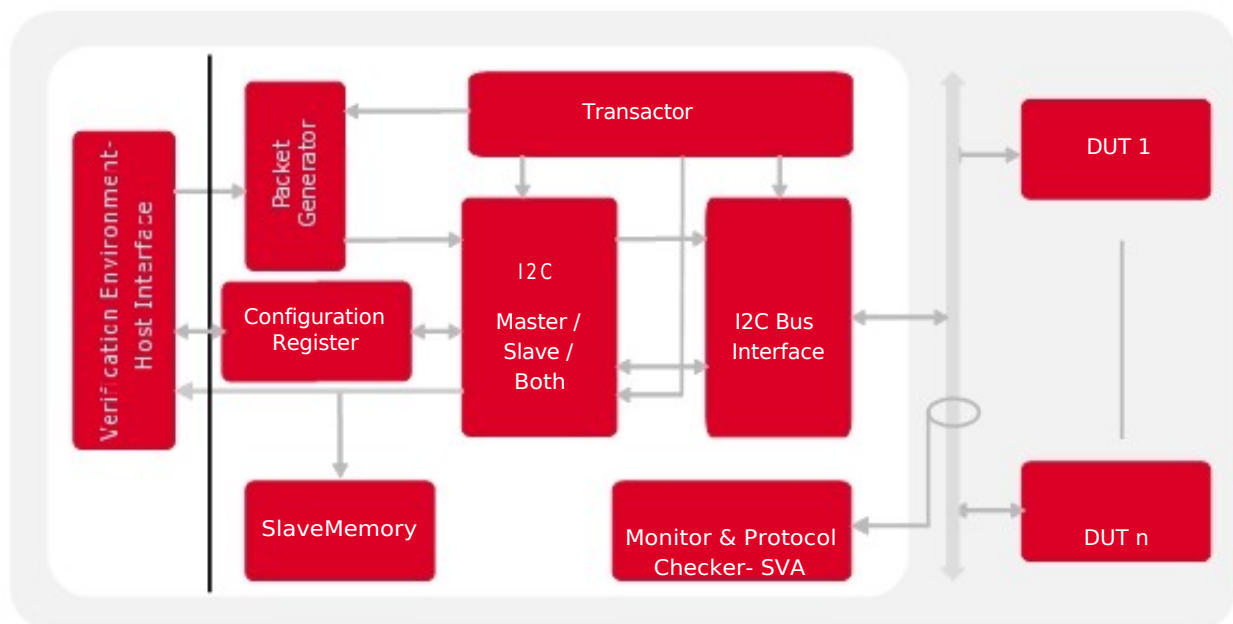
Infochips' OVM Ready I2C Verification IP is fully compliant with version 2.1 of the Philips I2C-Bus Specification and provides the following features:

- Supports standard, fast, and high speed operations. The model has a rich set of configuration parameters to set clock synchronization and generation of the Serial Clock Line (SCL) to meet all clocking requirements.
- Detects and notifies the testbench of all protocol errors.
- Contains many configurable features including the SCL's period and duty cycle, slave addresses, transfer abort, command retries, and data FIFO depths.
- Significant model events trigger the testbench through the use of notifications.

Infochips' OVM Ready I2C Verification Component is based on reusable methodology that allows coverage driven verification suitable for verifying Master, Slave and AHB bus with various combinations as the DUT.

Application

A DUT with an I2C interface can be verified with a single I2C SystemVerilog VC, configured appropriately. I2C SystemVerilog VC is fully configurable and easy to use for both module and system-level verification. It can be configured to emulate a single master or single slave device. It can also emulate the entire I2C bus system with multiple devices.



Functional Description

Conceptual Component	Elements	Purpose
Monitor	Bus Monitor <ul style="list-style-type: none"> • Protocol Checker • SystemVerilog Assertions 	SystemVerilog assertions interface
Transactor	<ul style="list-style-type: none"> • Master & Slave • Slave • Transactor 	Emulates the I2C agent that generates and drives data on bus. Functional Coverage to transactor component

Protocol checker and SystemVerilog Assertions can be plugged in or out without affecting the SystemVerilog I2C Verification Component functionalities. The SystemVerilog Verification component can work in both Verilog & VHDL environment and works with all HDL simulators that are supported in SystemVerilog.

Features

- Supports I2C bus specification version 2.1
- I2C device types implemented: MASTER - SLAVE
- General Call address handling
- Support for 7-bit and 10-bit addressing
- Speed modes supported: Standard mode (SS), and Fastmode (FS)
- Full control over bus transactions generation
- Error injection
- Scoreboard checking supported
- Detects and reports errors like
 - Invalid Slave Address
 - Invalid Data
 - Give Acknowledge Error
 - Create Collision
 - Invalid start
 - SystemVerilog Assertion at interface
 - Built in global bus monitor for protocol checking
 - Built in coverage analysis for all packet types
 - Directed-random test generation
 - HDL independent

Compatibility and Support

Deliverables

- Fully verified, encrypted I2C OVM Ready SystemVerilog code
- Test suites
- Documentation User's Guide, Release notes

eInfochips' support and maintenance services provide customer's with product updates. eInfochips' OVM Ready VCs are developed and supported by experts in reuse, verification and networking, who are available, round the clock on email to meet your requirements related to integrating OVM Ready VCs into your test environment.



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