The Effect of Memory Usage on Power consumption!

The accurate estimation of power for Processor based complex SoC design is the major challenge as it is important to plan the power distribution structure in Physical layout design. CMOS devices ideally draw current only when switching, thus it gives fully static devices with some idle modes and so very low current drain. This unique property of CMOS leads to low power portable, power-sensitive and battery-operated applications.

The Basic

The voltage change on a gate capacitance requires transfer of charge and therefore causes power consumption. Once the gate capacitance is charged, the gate can maintain a DC voltage level without any additional charge movement and does not consume current. The required charge to change voltage levels on the gate is
Q = C x VDD where,
Q is the charge required to change states (coulombs)
VDD is the power supply voltage (volts)
C is the gate capacitance (farads)

So continuous switching causes current proportional to the switching frequency. Since current is defined in terms of coulombs per second (amperes), the current can be calculated as,
I = Q × frequency = C × VDD × frequency where,
I is the current in amperes (coulombs per second)
Power = VI = C x VDD2 x f

The same approach can be applied to calculate the power dissipation of the chip. But knowing the capacitance of all of the internal switching nodes is really a time consuming task. The total power dissipation depends on internal operation as well as external bus cycles and the loads associated with the external buses. So the best way, to calculate the total power consumption, is calculating the power in known conditions based on the device activity, external load and IO circuitry etc.

Memory Power Consumption

The total power of any processor based SoC designs depends on CPU power and memory power. During layout phase, the power structure and wire width are decided based on the power consumption of the design. When we calculate the peak power for layout power structure, the understanding of power consumption of memories adds more accuracy in determining the power width. Using on-chip memory reduces system cost and power compare to external memory. The on-chip ROM (read-only memory) can be used as program memory or to store fixed data, which are never altered. The clear understanding of memory access from both internal/external memories is important in case power estimation. The different types of on-chip memory also exhibit different power characteristics for the same functions. On-chip memory requires less power because the external memory interface is not driven during internal accesses. Minimizing accesses to external memory space lowers the device current requirement. Use of internal ROM requires less power than use of internal RAM. Code execution from internal ROM requires about 10% less CPU current than the same code executing from internal single access RAM. Memory accesses to dual access RAM require approximately 4% less current than identical accesses to single access RAM. Memory accesses to ROM require approximately 10% less current than identical accesses to single access RAM.

Data Buses

Data buses are routed as a set of connections together. Each of these lines has a characteristic capacitance with respect to the silicon substrate on which they are fabricated. Since these bus lines frequently are routed adjacent to each other, they also possess an inter-signal capacitance, or a capacitance between the adjacent bus lines. When the voltage on a bus line changes, these capacitances also become charged and discharged as described previously. Since some of these capacitances exist between signal lines, the necessity to charge or discharge depends on the voltage levels on both lines. Therefore, the data patterns on the bus affect how many of these characteristic capacitances must charge, and consequently, affect the total device current. For this reason, driving a bus with an alternating pattern of AAAAh/5555h consumes more current than driving 0000h/FFFFh. In both cases, all 16 lines are switching so the current contribution due to each line s capacitance with respect to the silicon substrate is the same. So considering the worst-case situation to estimate the power consumed in such activities will add more accuracy affront to the layout phase. External buses have greater intrinsic capacitance than internal buses because of the nature of the packaging and the presence of high-output current drivers for the pins. External buses also experience the load of the other external devices to which they are connected. More capacitance results in high current.

Address buses

The address bus uses a similar amount of current as the data bus. If branches occur where many address lines change, the instantaneous current increases accordingly.

The total power can be calculated as

$I = (I_{int} + I_{addr} + I_{data} + I_{cntl}) \times VS \times T$ Where,

I is the total IDD supply current I_{int} is the current component due to all internal circuitry

I_{addr} is the current component due to external address bus activity

I_{data} is the current component due to external data bus activity

I_{cntl} is the current component due to external control line activity

VS is a scale factor due to supply voltage

T is a scale factor due to operating temperature.

Apart from CPU power and external load power, the memory power consumption plays a major role in total power of a chip. During Power estimation of the chip as well as to estimate the wire width, the accurate analysis of memory power is important to avoid Electromigration, IR drop kind of issues.