

Shrinking ASIC Library Cells

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Introduction:

A library strategy has been developed to enable ASIC development to keep pace with rapid technology enhancements and to offer leading-edge performance to ASIC customers. Library elements are designed using migratable design rules to allow designs to be reused in future advanced technologies; and library contents, design methodology, test methodology, and packaging offerings for the ASICs also are consistent between current and future technologies.

The benefit to the ASIC customer is an ASIC with a rich library of logic functions, arrays, and I/Os for today's designs, and with a ready migration path into future designs. Requirements of this market have stimulated a new strategy for creating ASIC libraries that emphasizes consistency with industry standards, and efficient migration of customer designs to future generations of technology. By using a migration strategy which emphasizes reuse of library elements, the ASIC developer can deliver new technologies to customers with minimized time and resources.

Types of Library cells:

There are two types of library cells:

1. Standard Cells

- The layouts of standard-cell elements are customized on both the diffused layers and the metallization layers.
- Each standard cell in the library is constructed using full-custom design methods, but you can use these pre-designed and pre-characterized circuits without having to do any full-custom design yourself i.e. in a semi custom ASICs. This design style gives you the same performance and flexibility advantages of a full-custom ASIC but reduces design time and reduces risk.

2. Gate array based cells

- Gate-array elements are customized only on the metallization layers.
- The transistors formed by the diffusion and poly-silicon layers are the standard templates for all gate-array cells. Only the metallization layers interconnecting the transistors are unique for this function.
- The availability of local interconnect allows this cell to leave many metal-1 tracks open for global routing

❖ **Shrinking Library cells:**

Importance of Shrinking Library cells:

Consider this example,

The present generation of IBM ASIC products was designed in the IBM 0.4-micron CMOS 5S and 0.35-micron CMOS 5X technologies, with anticipated migration to 0.25- μ m CMOS 6S technology and beyond. The layout design rules for the CMOS 5S and CMOS 5X technologies are not identical. However, a common set of migratable design rules (MDRs) were defined which encompass the layout restrictions of both technologies. Circuits laid out to the MDRs are then transportable between the technologies without modification.

The common features of the CMOS process technology, and the use of MDRs, allow layouts for CMOS 6 and beyond to be created from CMOS 5 layouts by scaling down the lithographic dimensions. This reduces the design time, saves the cost and allows reusability.

This is how we may shrink Library cells to a given size and accommodate it in a fixed pad using layout editor tools:

- Check the layout against the design rules with the help of the DRC tool
- Use schematic entry method and pass functionality with the LVS tool.
- The library conversion is particularly done on the existing proven library with specific grid.
- The idea behind converting library is to shrink the existing library cells of 91.45x945 micron 1x6 pad structure so that they can be sized and merged into the 50x1080 micron 1x12 pad structure.
- The shrinking is done such that it there is no violation of DRC's and that it passes the connectivity defined in schematic.
- The verification is done on each cell through schematic extraction and the cell is then passed through LVS (Layout Vs schematic match).

Challenges:

During the process of conversion and shrinking the biggest challenge is to pass LVS. Success in passing LVS says that your layout matches with the functionality. Layout generation is time-consuming and difficult to debug in case it is done by faultily managing the spacing.