

TMDXEVM6472

Technical Reference Manual

Version 1.2

Literature Number: SPRUFU2
Revised February 2010



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Publication Title:

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Preface

About this Document

This document is the Technical Reference Manual for the TMS320C6472 Evaluation Module (EVM) developed by elnfochips for Texas Instruments.

Notational Conventions

This document uses the following conventions:

Program listings, program examples, and interactive displays are shown in a mono-spaced font. Examples use **bold** for emphasis, and interactive displays use bold to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Square brackets ([and]) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets. Unless the square brackets are in a bold typeface, do not enter the brackets themselves.

Underlined, italicized non-bold text in a command is used to mark place holder text that should be replaced by the appropriate value for the user's configuration.

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Document Revision History

| Release | Chapter | Description of Change |
|---------|-------------|--|
| 1.0 | All | First Issue |
| 1.1 | | Added Document Revision History |
| | Chapter 1.2 | Block Diagram revised |
| | Chapter 2.7 | Changes due to new ethernet PHY 88E1145 |
| | Chapter 3.1 | Change in board layout Revised AMC edge connections at connector J2 |
| 1.2 | All | Updated after TI's review |

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1. Overview

This chapter provides an overview of the TMDXEVM6472 along with the key features and block diagram.

- 1.1 Key Features
- 1.2 Functional Overview
- 1.3 Basic Operation
- 1.4 Configuration Switch Settings
- 1.5 Power Supply

1.1 Key Features

The TMDXEVM6472 is a high performance, standalone development platform that enables users to evaluate and develop applications for the Texas Instruments' TMS320C6472 multicore Digital Signal Processor (DSP). The Evaluation Module (EVM) also serves as a hardware reference design platform for the TMS320C6472 DSP. The EVM's form-factor is equivalent to a single-width AMC (PICMG's AdvancedTCA Mezzanine Card) module.

Schematics, logic equations and application notes are available to ease the hardware development process and reduce time to market.

The key features of the C6472 EVM are:

- EVM contains Texas Instruments' next-generation six core, fixed point DSP - TMS320C6472. C6472 DSP contains six on-chip C64x+ Megamodules.
- 256 Mbytes of DDR2 Memory
- 128 Mbytes of NAND Flash
- 2 Gigabit Ethernet ports supporting 10/100/1000 Mbps data-rate
- 170 pin B+ style AMC Interface
- I2C EEPROM for boot loading
- 2 user LEDs and 2 user switches
- 8 I2C controlled LEDs
- RS232 Serial port
- Host port interface (HPI) connector
- On Board FPGA (Actel's ProASIC 3) for DSP boot-strapping and NAND Flash interface
- On Board Emulation using High-speed USB interface
- 14-Pin JTAG header for optional external emulator connectivity
- Powered by DC power-brick adaptor (12V/2.5A) or AMC Carrier back-plane

1.2 Functional Overview

The TMDXEVM6472 is a single width AMC module with Texas Instruments' six core C6472 DSP, working as a bridge between circuit switched network (telecom serial interface ports) and packet switched network (Ethernet). Alternatively, it can be used for voice or video transcoding solely through the Ethernet interfaces. Below figure shows the block diagram of TMDXEVM6472.

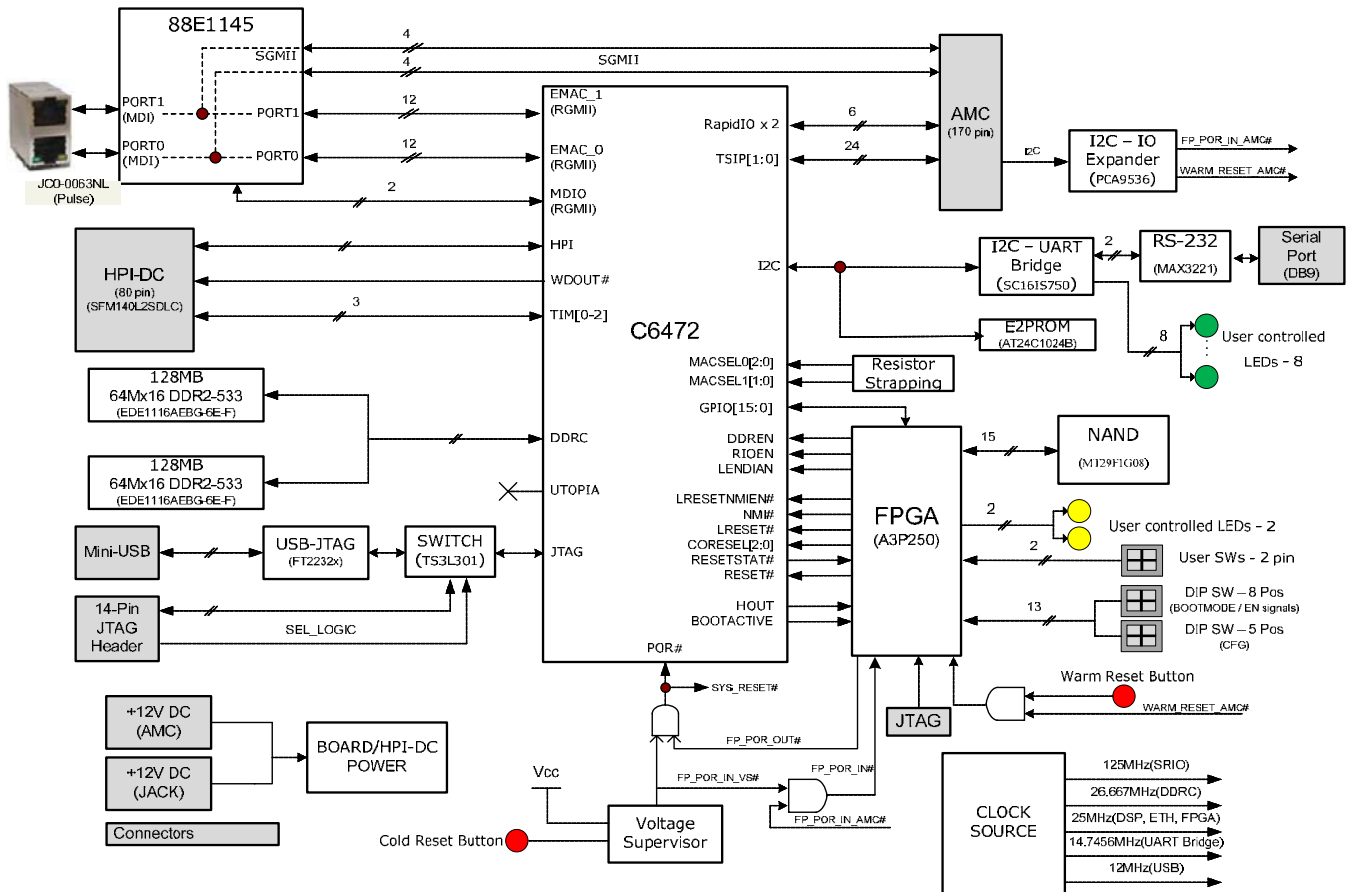


Figure 1.1: Block Diagram of TMDXEVM6472

1.3 Basic Operation

The TMDXEVM6472 platform is designed to work with TI's Code Composer Studio (CCS) development environment and ships with a version specifically tailored for this board. CCS interfaces with the board via on-board emulation circuitry using the USB cable supplied along with this EVM.

To start operating the board, follow instructions in the Quick Start Guide. This process will install all the necessary development tools, drivers and documentation.

After the installation is completed, follow the steps below to run Code Composer Studio.

1. Power ON the board using power brick adaptor (12V/2.5A) supplied along with this EVM or insert this EVM board into standard AMC carrier back-plane.
2. Connect USB cable from host PC to EVM board.
3. Launch Code Composer Studio from host PC by double clicking on its icon at PC desktop.

Detailed information about the EVM including examples and reference material is available in the DVD available with this package.

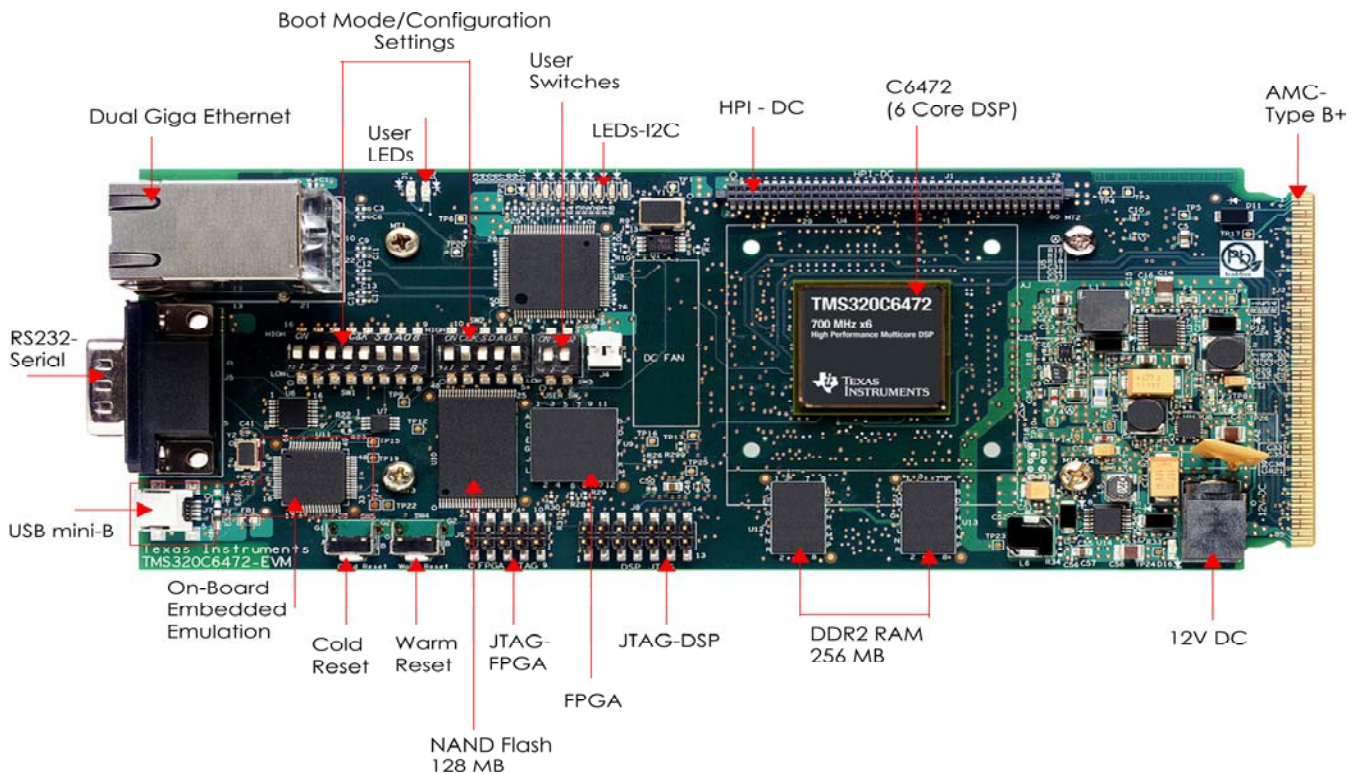


Figure 1.2: TMDXEVM6472*

(*The actual board may look slightly different due to up-gradation)

1.4 Boot Mode and Boot Configuration Switch Setting

The TMDXEVM6472 has 13 sliding DIP switches (Board Ref. SW1 and SW2) to determine boot mode, boot configuration, endian mode, system clock out enable and DDR/SRIO interface enable options at every reset of the DSP.

1.5 Power Supply

The TMDXEVM6472 can be powered from a single +12V / 2.5A DC (30W) external power supply connected to the DC power jack (J6). Internally, +12V input is converted into desired voltage levels such as, +5V, +3.3V, +1.8V, +1.5V and +1.2V using local DC-DC converters.

- +1.2V is used for DSP Core (CVDDx) and Ethernet PHY transceiver.
- +1.5V is used for FPGA core.
- +1.8V is used for DDR2 / Ethernet RGMII interface.
- +3.3V is used for DSP GPIOs.
- +5V is used for DC Fan.
- The DC power jack connector is a 2.5mm barrel-type plug with center-tip as positive polarity.

The TMDXEVM6472 can also draw power from the AMC edge connector (J2). If the board is inserted into an AMC Carrier or AMC-compatible chassis, the external +12V supply from DC jack (J6) is not required and should not be connected in that case.

2. Introduction to the TMDXEVM6472 board

Chapter two provides an introduction and interface details for the TMDXEVM6472 board. It contains:

- 2.1 Memory Map
- 2.2 EVM Boot mode and Boot configuration switch settings
- 2.3 JTAG - Emulation Overview
- 2.4 Clock Domains
- 2.5 I2C Configuration EEPROM
- 2.6 FPGA
- 2.7 Gigabit Ethernet PHY
- 2.8 TSIP Interface
- 2.9 Serial Rapid I/O(SRIO) Interfaces
- 2.10 UART Interfaces

2.1 Memory Map

The memory map of the TMDXEVM6472 device is as shown in Table 1. It provides a combined view of both local and global addresses. The C64x+ Megamodule local memories have both local and global addresses. The Megamodule registers have only local addresses which can be resolved within the Megamodule and cannot be accessed outside Megamodule. All other addresses listed in this table are global addresses which can be accessed from any bus master including all six C64x+ Megamodules, transfer controllers within the EDMA3 block and any peripheral that can master the bus.

Table 1: TMS320C6472 Memory Map

| Six Address Range | Memory Block Description |
|-------------------------|------------------------------|
| 0x 00000000 - 001FFFFFF | Reserved |
| 0x 00200000 - 002BFFFF | SL2 RAM |
| 0x 002C0000 - 007FFFFFF | Reserved |
| 0x 00800000 - 017FFFFFF | Local L1 / L2 SRAM, Reserved |
| 0x 01800000 - 01BFFFFFF | C64x+ Megamodule Registers |
| 0x 01C00000 - 0FFFFFFF | Control Registers, Reserved |
| 0x 10000000 - 1FFFFFFF | Global Memory Map, Reserved |
| 0x 20000000 - 77FFFFFF | Reserved |
| 0x 78000000 - DFFFFFFF | DDR2 EMIF Config, Reserved |
| 0x E0000000 - FFFFFFFF | CE0-CE1 DDR2 SDRAM |

2.2 EVM Boot mode and Boot configuration switch settings

The TMDXEVM6472 has two configuration switches SW1 and SW2. Whenever the user presses a Cold or Warm Reset button or if they power-cycle the board, an on-board FPGA latches the state of configuration signals from SW1 and SW2 and presents them to the DSP during the reset period.

SW1 determines general DSP configuration, little or big endian mode, DDR interface enable and SRIO interface enable. SW2 determines DSP boot mode and system clock out enable options. Please refer [section 3.3](#) of this document for default switch setting and details of each switch.

2.3 JTAG - Emulation Overview

The TMDXEVM6472 has on board embedded JTAG emulation circuitry; hence user does not require any external emulator to connect EVM with Code composer studio. User can connect CCS with target DSP in EVM through USB cable supplied along with this board.

In case user wishes to connect external emulator to EVM, 14-pin JTAG header (J8) is provided on-board for the purpose.

On board embedded JTAG emulator is the default connection to DSP, however when external emulator is connected to EVM, board circuitry switches automatically to give DSP's emulation access to external emulator. When On board emulator and external emulator both are connected at the same time, external emulator has priority and on board emulator is disconnected from DSP.

The interface between DSP, on board and external emulator is shown in figure below.

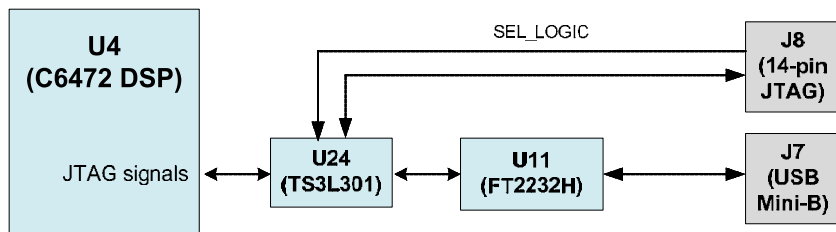


Figure 2.1: C6472 EVM JTAG emulation

2.4 Clock Domains

The EVM incorporates variety of clocks to the TMS320C6472 device which are configured automatically during the power up configuration sequence. The figure below illustrates the clocking for the system in EVM module.

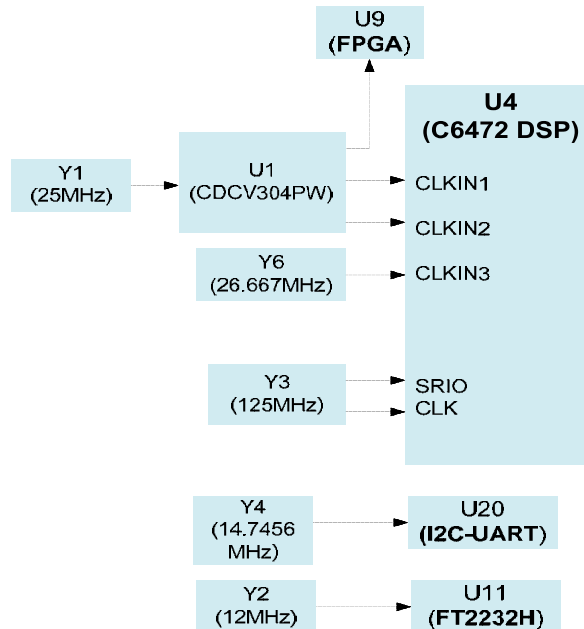


Figure 2.2: C6472 EVM Clock Domains

2.5 I2C Configuration EEPROM

The I2C EEPROM address 0x50 contains Power on Self Test (POST) program and I2C address 0x51 contains second level boot-loader program. The second level boot-loader reads the Out-Of-Box Demo program from the NAND FLASH memory. The I2C address 0x51 also contains two unique MAC addresses reserved for your TMDXEVM6472. These MAC addresses are flashed into the EEPROM at address offset of 0xF400 to 0xF40B.

2.6 FPGA

FPGA (Actel #A3P250-FGG144) controls the reset mechanism of DSP and provided boot mode and boot configuration data to DSP. FPGA also provides interface to 128MB NAND Flash. Nand Flash Controller (NFC) is implemented within FPGA to support below configuration:

- Maximum Density: 1GB
- Data width: 8-bit
- Page size: 2KB
- HW/SW ECC
- 1 bit ECC

Below figure shows interface between TMS320C6472 and FPGA.

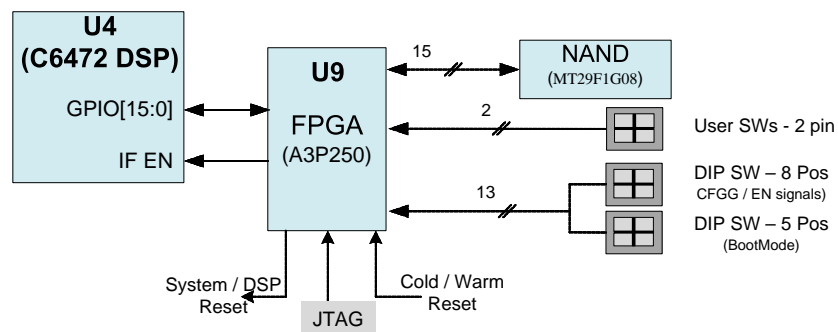


Figure 2.3: C6472 EVM FPGA Connections

2.7 Gigabit Ethernet PHY

The TMDXEVM6472 incorporates a quad-port Marvell 88E1145 Ethernet PHY transceiver. The DSP can configure PHY (U2) over MDIO interface. TMDXEVM6472 is interfaced with PHY as shown in figure below.

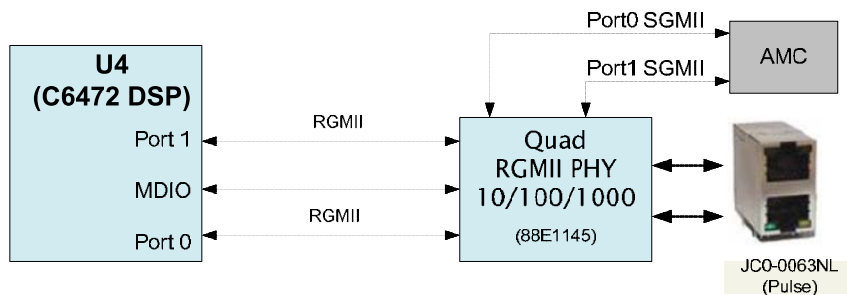


Figure 2.4: C6472 EVM Ethernet PHY Routing

At Power On, Port0 of 88E1145 will be configured as "RGMII to SGMII" mode and Port1 will be "RGMII to Copper" mode. This will be ensured by hardware strapping of 88E1145. After the DSP boot-up, user has the flexibility to change above configuration by re-configuring the drivers. If the board executes the POST program, this program will detect whether the board is installed in an AMC connector and it will configure both EMAC ports to either the AMC connector or to the RJ45 connector.

2.8 TSIP Interfaces

The TMS320C6472 has three independent Telecom Serial Interface Ports (TSIP0:2). The TSIP is a multi-link serial interface consisting of a maximum of eight transmit data signals (or links), eight receive data signals (or links), two frame sync input signals, and two serial clock inputs. The TSIP module in DSP offers support for a maximum of 1024 timeslots for transmit and receive. Typically, 672 timeslots for transmit and receive are utilized on these links. The TSIP module can be configured to use the frame sync signals and the serial clocks as redundant sources for all transmit and receive data signals or one frame sync and serial clock for transmit and the second frame sync and clock for receive.

In TMDXEVM6472, two TSIP ports (TSIP0 and TSIP1) are routed to AMC edge connector. 4 Active links from each of the TSIP0 and TSIP1 ports are routed to AMC edge connector. Below is the interface diagram for TSIP signals in TMDXEVM6472.

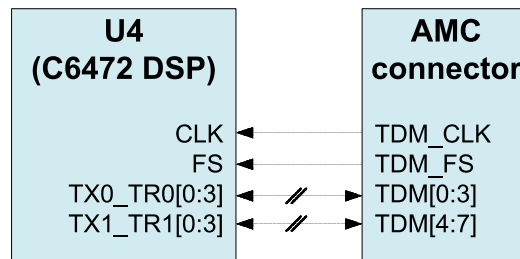


Figure 2.5: C6472 EVM TSIP Connections

2.9 Serial Rapid I/O (SRIO) Interfaces

The TMDXEVM6472 contains high speed SERDES based Serial Rapid I/O (SRIO) interface. Both SRIO ports are taken to AMC edge connector on board. The Figure below shows the SRIO connections between DSP and AMC connector.

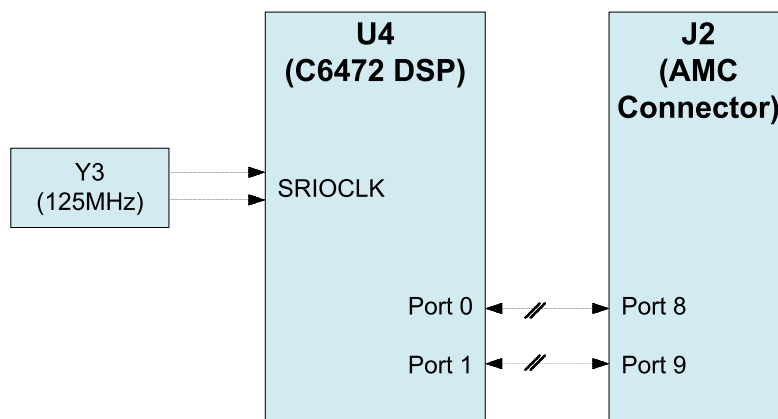


Figure 2.6: C6472 EVM SRIO Port Connections

2.10 UART Interface

The TMDXEVM6472 has UART interface on board. I2C to UART converter bridge is used for the purpose. This UART bridge also contains 8 GPIOs which are used to control 8 LEDs on board. Below figure shows the interface between DSP to UART and DSP to 8 status LEDs.

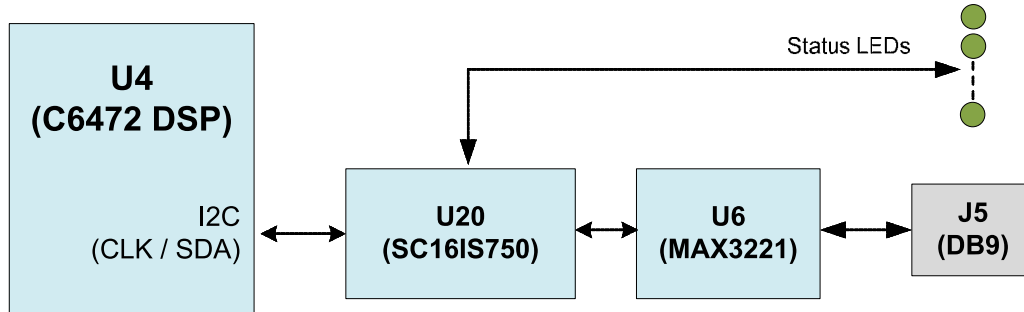


Figure 2.7: C6472 EVM UART Connections

3. TMDXEV6472 Board Physical Specifications

This chapter describes the physical layout of the TMDXEV6472 board and its connectors, switches and test points. It contains:

- 3.1 Board Layout
- 3.2 Connector Index
- 3.3 Switches
- 3.4 Test Points
- 3.5 System LEDs

3.1 Board Layout

The TMDXEV6472 Board is a 7.11" x 2.89" (180.6 x 73.5 mm²) multi-layer board which is powered through connector J6. Figure 3-1 shows the layout of the C6472 EVM Board.

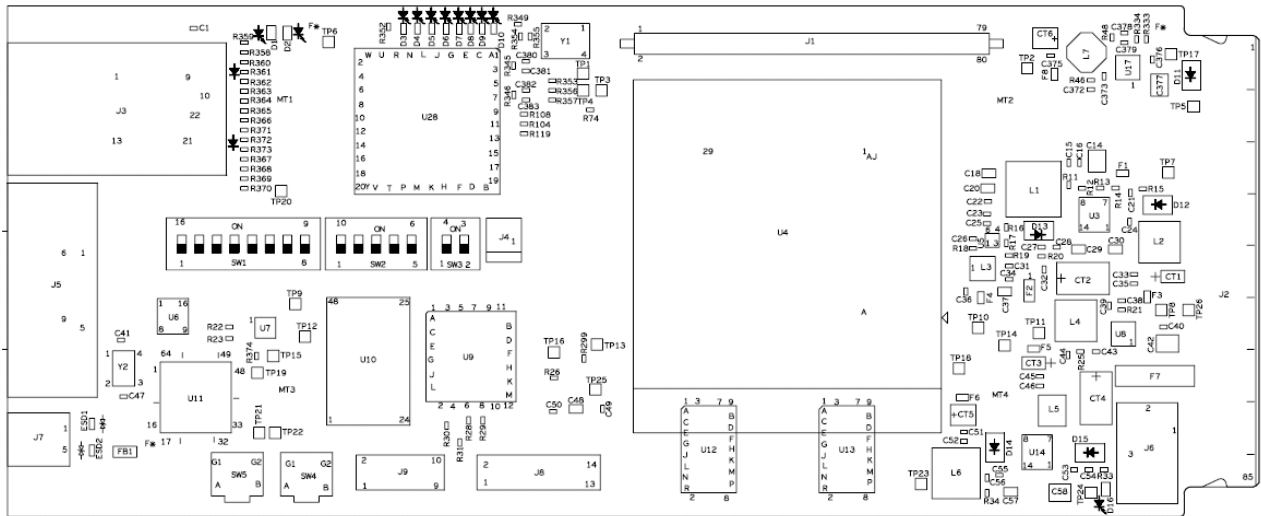


Figure 3.1: C6472 EVM Board layout – TOP view

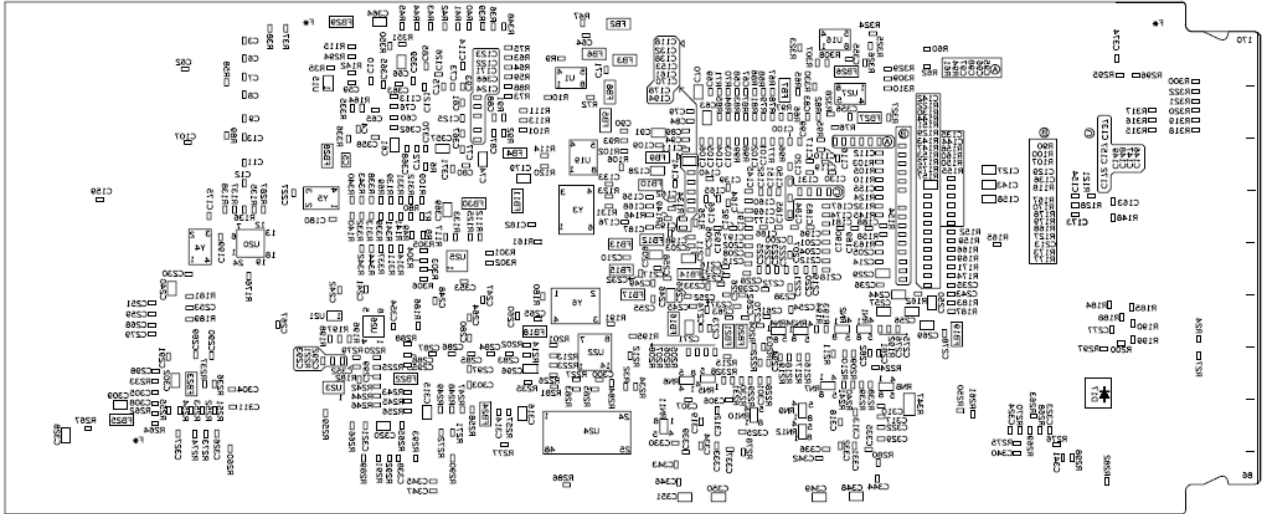


Figure 3.2: C6472 EVM Board layout – Bottom view

3.2 Connector Index

The TMDXEVM6472 Board has several connectors which provide access to various interfaces on the board.

Table 2: TMS320C6472 EVM Board Connectors

| Connector | Pins | Function |
|-----------|------|----------------------------|
| J1 | 80 | HPI DC Connector |
| J2 | 170 | AMC Edge Connector |
| J3 | 28 | Ethernet Connector |
| J4 | 2 | DC Fan Connector |
| J5 | 9 | DB9 Connector |
| J6 | 3 | Power Input Jack Connector |
| J7 | 5 | Mini-USB Connector |
| J8 | 14 | DSP JTAG Connector |
| J9 | 10 | FPGA JTAG Connector |

3.2.1 J1, HPI DC Connector

Connector J1 provides the HPI Interface of the DSP to an external host. The signals on this connector are shown in the table below. This connector is identical to the HPI connector implemented on previous AMC EVMs of TI, so that any previous test fixtures will connect without revision.

Table 3: J1, HPI DC Connector

| Pin | Signal | Description | Pin | Signal | Description |
|-----|-----------|-----------------------|-----|-----------|------------------|
| 1 | VCC5 | +5V Power | 2 | VCC3.3 | +3.3V Power |
| 3 | GND | Ground Signal | 4 | VCC3.3 | +3.3V Power |
| 5 | VCC5 | +5V Power | 6 | VCC1.8 | +1.8V Power |
| 7 | GND | Ground Signal | 8 | GND | Ground Signal |
| 9 | HPI_D1 | Data Signal - 1 | 10 | VCC1.8 | +1.8V Power |
| 11 | HPI_D3 | Data Signal - 3 | 12 | HPI_D0 | Data Signal - 0 |
| 13 | HPI_D5 | Data Signal - 5 | 14 | HPI_D2 | Data Signal - 2 |
| 15 | HPI_D7 | Data Signal - 7 | 16 | HPI_D4 | Data Signal - 4 |
| 17 | GND | Ground Signal | 18 | HPI_D6 | Data Signal - 6 |
| 19 | HPI_D9 | Data Signal - 9 | 20 | GND | Ground Signal |
| 21 | HPI_D11 | Data Signal - 11 | 22 | HPI_D8 | Data Signal - 8 |
| 23 | HPI_D13 | Data Signal - 13 | 24 | HPI_D10 | Data Signal - 10 |
| 25 | HPI_D15 | Data Signal - 15 | 26 | HPI_D12 | Data Signal - 12 |
| 27 | GND | Ground Signal | 28 | HPI_D14 | Data Signal - 14 |
| 29 | HPI_DS2# | Data Strobe - 2 | 30 | GND | Ground Signal |
| 31 | GND | Ground Signal | 32 | HPI_HAS# | |
| 33 | HPI_DS1# | Data Strobe - 1 | 34 | GND | Ground Signal |
| 35 | GND | Ground Signal | 36 | HPI_CNTL0 | Control Select 0 |
| 37 | HPI_CS | Chip Select | 38 | GND | Ground Signal |
| 39 | GND | Ground Signal | 40 | NC | |
| 41 | HPI_CNTL1 | Control Select 1 | 42 | GND | Ground Signal |
| 43 | GND | Ground Signal | 44 | HPI_INT | Interrupt |
| 45 | HPI_RDY# | Ready indication | 46 | GND | Ground Signal |
| 47 | GND | Ground Signal | 48 | NC | |
| 49 | HPI_RW# | Read / Write select | 50 | NC | |
| 51 | NC | | 52 | NC | |
| 53 | NC | | 54 | NC | |
| 55 | NC | | 56 | GND | Ground Signal |
| 57 | NC | | 58 | NC | |
| 59 | NC | | 60 | NC | |
| 61 | GND | Ground Signal | 62 | NC | |
| 63 | NC | | 64 | NC | |
| 65 | NC | | 66 | NC | |
| 67 | NC | | 68 | TIMI0 | Timer Input |
| 69 | NC | | 70 | GND | Ground Signal |
| 71 | GND | Ground Signal | 72 | TIMI1 | Timer Input |
| 73 | WDOUT# | Watchdog timer output | 74 | GND | Ground Signal |
| 75 | GND | Ground Signal | 76 | TIMO2 | Timer Output |
| 77 | HPI_HWIL | Half Word Select | 78 | GND | Ground Signal |
| 79 | GND | Ground Signal | 80 | NC | |

3.2.2 J2, AMC Edge Connector

The J2 card edge connector plugs into an AMC compatible carrier board and provides a high speed Serial Rapid IO, TSIP and I2C interfaces to the carrier board. This connector is the 170 pin B+ style. The signals on this connector are shown in the tables below.

Table 4: J2, AMC Edge Connector

| Pin | Signal | Description | Pin | Signal | Description |
|-----|-------------|----------------|-----|---------|---------------|
| 1 | GND | Ground Signal | 170 | GND | Ground Signal |
| 2 | VCC12 | +12V Power | 169 | NC | |
| 3 | PS1# | Presence 1 | 168 | NC | |
| 4 | MP | +3.3V Power TP | 167 | NC | |
| 5 | NC | | 166 | NC | |
| 6 | NC | | 165 | NC | |
| 7 | GND | Ground Signal | 164 | GND | Ground Signal |
| 8 | NC | | 163 | NC | |
| 9 | VCC12 | +12V Power | 162 | NC | |
| 10 | GND | Ground Signal | 161 | GND | Ground Signal |
| 11 | P0_SG_OUT_P | | 160 | NC | |
| 12 | P0_SG_OUT_M | | 159 | NC | |
| 13 | GND | Ground Signal | 158 | GND | Ground Signal |
| 14 | P0_SG_IN_P | | 157 | NC | |
| 15 | P0_SG_IN_M | | 156 | NC | |
| 16 | GND | Ground Signal | 155 | GND | Ground Signal |
| 17 | NC | | 154 | NC | |
| 18 | VCC12 | +12V Power | 153 | NC | |
| 19 | GND | Ground Signal | 152 | GND | Ground Signal |
| 20 | P1_SG_OUT_P | | 151 | NC | |
| 21 | P1_SG_OUT_M | | 150 | NC | |
| 22 | GND | Ground Signal | 149 | GND | Ground Signal |
| 23 | P1_SG_IN_P | | 148 | NC | |
| 24 | P1_SG_IN_M | | 147 | NC | |
| 25 | GND | Ground Signal | 146 | GND | Ground Signal |
| 26 | NC | | 145 | NC | |
| 27 | VCC12 | +12V Power | 144 | NC | |
| 28 | GND | Ground Signal | 143 | GND | Ground Signal |
| 29 | NC | | 142 | NC | |
| 30 | NC | | 141 | NC | |
| 31 | GND | Ground Signal | 140 | GND | Ground Signal |
| 32 | NC | | 139 | NC | |
| 33 | NC | | 138 | NC | |
| 34 | GND | Ground Signal | 137 | GND | Ground Signal |
| 35 | NC | | 136 | NC | |
| 36 | NC | | 135 | NC | |
| 37 | GND | Ground Signal | 134 | GND | Ground Signal |
| 38 | NC | | 133 | NC | |
| 39 | NC | | 132 | NC | |
| 40 | GND | Ground Signal | 131 | GND | Ground Signal |
| 41 | AMC_DETECT# | | 130 | AMC_SDA | I2C_SDA_ALT |
| 42 | VCC12 | +12V Power | 129 | AMC_SCL | I2C_SCL_ALT |
| 43 | GND | Ground Signal | 128 | GND | Ground Signal |

| | | | | | |
|----|-----------|---------------|-----|----------|----------------|
| 44 | NC | | 127 | NC | |
| 45 | NC | | 126 | NC | |
| 46 | GND | Ground Signal | 125 | GND | Ground Signal |
| 47 | NC | | 124 | TDM_FS | TDM_FS_ALT |
| 48 | NC | | 123 | TDM_CLK | TDM_CLK_ALT |
| 49 | GND | Ground Signal | 122 | GND | Ground Signal |
| 50 | NC | | 121 | TDM7 | TSIP1_TR3 |
| 51 | NC | | 120 | TDM6 | TSIP1_TR2 |
| 52 | GND | Ground Signal | 119 | GND | Ground Signal |
| 53 | NC | | 118 | TDM5 | TSIP1_TR1 |
| 54 | NC | | 117 | TDM4 | TSIP1_TR0 |
| 55 | GND | Ground Signal | 116 | GND | Ground Signal |
| 56 | SCL_IPMB | | 115 | TDM3 | TSIP0_TR3 |
| 57 | VCC12 | +12V Power | 114 | TDM2 | TSIP0_TR2 |
| 58 | GND | Ground Signal | 113 | GND | Ground Signal |
| 59 | NC | | 112 | TDM1 | TSIP0_TR1 |
| 60 | NC | | 111 | TDM0 | TSIP0_TR0 |
| 61 | GND | Ground Signal | 110 | GND | Ground Signal |
| 62 | NC | | 109 | NC | |
| 63 | NC | | 108 | NC | |
| 64 | GND | Ground Signal | 107 | GND | Ground Signal |
| 65 | NC | | 106 | NC | |
| 66 | NC | | 105 | NC | |
| 67 | GND | Ground Signal | 104 | GND | Ground Signal |
| 68 | NC | | 103 | NC | |
| 69 | NC | | 102 | NC | |
| 70 | GND | Ground Signal | 101 | GND | Ground Signal |
| 71 | SDA_IPMB | | 100 | NC | |
| 72 | VCC12 | +12V Power | 99 | NC | |
| 73 | GND | Ground Signal | 98 | GND | Ground Signal |
| 74 | TDM_CLK_P | TSIP Clock A | 97 | RIOTX_P1 | SRIO Port 1-TX |
| 75 | TDM_CLK_N | | 96 | RIOTX_N1 | SRIO Port 1-TX |
| 76 | GND | Ground Signal | 95 | GND | Ground Signal |
| 77 | TDM_FS_P | TSIP Clock B | 94 | RIORX_P1 | SRIO Port 1-RX |
| 78 | TDM_FS_N | | 93 | RIORX_N1 | SRIO Port 1-RX |
| 79 | GND | Ground Signal | 92 | GND | Ground Signal |
| 80 | NC | | 91 | RIOTX_P0 | SRIO Port 0-TX |
| 81 | NC | | 90 | RIOTX_N0 | SRIO Port 0-TX |
| 82 | GND | Ground Signal | 89 | GND | Ground Signal |
| 83 | PS0# | Presence 0 | 88 | RIORX_P0 | SRIO Port 0-RX |
| 84 | VCC12 | +12V Power | 87 | RIORX_N0 | SRIO Port 0-RX |
| 85 | GND | Ground Signal | 86 | GND | Ground Signal |

3.2.3 J3, Ethernet Connector

J3 is vertically stacked dual gigabit ethernet connector with integrated magnetics. It is driven from the 88E1121 Marvell PHY device. The connections are shown in the table below.

Table 5: Ethernet Connector pin out

| Pin # | Signal Name |
|-------|---------------|
| 1 | Port 0 – MD0+ |
| 2 | Port 0 – MD0- |
| 3 | Port 0 – MD1+ |
| 4 | Port 0 – MD1- |
| 5 | Port 0 – MD2+ |
| 6 | Port 0 – MD2- |
| 7 | Port 0 – MD3+ |
| 8 | Port 0 – MD3- |
| 9 | VCC1.8 |
| 10 | Ground |
| 11 | Port 0 – LED+ |
| 12 | Port 0 – LED- |
| 13 | Port 1 – MD0+ |
| 14 | Port 1 – MD0- |
| 15 | Port 1 – MD1+ |
| 16 | Port 1 – MD1- |
| 17 | Port 1 – MD2+ |
| 18 | Port 1 – MD2- |
| 19 | Port 1 – MD3+ |
| 20 | Port 1 – MD3- |
| 21 | VCC1.8 |
| 22 | Ground |
| 23 | Port 1 – LED+ |
| 24 | Port 1 – LED- |

3.2.4 J4, DC Fan Connector

J4 is a 2 pin polarized connector to power, on board FAN for DSP cooling. Pin 1 is +5V and pin 2 is ground.

3.2.5 J5, DB9 Connector

J5 is standard DB9 male connector for RS232 serial interface. The connector presents a DCE interface. A female-to-female straight cable will be needed to connect this to a PC.

Table 6: DB9 Connector pin out

| Pin # | Signal Name |
|-------|-------------|
| 1 | NC |
| 2 | Transmit |
| 3 | Receive |
| 4 | NC |
| 5 | Ground |
| 6 - 9 | NC |

3.2.6 J6, Power Input Jack Connector

J6 is a 3 pin, 2.5mm power jack with the center tip as positive polarity. Do NOT use this connector, if powering the board from the AMC carrier back-plane.

3.2.7 J7, Mini-USB Connector

J7 is a 5 pin Mini-USB connector to connect Code composer studio with C6472 DSP using on board emulation circuitry. Below table shows the pin out of Mini-USB connector.

Table 7: Mini-USB Connector pin out

| Pin # | Signal Name |
|-------|-------------|
| 1 | VBUS |
| 2 | D- |
| 3 | D+ |
| 4 | ID |
| 5 | Ground |

3.2.8 J8, DSP JTAG Connector

J8 is a standard TI 14 pin JTAG connector. The onboard switch multiplexes this interface with the onboard emulation interface. When an external emulator is plugged into J8, the external emulator can connect with the DSP. The I/O voltage level on these pins is 3.3V. So any 3.3V compatible emulator can be used to interface to the C6472 device. Note, that when an external emulator is plugged into this connector (J8), the onboard emulation circuitry will be disabled. The pin out for the connector is shown in the figure below.

Table 8: DSP JTAG Connector pin out

| Pin # | Signal Name |
|-------|--------------|
| 1 | TMS |
| 2 | TRST# |
| 3 | TDI |
| 4 | GND |
| 5 | PD |
| 6 | No pin (Key) |
| 7 | TDO |
| 8 | GND |
| 9 | TCK-RET |
| 10 | GND |
| 11 | TCK |
| 12 | GND |
| 13 | EMU0 |
| 14 | EMU1 |

3.2.9 J9, FPGA JTAG Connector

J9 is a 10 pin JTAG connector for FPGA only. The pin out for the connector is shown in the figure below.

Table 9: FPGA JTAG Connector pin out

| Pin # | Signal Name |
|-------|-------------|
| 1 | TCK |
| 2 | GND |
| 3 | TDO |
| 4 | NC |
| 5 | TMS |
| 6 | VJTAG |
| 7 | VPUMP |
| 8 | TRST# |
| 9 | TDI |
| 10 | GND |

3.3 Switches

The TMS320C6472 EVM Board has three DIP and two push button switches, namely SW1 to SW5. SW1 to SW3 are DIP switches and SW4 and SW5 are push button switches. The function of each of the switches is listed in the table below.

Table 10: EVM Board Switches

| Switch | Function |
|--------|-------------------|
| SW1 | DSP Configuration |
| SW2 | DSP Boot mode |
| SW3 | User switch |
| SW4 | Warm Reset |
| SW5 | Cold Reset |

3.3.1 SW1, DSP Configurations

SW1 is an 8 position DIP switch that is used for DSP configuration. A diagram of SW1 switch (with factory default settings) is shown below.

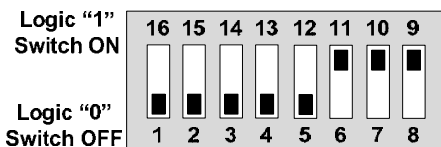


Figure 3.3: SW1 default settings

The following table describes the positions and corresponding function on SW1.

Table 11: SW1, DSP Configuration Switch

| SW1 Position | Description | Default Value | Function |
|--------------|-------------|---------------|--|
| 5 - 1 | CFGG[4:0] | 00000 | DSP Configuration selection Pins |
| 6 | DDREN | 1(ON) | OFF - DDR2 disable ON - DDR2 enable |
| 7 | RIOEN | 1(ON) | OFF - SRIO disable ON - SRIO enable |
| 8 | LENDIAN | 1(ON) | OFF - Big Endian mode ON - Little Endian mode |

3.3.2 SW2, DSP Boot mode

SW2 is a 5 position DIP switch that is used for DSP boot mode selection and system clock out enable option. A diagram of the SW2 switch (with factory default settings) is shown below.

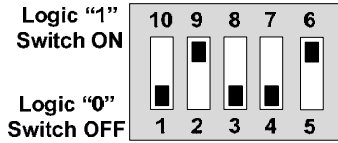


Figure 3.4: SW2 default settings

The following table describes the positions and corresponding function on SW2.

Table 12: SW2, DSP Boot Mode Selection Switch

| SW2 Position | Description | Default Value | Function |
|--------------|----------------|---------------|---|
| 4 - 1 | Boot Mode[3:0] | 0010 | Boot mode selection pins for DSP Master I2C boot mode for I2C address 50h Refer TMS320C6472 datasheet (http://www.ti.com/lit/pdf/SPRS612) for details of other boot modes supported. |
| 5 | CLKOUTEN | 1(ON) | OFF – SYSCLKOUT disable ON – SYSCLKOUT enable |

Note: Please change Boot Mode[3:0] to “0011” for NAND boot mode of this EVM. “0011” is primarily a Master I2C boot mode for I2C address 51h for DSP, which works as NAND boot mode in this EVM.

3.3.3 SW3, User Switch

SW3 is a 2 position user accessible switch. A diagram of the SW3 switch (with factory default settings) is shown below. FPGA monitors status of the user switches and stores its value into internal FPGA registers. The DSP can read user switches’ value by accessing FPGA’s internal registers.

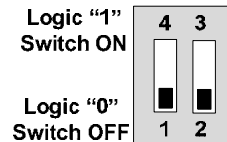


Figure 3.5: SW3 default settings

3.3.4 SW4, Warm Reset

Push button Switch SW4 asserts DSP's RESET# input when pressed. This will reset the DSP and boot parameters will be reloaded.

3.3.5 SW5, Cold Reset

Push button Switch SW5 asserts DSP's POR# and global board reset when pressed. This is equivalent to a power cycle of the board and will have following effects:

- Resets DSP
- Resets FPGA
- Resets Ethernet PHY
- Resets I2C-UART bridge
- Reloads boot parameters.

Re-launch and/or re-connect of CCS application may be required after pressing warm or cold reset buttons.

Note: User may refer TMS320C6272 datasheet (<http://www.ti.com/lit/pdf/SPRS612>) to check difference between assertion of DSP RESET# and DSP POR# signals.

3.4 Test Points

The TMS320C6472 EVM Board has 26 test points. The position of each test point is shown in the figure below.

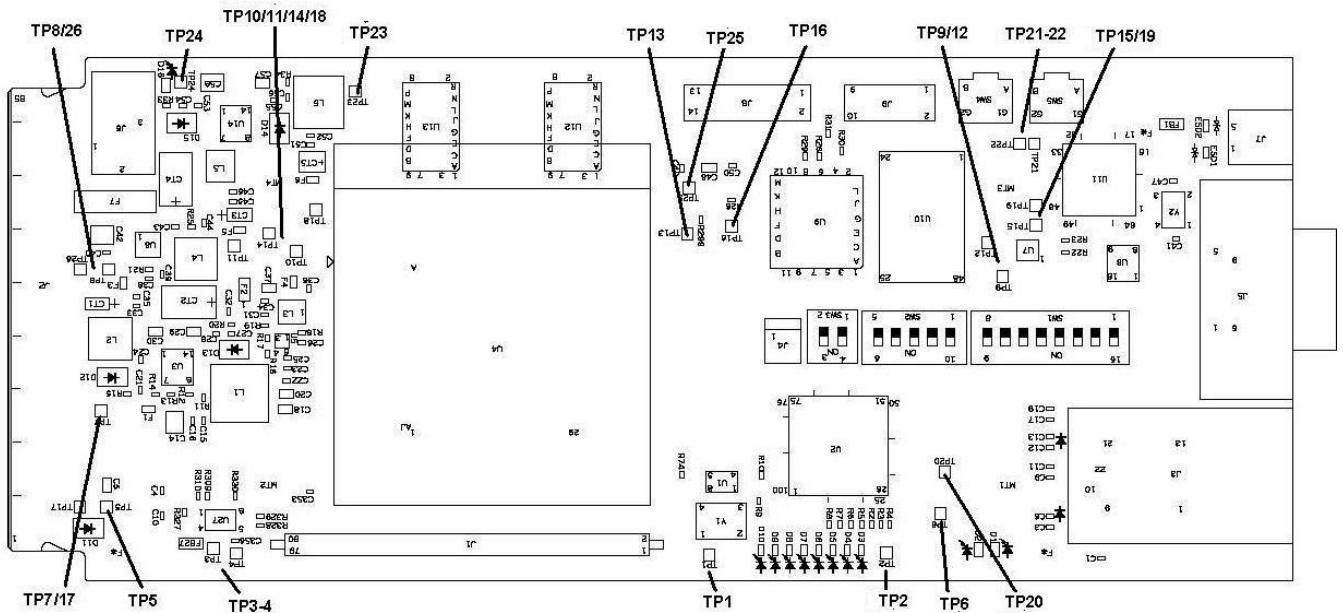


Figure 3.6: Board Test Points

Table 13: EVM Board Test Points

| Test Point | Signal |
|-------------------------------------|--------------------------------|
| TP1, TP5, TP20, TP23, TP25, TP26 | Ground |
| TP2 | Port # 1, LED1 of Ethernet PHY |
| TP3 | RGCLK0 |
| TP4 | RGCLK1 |
| TP6 | Test Point, Ethernet PHY |
| TP7 | +3.3V Supply |
| TP8 | +5V Supply |
| TP9 | System (Cold) Reset |
| TP10 | +1.5 Supply |
| TP11 | CVDD Supply (+1.2V) |
| TP12 | DSP (Warm) Reset |
| TP13 | System Clock Out |
| TP14 | +1.2V Supply |
| TP15 | FT232H, PWREN# |
| TP16 | AMC Detect# |
| TP17 | Management Power (+3.3V) |
| TP18 | +1.8V |
| TP22 | FT232H, GPIOH1 |
| TP24 | +12V Input Supply |

3.5 System LEDs

The TMDXEVM6472 board has eleven LEDs. Their positions on the board are indicated in figure below. The description of each LED is listed in table below.

Table 14: C6472 EVM Board LEDs

| LED# | Color | Description |
|----------|--------|----------------------------|
| D1, D2 | Orange | User LEDs |
| D3 – D10 | Green | I2C LEDs |
| D16 | Green | Board Powered ON Indicator |

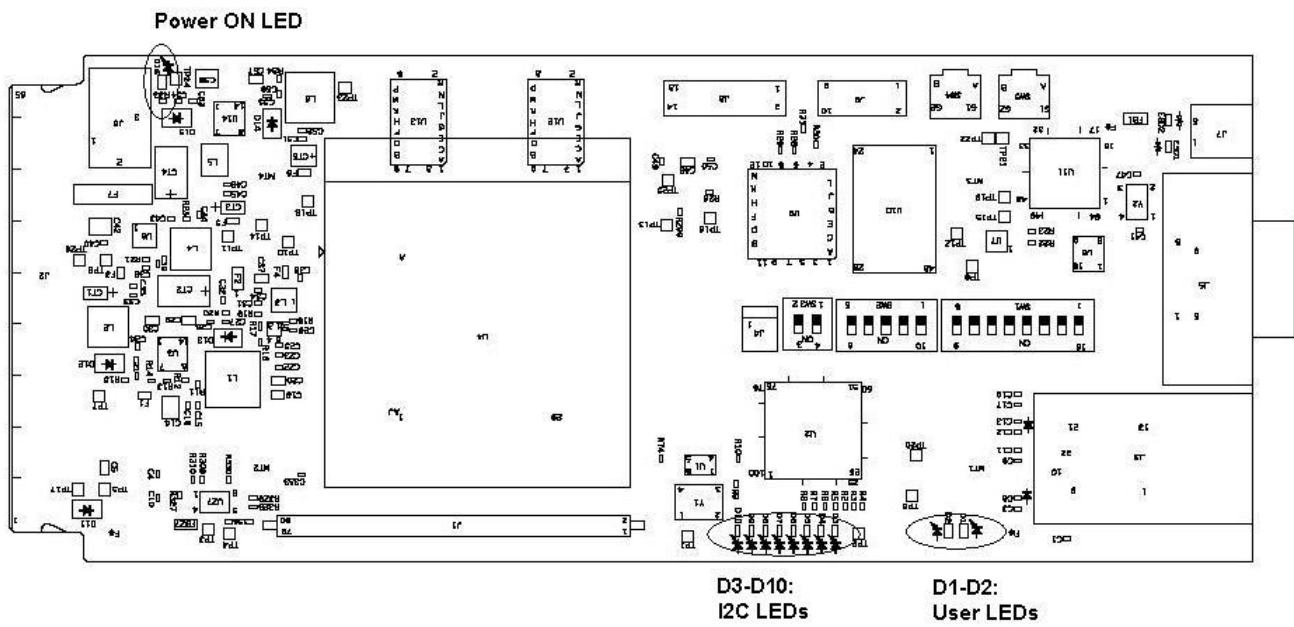


Figure 3.7: Board LEDs

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